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Metal Additive Microfabrication Of Semiconductor Packages With Inbuilt Thermal Management System

Bhushan Lohani
University of Texas at El Paso

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METAL ADDITIVE MICROFABRICATION OF SEMICONDUCTOR PACKAGES WITH
INBUILT THERMAL MANAGEMENT SYSTEM

BHUSHAN LOHANI

Doctoral Program in Electrical and Computer Engineering

APPROVED:

Robert C. Roberts, Ph.D., Chair

David Zubia, Ph.D.

Raymond C. Rumpf, Ph.D.

Brian E. Schuster, Ph.D.

Stephen L. Crites, Jr., Ph.D.
Dean of the Graduate School

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Bhushan Lohani

2023

Dedication

I dedicate this to my parents, Bishnu Raj Lohani, and Bimala Lohani, and my wife Astha Regmi,
for their encouragement and constant support to pursue this degree.

METAL ADDITIVE MICROFABRICATION OF SEMICONDUCTOR PACKAGES WITH
INBUILT THERMAL MANAGEMENT SYSTEM

by

BHUSHAN LOHANI, MSEE, B.Tech.

DISSERTATION

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The two people who brought me to this world and who always have been my source of inspiration, my mom and dad, this is for you. Moreover, I cannot express enough gratitude to my family members who have been my pillar of strength. To my wife Dr. Astha Regmi, for bearing me during these tough years. My sister Barsha Lohani, and siblings Binu and Bidur Lohani, I am forever thankful for your unwavering motivation and support during this journey. To my family members, friends, and colleagues, thank you for your constant presence and support. One name is a must, Chitra B. Karki, one of my friends, we started this journey together and he has been a great support and help throughout this process. Lastly, I want to extend a special thanks to Nitesh Amatya for his exceptional support and encouragement throughout this process.

Abstract

Moore's law describes the development capabilities in electronics manufacturing. Although his estimation held for decades, at present, the doubling of components every two years seems to be approaching a halt. The assessment was based on the miniaturization of transistors to create space for more. Miniaturization led to higher component density, decreased cost, lowered power consumption, and compactness. However, it also came with high current density, increased Joule heating, and reduced critical charge. One of the limiting factors is the heat generated from such devices, which is heavily discussed in International Roadmap for Devices and Systems (IRDS) and International Technology Roadmap for Semiconductors (ITRS). Both the roadmaps have called for appropriate solutions and proposed heterogeneous integration of System in Package (SiP) to be one approach to help solve the problem. The proposal has also led to the formation of the Heterogeneous Integration Roadmap (HIR), which has proposed different solutions for developing the semiconductor industry. ITRS defines "Heterogeneous Integration refers to the integration of separately manufactured components into a higher-level assembly (System in Package – SiP) that, in the aggregate, provides enhanced functionality and improved operating characteristics." One of the possibilities would be the use of additive manufacturing for the heterogeneous integration of assistive devices, for which this field has been heavily explored recently. In this dissertation, metal additive manufacturing, and mostly metal microfabrication, has been researched to study the possibilities of heterogeneous integration. This dissertation will present the metal additive microfabricated SiPs demonstrated by quad flat no-lead (QFN) packages with an integrated microfluidic and pin-fin thermal management system for semiconductor devices. This metal additive microfabrication for microsystems is also compared with the conventional cleanroom processes.

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Chapter 1: Introduction

1.1. Hotspots Generation in Semiconductor Devices

The semiconductor industry has been keeping up with the demand for high-performance electronic devices to process and handle the ever-increasing data [1], [2] by incorporating a large number of smaller components on a single chip [3], [4]. An increase in component density without increasing the overall footprint of a chip is made possible by the proportional decrease in the gate length of each component and then the crowding of the integrated circuit (IC) with these smaller components [5]. Moore's law guided this approach of cramming more components onto a single integrated circuit [6]. Another trend seen in the power electronics field is the use of wide-bandgap devices to increase power efficiency [7], [8]. The mentioned miniaturization and use of wide-bandgap devices have led to increased current and power density and Joule heating, resulting in localized hotspot generation on the channels [9]–[15].

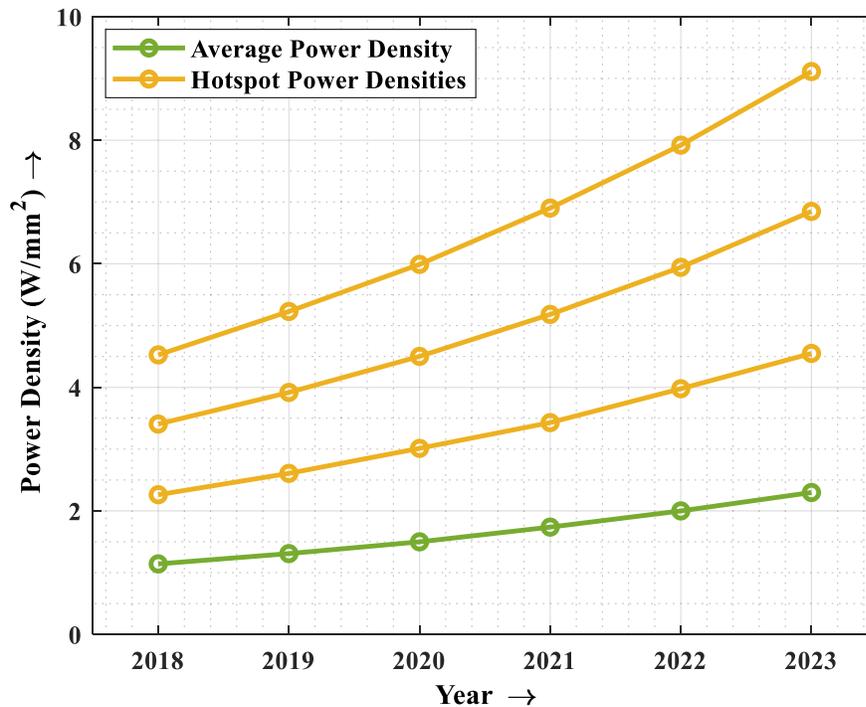


Figure 1.1: Average and hotspot power density as predicted by HIR (Reproduced from: Heterogeneous Integration Roadmap- Chapter 20 [16])

As per the thermal demand envelopes in Fig. 1.1 elucidated from the HIR, the hotspot power density is more than four times the average power density [16]. This localized hotspot on the active region then gets conducted to the junction, increasing the device junction temperature as well as the whole chip resulting in the overall increase in the IC temperature [17] as shown in Fig. 1.2. The increased hotspot degrades the performance, reliability, and lifetime of the electronic devices [18].

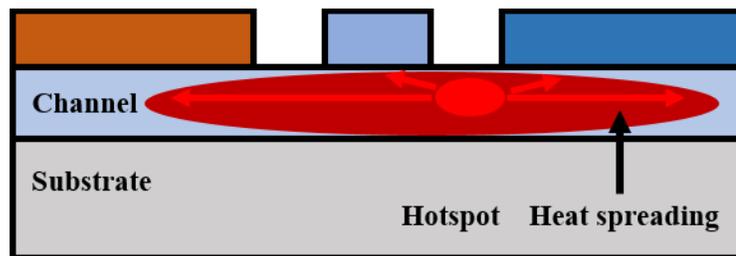


Figure 1.2: Generation of hotspot on channel (bright red) due to higher hotspot power density and spread of heat towards the junction in semiconductor devices: a demonstration.

1.2.Effect of Hotspots in Semiconductor Devices

Hotspots in semiconductors are one of the various challenges faced by today's semiconductor industry. The increase in the temperature of the IC affects its performance as the concentration of electrons and holes in silicon increases with temperature. This alteration due to the temperature increase affects the reliability of the device. A study by NXP Semiconductors Inc. on the temperature dependency of their P-N Junction diodes' forward voltage would be an exciting finding to demonstrate this point. The study showed that the forward voltage keeps decreasing with temperature, as shown in Fig. 1.3[19]. Upon extrapolation of the forward voltage, it reaches 0 volts at a temperature of 318.81°C, and this is a very much attainable temperature based on the increasing hotspot power densities demonstrated in Fig. 1.1. A similar relation between temperature and base-emitter junction voltage can be expected for Bipolar Junction Transistors (BJT). As the gate-source threshold voltage also decreases with the increase in temperature, effects

similar to the P-N junction diode can be deduced for metal-oxide-semiconductor field-effect-transistors (MOSFET). This phenomenon invites an even bigger problem: a high temperature resulting from a localized hotspot might result in a small voltage at the respective junctions for diodes, BJT, and MOSFET to turn on the devices even when they are supposed to be off. The undesirable “on” state again increases the junction temperature, further decreasing the switching voltage, and continues as a vicious cycle until the devices endure permanent damage.

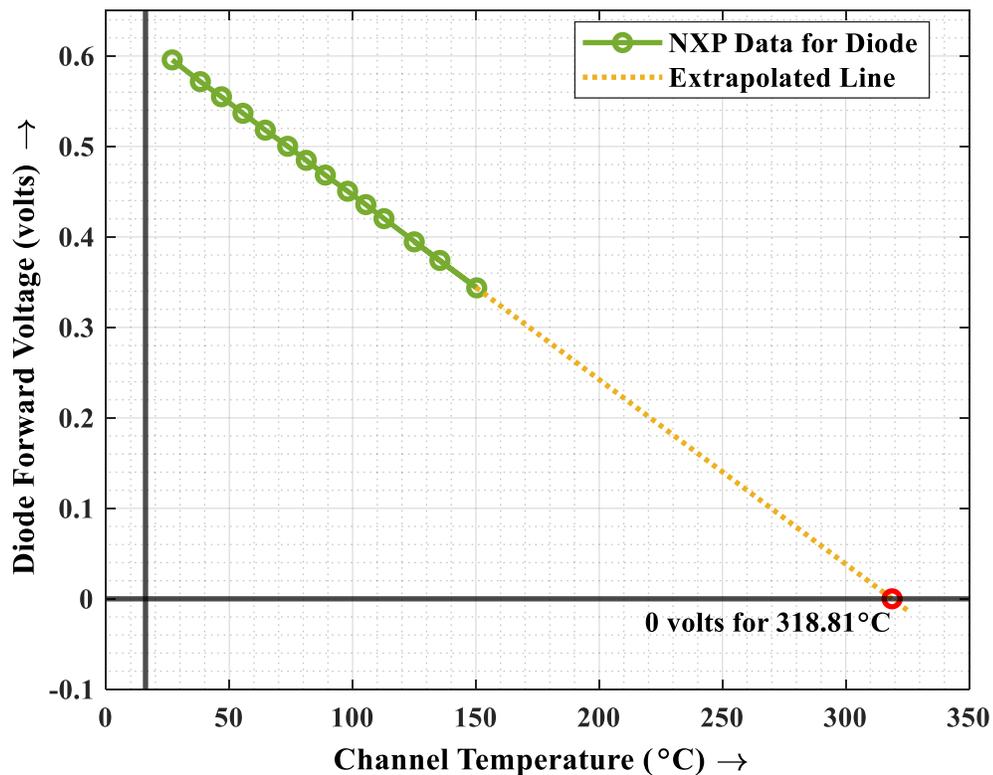


Figure 1.3: Diode forward voltage as a function of operating channel temperature from the NXP white paper [19] and the extrapolation of the data indicating the temperature at which the forward voltage reaches 0 volts.

As discussed previously, the increased hotspots degrade the IC’s reliability. At present such degradation is avoided by, most of the time, operating the devices under their nominal operating limits [20]. In other words, ICs today operate below their thermal limit rather than their electronic limit; the latter is often much higher than the formal one. This difference in the theoretical

operating power and the present operating power limited by the thermal limit is demonstrated in Fig. 1.4., obtained from a talk by Defense Advanced Research Project Agency (DARPA) scientists, where the power amplifiers, at present, are operated almost ten times below their electronic limit due to the thermal bottleneck [21], [22]. This inability to operate devices at their electronic limits not only degrades the device’s performance but also undermines several decades of endless research from around the world for the improvement of electronic devices.

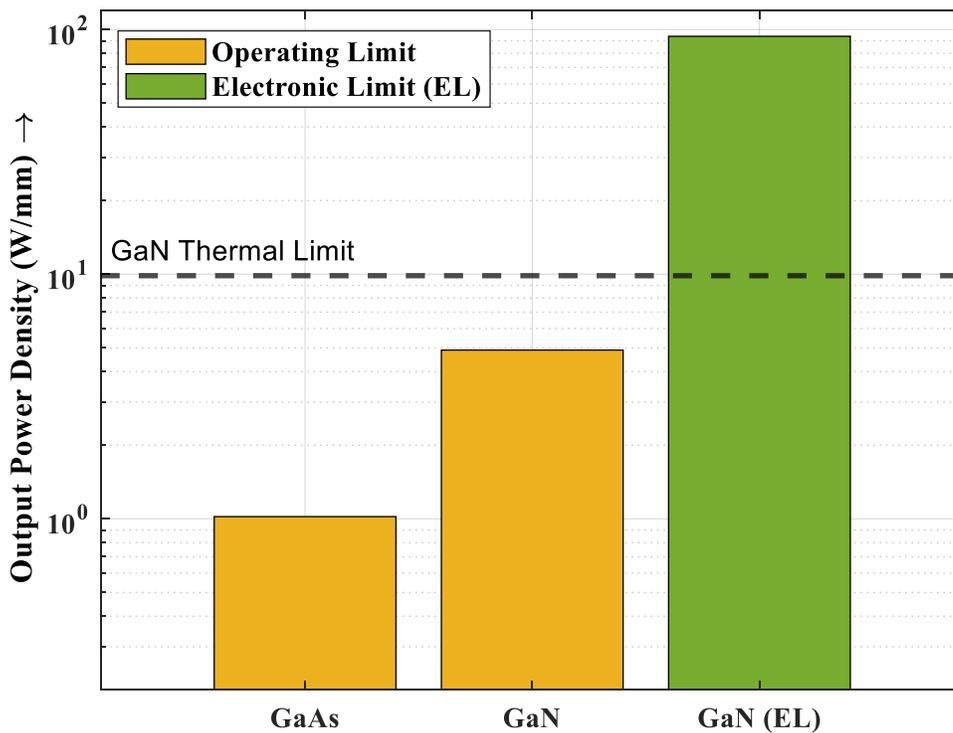


Figure 1.4: Thermal bottleneck as the limit for the operation of GaAs and GaN power amplifiers as discussed by DARPA scientist.

Another effect of hotspot is the degradation of overall functional lifetime of the device. Researchers have predicted that with every 10°C rise in the operating temperature, the overall lifetime of an electronics device decreases by half following an approximation like Arrhenius equation generalization used in chemistry for chemical reaction rates dependency on temperature [23]. There are also some criticisms for this logic [24] but a simple example for a case of a power

amplifier (Qorvo QPD0030) seconds that the Arrhenius equation generalization might give the basic idea of temperature dependency on the Median Time to Failure (MTTF) of a power amplifier. As demonstrated in Fig. 1.5., derived from the datasheet of the mentioned power amplifier.

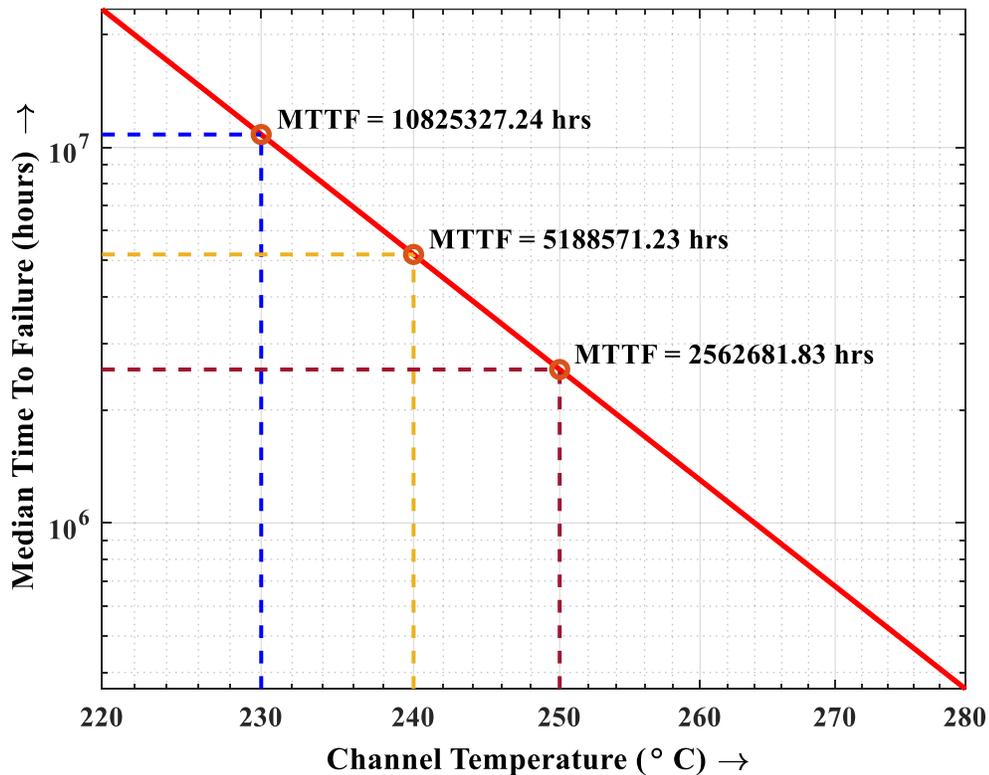


Figure 1.5: Median Time to Failure (MTTF) in hours at different operating temperatures (220°C to 280°C) for QPD0030 power amplifier as obtained from the manufacturer’s datasheet [25].

Fig. 1.5., shows a part of the plot of MTTF vs Channel Operating Temperature of the mentioned power amplifier. The temperature range in the x-axis is the actual temperature range for the operation of the device as per the datasheet. It is clear from the plot that the for every 10°C rise in temperature the MTTF value is decreasing by two times, for example, the MTTF for the device operating at the channel temperature of 230°C is around 10.8E6 hours, and it decreases to around 5.2E6 hours if the channel temperature is increased to 240°C, implying the decrease of MTTF by two times for a 10°C rise in temperature. Similarly, for the channel temperature of 250°C

(another 10°C rise), the MTTF decreases to around 2.6E6, which is also two times decrease as compared to the MTTF for 240°C.

The discussions in the previous paragraphs shed light onto the need for proper thermal management of electronic devices for the improvement of performance, reliability, and improved lifetime of the devices. As the present electronic industry is determined to move towards heterogeneous integration of a number of devices onto a single SiP, embedded thermal management will be required for individual devices to avoid the confinement of heterogeneously integrating only to the low power chips [26]. Introduction of advanced semiconductor cooling technologies is a must for the advancements of electronic devices to avoid the thermal bottleneck faced by present devices. Semiconductor cooling can be performed via three different modes. Conduction of the transfer of heat energy between stationary molecules without the involvement of the actual movements of the bodies. Compared to other modes of heat transfers, this method is a relatively slower process. Convection heat transfer takes place by movement of fluids (air or liquid) and is a faster and more efficient process of heat removal compared to conduction. Radiation involves removal of heat in the form of electromagnetic waves but is weak below 400°C.

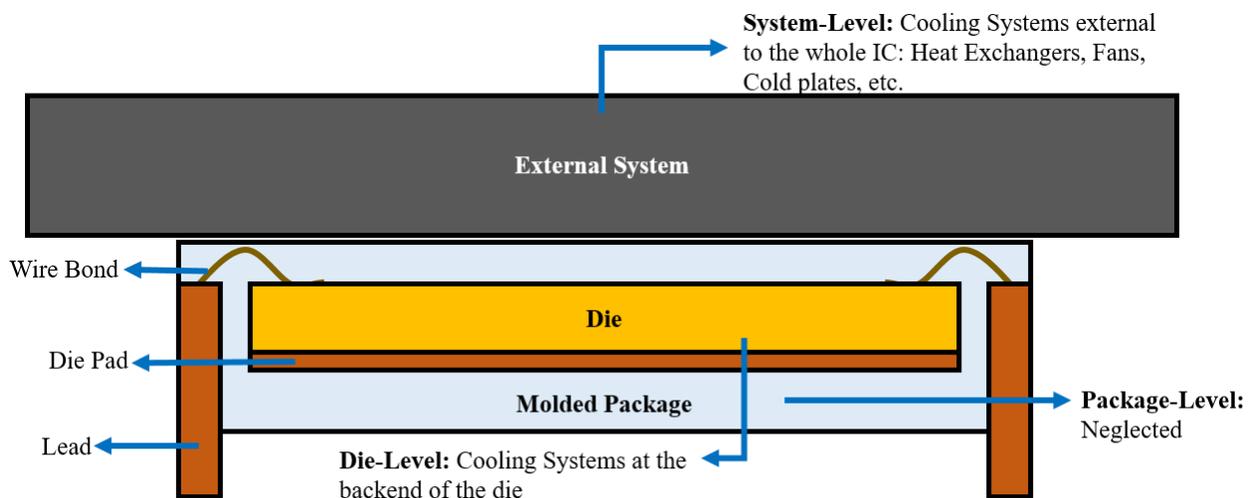


Figure 1.6: Cartoon demonstrating a fully packaged IC and different levels where thermal management can be added.

1.3.Semiconductor Cooling: Present State of Practice

There are various levels of thermal management for electronics in practice. The cartoon in Fig. 1.6., displays a general demonstration of a fully packaged IC with die on the die pad of a package, connected to the leads via wire bonding inside a molded package. Conventional packages, with die pad and leads are created from metal plates by stamping or etching and have no other functionalities except for holding the die (die pad) and connecting the die to the external via wire bonding with the leads. To prevent the die and bonds from environment, the die and package combination is covered with epoxy forming the molded package. The current state of practice also includes additional external systems like heat exchangers, fans, cold plates, etc. for heat removal. Fig. 1.6., also demonstrates the different location or levels where thermal management can be added.

1.3.1. System-Level Thermal Management

The current state-of-practice for semiconductor cooling is the use of macroscopic scale heat sinks which move heat away from IC quickly and eliminate it using cooling mechanism like fans as seen in Fig. 1.7., (top). Cooling fins are sometimes placed in direct contact with the packaged high power density semiconductor devices and heat removal is obtained by air flow into the fins as seen in Fig. 1.7., (bottom). These types of cooling systems are quite common ones seen in the majority of the devices, from computers and laptops to vehicle parts. They are low cost and easily available due to their established fabrication. However, due to several interfaces, and conduction being the main mode of heat transfer mode in these system-level coolants, they are slow and possess higher thermal resistance. Their cm-scale sizes also make them consume a large space and hence sub-optimal.

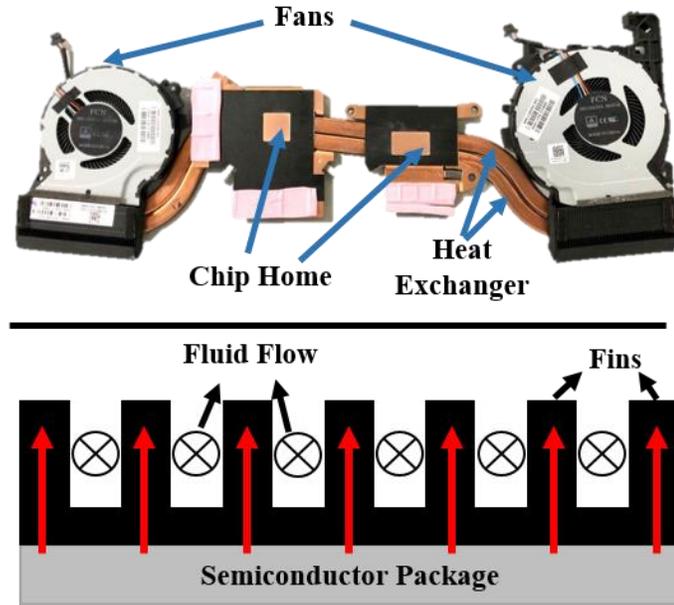


Figure 1.7: System-Level Thermal Management comprising of thermally conductive copper heat exchangers and fans (top) and fin array placed in direct contact with package.

1.3.2. Die-Level Thermal Management

Microfabrication of microfluidic channels on the backend of a semiconductor die with electronic components on the front side was first demonstrated by Tuckerman and Pease in 1981 [27]. The work formed the basis of Die-Level Thermal Management of semiconductor devices and a lot of works have been done at this level as well. Apart from microchannel, Chou et.al, also initiated the idea of using micro pin-fin for cooling in 1999 [28]. The rationale for using microfluidic structure is because these structures when supplied with water or fluid flow increase the ratio of total fluid volume by total wetted area consequently increasing the overall convective heat transfer coefficient [29], [30]. Researchers have etched, mostly Deep Reactive Ion Etching (DRIE), at the backend of the semiconductor die to introduce direct convective cooling microfluidic channels [31]–[33] or micro pin-fins [34], [35]. These microfluidic structures are then covered by attaching to another silicon or glass as shown in Fig. 1.8. With introduction of direct

convective cooling very close to the heat source (electronic components at the front end) make these cooling systems efficient and compact on top of reduction of thermal resistance bypassing the thermal resistance of several interface materials used in System-Level Thermal Management setups. However, they also come with higher cost and complicates the already complex IC fabrication with addition of backend processes. The electronic components on the front end are also strained during the microfabrication of the microfluidic channels. The complexity and additional strains might be the reason for Die-Level Thermal Management appears to always be limited to academic research and has not seen commercial mass fabrication. However, studies in this level have opened pathways for the third level discussed in this dissertation.

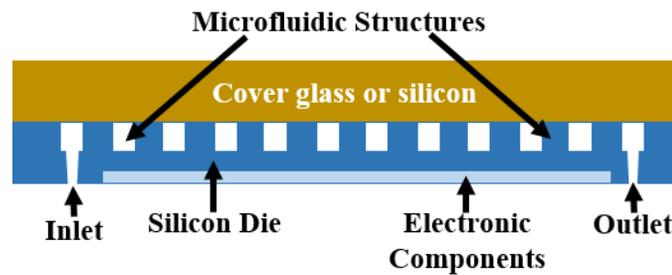


Figure 1.8: Die-Level Thermal Management comprising of silicon die with components at frontend and itched microfluidic structures at the backend covered with glass or another silicon.

1.3.3. Package-Level Thermal Management

The third location or level where the cooling systems can be added would be at the package-level. However, this level of thermal management integration is mostly neglected. The state-of-practice for packages is limited to creating housing for the die as die pad, connection from die to the leads and to the external, and epoxy molding to prevent the die from the external environment. The die pad if extended and microfluidic structures as in the die-level cooling systems if fabricated onto the die pad, the hence formed package-level thermal management systems would be closely as efficient as the die-level cooling systems. This level can be designed to lie between the die-level

and system-level. Cooling at this level can bypass the thermal resistance imposed by interface materials in the system-level without complicating the IC fabrication as suffered by the die-level. Like die-level, this level also employs efficient direct convective cooling. For this dissertation a normal lead frame package was taken, and microfluidic cooling was added to improve its thermal management performance as demonstrated in Fig. 1.9.

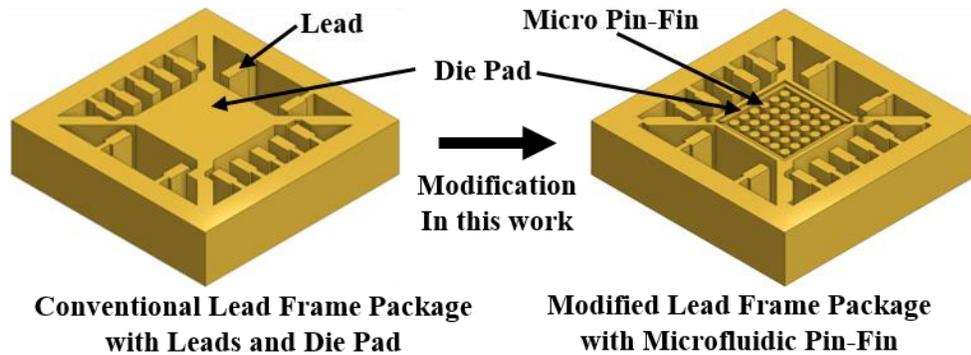


Figure 1.9: Conventional lead frame package for semiconductor die (left) and addition of microfluidic pin-fin on the die pad for improvement of its thermal management performance.

1.4. Microfluidic Cooling in Packages: The Why and How?

It might have been clear from the previous sub-sections that this dissertation is based on the package-level thermal management of semiconductor devices. However, the rationale for the mentioned microfluidic channels and pin-fins is derived from the heat transfer study of those structures. The convective heat transfer coefficient due to a fluid flowing through a tube is given by equation 1.1 [36].

$$h_c = \frac{Nu \times k}{D_h}$$

Equation 1.1

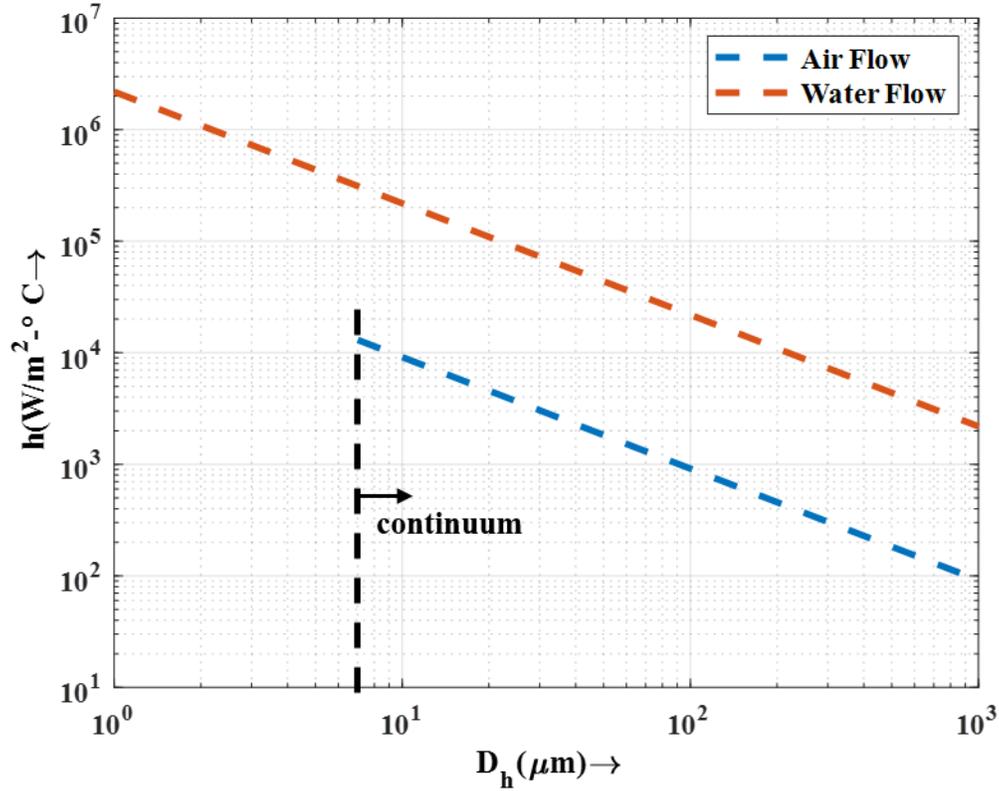


Figure 1.10: Theoretical values for the heat transfer coefficient (h_c) with respect to the hydraulic diameter (D_h in the range of $1\mu\text{m}$ to $1000\mu\text{m}$) for microchannel for air and water as the fluid flow

As seen in the equation, the heat transfer coefficient (h_c) due to the flowing fluid in the tube depends on parameters like Nusselt Number (Nu) pertaining to the flow, thermal conductivity of the flowing fluid (k_c), and the hydraulic diameter (D_h). Nusselt Number is the ratio of convective to conductive heat transfer across the boundary of the fluid flow and is predicted to be almost constant for laminar flow [37], the type of flow predicted to be dominant in microchannel [38]. In simple words, the Nusselt Number of a fluid flow tells if the flowing fluid is transferring heat by conduction or convection. If the change in thermal conductivity of the flowing fluid (k_c) is assumed to be minimal for small changes in temperature, then the only parameter h_c depends inversely on will be the hydraulic diameter (D_h). As we go on decreasing the value of D_h , the value of h_c keeps increasing as long as the condition for continuum, thermodynamic equilibrium, no-velocity slip, and no-temperature jump condition are met [39]. For micro-meter sized D_h , in the range of 1 to

1000 μm (for which all the conditions mentioned in the previous lines are met), h_c would be in the 10^3 to 10^6 W/m^2 as seen in Fig.1.10., range which is a huge enhancement in the heat transfer coefficient. This huge improvement of h_c is the reason for using microfluidic channel in this work.

Another procedure to enhance the convective heat transfer coefficient is to decrease the ratio of the total volume (V_{fluid}) of coolant flowing and the total wetted surface area (A_{fluid}) as the expression for hydraulic diameter (D_h) is as shown in equation 1.2 [40].

$$D_h = \frac{4 * V_{\text{fluid}}}{A_{\text{fluid}}}$$

Equation 1.2

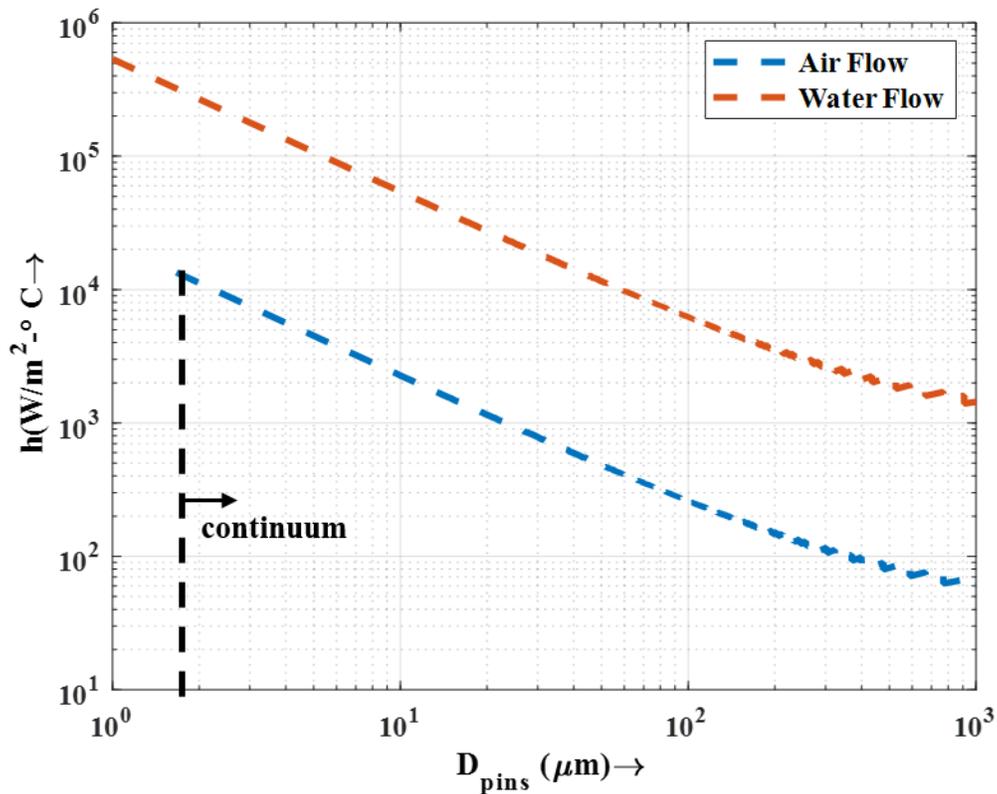


Figure 1.11: Theoretical values for the heat transfer coefficient (h_c) with respect to the diameter of the micro pin-fin (D_{pins} in the range of $1\mu\text{m}$ to $1000\mu\text{m}$) for air and water as the fluid flow.

As per equation 1.2., if a square flow area is considered, it would be possible to decrease the total fluid flowing through it and at the same time increase the total wetted area by introducing structures like pins in the flow regions. In other words, formation of pins on the flow region will decrease the hydraulic diameter and increase the heat transfer coefficient (h_c) as per equation 1.1. Fig.1.11., shows the h_c values derived from equations 1.1 and 1.2 for a 1cm-by-1cm fluid flow region for different diameters of pins on the x-axis. As seen in the figure, decreasing the diameter of the pins to micrometer level, at the same time making space for more and more pins can improve h_c to a greater extent. This improvement can be taken into consideration for the use of microfluidic pin-fins for thermal management.

As discussed in the previous sections, microfluidic structures like microchannel and micro pin-fins are excellent options for cooling and can be used for electronic cooling. When it comes to analysis of physics of liquid flow in microfluidic structures, it has not been well known [39], [41]. However, many studies have demonstrated the thermal efficiency enhancement introduced due to presence of microfluidic structures. One study acknowledges the enhancement due to onset of thin water film formation, and its evaporation resulting into higher heat transfer in two phase cooling [42]. Similar enhancement in heat transfer can be imagined for single phase cooling. A review on single phase cooling deduces that the flow compression in microfluidic causes surface friction leading to turbulence and higher heat transfer [43]. Addition of flow disturbing structures like micro-pin fins has been deemed to induce bubble formation and better mixing of fluid enhancing the heat transfer [44]. Hence, turbulence and fluid mixing in microfluidic structures might be the main reason for the enhancement of heat transfer coefficient in this domain. In conclusion, microfluidic structures like micro pin-fins and microchannels can enhance cooling. This dissertation considers the fact mentioned and employs metal additive microfabrication of lead frame packages with microchannel or micro pin-fin and studies the heat transfer efficacy of such packages. The rationale for using metal additive microfabrication for fabrication of these microfluidic structures for electronics cooling, which otherwise is fabricated on silicon via etching

in cleanroom, is because of the excellent features of metal additive manufacturing like rapid prototyping and testing of such packages, flexibility of design, low cost for prototyping, lower material waste, etc. Here onwards, metal additive microfabrication and characterization of lead frame packages with microfluidic cooling for implementation of package-level thermal management will be extensively presented.

Aim and Research Objective

This Ph.D. dissertation deals with the exploration of DMLS/ μ MMS for the microfabrication and characterization of electronic packaging devices. DMLS/ μ MMS works by selectively sintering precursor fine metal powder in a layer-by-layer fashion based on the slices of the 3D CAD file fed to the printing system. It is hypothesized that these printed metal parts will have some changes in their physical and mechanical properties compared to the bulk metal parts due to the introduction of microstructures by the print process. This proposal intends to study such deviation on a few of those properties like resistivity, thermal conductivity, and surface roughness associated with the final product, which is a semiconductor packaging device with embedded microfluidic thermal management. The degree of effects of such deviation on the final packaging device performance will also be studied. Finally, the thermal management and electrical performance of such packages will be determined, along with the determination of the optimized design. This work will try to develop package or SiP-level thermal management as proposed by the thermal technology work group for HIR. As the mentioned level of thermal management is proposed but a complete package-level thermal management solution is lacking till date, this work might be one of the firsts in this domain. In a condensed form, the major research objective would be to answer the following research question associated with metal additively microfabricated packaging devices printed using DMLS or μ MMS:

- Is it possible to create a complete package-level thermal management solution with lead frame as a proof of concept as proposed by HIP?
- How will the thermal management system in this fairly new package domain perform compared to state-of-the-art devices?
- What would be the best design for the optimized thermal management of these kinds of systems?
- Is it possible to use metal additive microfabrication to produce these package-level solutions to decrease the strain on chip manufacturing?
- What are the dimensional differences between the CAD file and as printed parts of the metal packages created using the technology of interest?
- What are the changes in physical and functional characters of printed parts compared to the bulk material? How does the study of the microstructure of the printed parts correlate to changes in electrical resistivity, thermal conductivity, the strength of the material, and surface roughness of the parts and possibly the effects of them on the thermal management and electrical performance of the overall electronic packaging device?
- How similar are the functionalities of printed systems compared to multiphysics simulations and similar parts created using conventional cleanroom processes?

Organization of Dissertation

Chapter 2 provides the background on the rationale for using additive manufacturing and its comparative study with cleanroom processes. Chapter 3 provides a brief introduction of some

additive manufacturing technologies with a focus on DMLS. Chapters 4 and 5 report the preliminary works of this dissertation with Chapter 5 introducing the major work. Chapter 6 discusses the final optimization and results with Chapter 7 concluding the dissertation with the findings and possible future works.

Chapter 2: Background

2.1.Literature Review: Technologies for Thermal Management in Electronics

The thermal management of electronics commonly utilizes heat sinks in the form of fans and conductive metal plates [45]. This cooling mechanism involving the final air-cooling systems is very commonly seen in a lot of devices. However, the long conduction path [46] and today's chip hotspot power density exceeding the cooling capacity of these heatsinks [47] has caused an increase in the size of heat sinks which negates the whole purpose of component miniaturization [48]. Highly conductive substrate materials like gas-derived graphite fibers [49] have been proposed for passive and quick heat transfer but introduce intermediate thermal resistance. The present increases in chip hotspot density have called for the need for liquid cooling.

The history of liquid cooling of electronics is attributed to Tuckerman and Pease, who designed the first microfluidic cooling systems on the back end of the die [27]. Since then, a lot of work has been done around the liquid cooling of electronic devices using several technologies. Forced convective cooling of the semiconductor by direct flow of coolant parallel to the back side of the die using a liquid injection port was proposed [50], but this imposed greater pressure on the solder. One solution for this could be the flow of coolant inside a cold plate that is in direct contact with the die [51], but this introduces high heat resistance between the die and the cold plate. Immersion cooling, where the whole IC is immersed into the coolant [52], appears promising, but the dielectric coolants used in these methods possess poor thermophysical properties. There are several other methods of cooling electronics with liquid coolants, like spray cooling, jet impingement cooling, droplet electrowetting cooling, etc. [53]. Still, all these excellent cooling technologies come with their disadvantages in one form or another. Out of all these options,

microfluidic cooling is considered a superior one in terms of its compact size and higher heat transfer capability [53].

The large number of published works in literature indicates the popularity of microfluidic cooling. Many researchers have employed microfluidic cooling at the back end of a die to impart direct cooling of the device comprising the die-level thermal management [27], [32], [33], [54]–[57]. It should be noted that by die-level thermal management, it means the die itself is directly exposed to the coolant. Works on creating microfluidics in a metal plate closed on all sides except the inlet and outlet are categorized as cold plates [58], [59]. The introduction of microfluidic structures on the back side of the die and its complications have already been discussed in the previous chapter. These cooling systems, although highly efficient and compact, are expensive and complicated to fabricate. This issue can be solved by leaving the electronics fabrication in the cleanroom and assigning new fabrication domain like additive manufacturing for thermal management system fabrication and then heterogeneously integrating both.

Additive Manufacturing, initially developed to produce larger parts, has now been employed for micro-scale device fabrication [60]. The tools for additive manufacturing have been updated to produce smaller parts and can also be used for microfabrication of more minor features like microchannel and micro pin-fins. Collins et al. have developed a microchannel cold plate using metal additive microfabrication to study the possibility of this new manufacturing domain [61]. A Microsystem in the form of an electrostatic MEMS switch has been fabricated using micro laser sintering with a feature size of around $40\mu\text{m}$ [60]. Microelectrode arrays in the diameter range of $260\mu\text{m}$ are one more example of how small a micro laser sintering can print [62], forming the foundation for the micro pin-fin fabrication. The flexibility of design and fabrication of direct

metal laser sintering has been thoroughly explored by Shamvedi et al. [63] by fabricating different shapes of heatsinks. Hence, there is a prospect of using metal additive manufacturing for microfluidic cooling systems design, which is explored in this work.

2.2. Why Additive Manufacturing?

Additive Manufacturing (AM), commonly known as three-dimensional (3D) printing, previously referred to as rapid prototyping, is a process by which a 3D structure is created by fusing materials in a layer-by-layer fashion directly from computer-aided design (CAD). AM is considered a noble technology introduced by today's industrial developments [64]. It has been named one of the disruptive technologies to bring about a revolution in the present industrial era [65]. For the same reasons, this technology has found many applications in the fields of manufacturing [66]–[70], construction industries [71]–[74], biomedical materials, devices, and implants [75]–[79], electronic devices [80]–[82], micro-electromechanical systems (MEMS) [60], [83], [84], sensors [85]–[87], and many more. The popularity of 3D printing is increasing due to its ease of use, low cost, versatility, low waste products, minimal to no use of hazardous chemicals, and the possibility of its integration into semiconductor fabrication [88]–[93]. Other features, like print structure and parameter optimization, lower power consumption, reusability of materials, and production scalability, have encouraged its use in low-volume prototype fabrication [93]. The capability of additive manufacturing technologies that can use diverse raw materials, from metals to insulators, including semiconductors, has inspired industries, national labs, and researchers for its further developments, optimization, incorporation into education, and standardization [94]–[99]. One of the most attractive features of additive manufacturing is its ability to fabricate

products directly from CAD files. One can easily set the custom dimensions, load the printer with the desired material, start it, and obtain the manufactured product with the same or almost the same dimension as the design. This fabrication flexibility has gathered much attention in modern manufacturing [100]. Further details about the advantages, available technologies, and applications of AM will be discussed in upcoming chapters focusing on metal additive manufacturing.

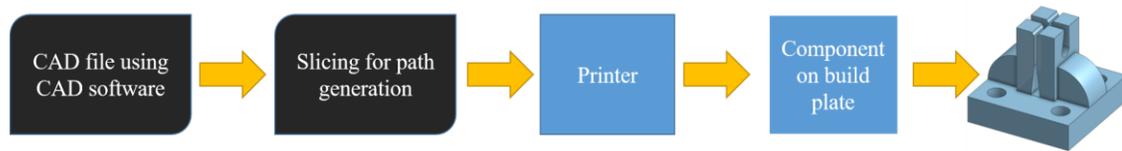


Figure 2.1: Typical manufacturing steps for Additive Manufacturing Technologies

2.3. Additive Manufacturing Basics

Additive Manufacturing comprises a group of manufacturing technologies that have the capability of manufacturing components a component in a layer-by-layer fashion until the desired component is built. The component is built directly from a CAD file after appropriate slicing of the design itself. The CAD files can be drafted using various CAD software like Onshape, SolidWorks, AutoCAD, TinkerCAD, and many more. The slicing of layers can be done using software like Ultimate Cura, Netfabb, Magic, and others. In other words, one can create a computer-based customized design and instruct the 3D printer to directly print the component. This feature encompasses a lot of flexibility and customization capability which has been widely explored to create a lot of components for different applications like construction, manufacturing, electronic devices, sensors, transducers, MEMS devices, and many more. Fig. 2.1., shows the

process flow of a typical Additive Manufacturing technology showing its versatile and customizability capability.

The above-mentioned features of customizability, versatility, ease of use, and flexibility have garnered a lot of attention towards 3D printed components fabrication and characterization. A lot of researchers have been focusing on the use of additively manufactured parts. Fig. 2.2., shows the publication trends data when the keywords Additive Manufacturing, 3D Printing, and Metal Additive Manufacturing were searched in Clarivate Web of Science™. The almost exponential growth in the number of publications each year certainly shows the amount of work that has been ongoing in the field of additive manufacturing.

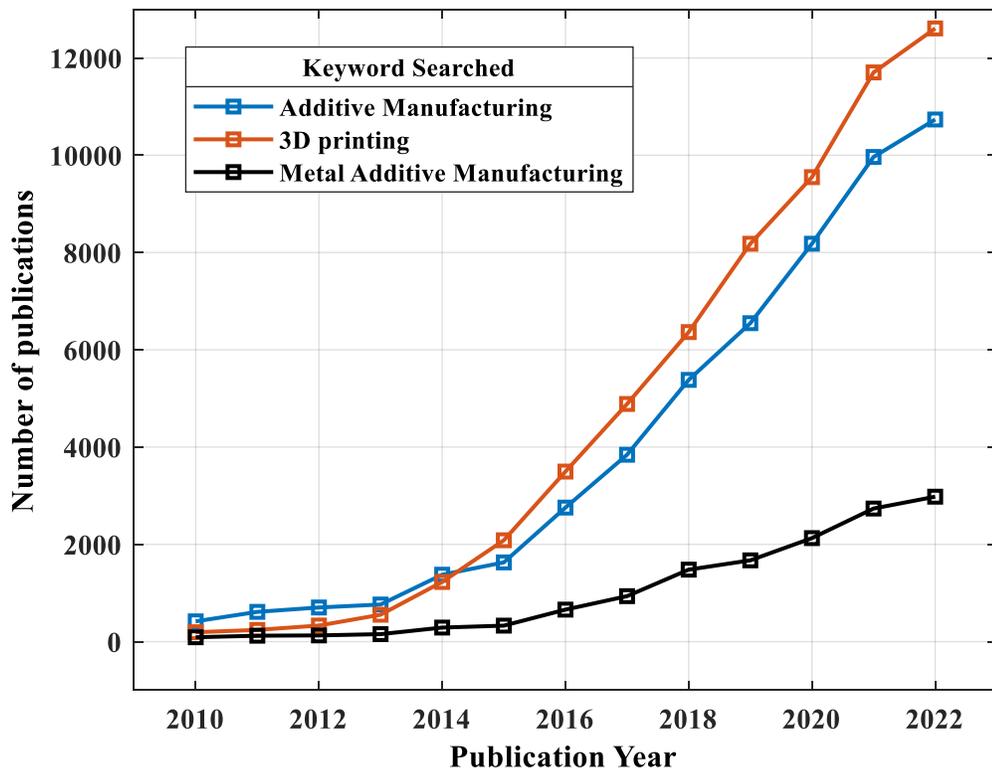


Figure 2.2: Publication trends for AM, 3D printing, and Metal AM from 2010 to 2022.

2.4.Additive vs Subtractive Fabrication of Electronic Devices

Additive manufacturing has been advocated by several researchers as a process capable of competing with and/or complementing conventional manufacturing [101]–[104]. The conventional process for electronics manufacturing follows successive additive and subtractive processes like deposition, photolithography, masking, etching, and many other complicated, time-consuming, as well as expensive processes inside an expensive clean room with a controlled environment [104]–[107]. AM, however, has the capability of fabricating similar devices bypassing most of the aforementioned processes. This flexibility creates hopes of further development of the technology to achieve its expected heights.

The use of 3D printing has been explored mostly for biomedical devices and implants fabrication [108]–[111]. However, several works have been done in the field of MEMS devices [60], RF antennas and waveguides [112], antennas [87], and more. This being said, the technology might soon develop to fabricate realistic electronic devices as this process requires lesser steps for manufacturing compared to traditional clean rooms as demonstrated by Fig. 2.3. The figure shows the steps in cross-section required to just fabricate a three electrode MEMS device (discussed in detail in Chapter 4) using additive manufacturing (in light green background) compared to a conventional clean room process (in light blue background) and the final product from additive manufacturing. As demonstrated by Fig. 2.3., conventional process comprises of a lot of redundant processes.

2.5.Advantages of Additive Manufacturing over Cleanroom Processes

As demonstrated by Fig. 2.3, conventional process of fabricating a simple three electrode switch has to go through a lot of steps starting form metal deposition on the substrate, to photoresist

coating and baking, photolithography using a mask to cure photoresist only at the region of interest (ROI), removal of uncured photoresist, etching to remove metal from all other regions except for the ROI, and a final step of dissolving the remaining photoresist. All these processes are tedious, need trained manpower, used chemicals, and needs to be performed inside an expensive to manage clean room.

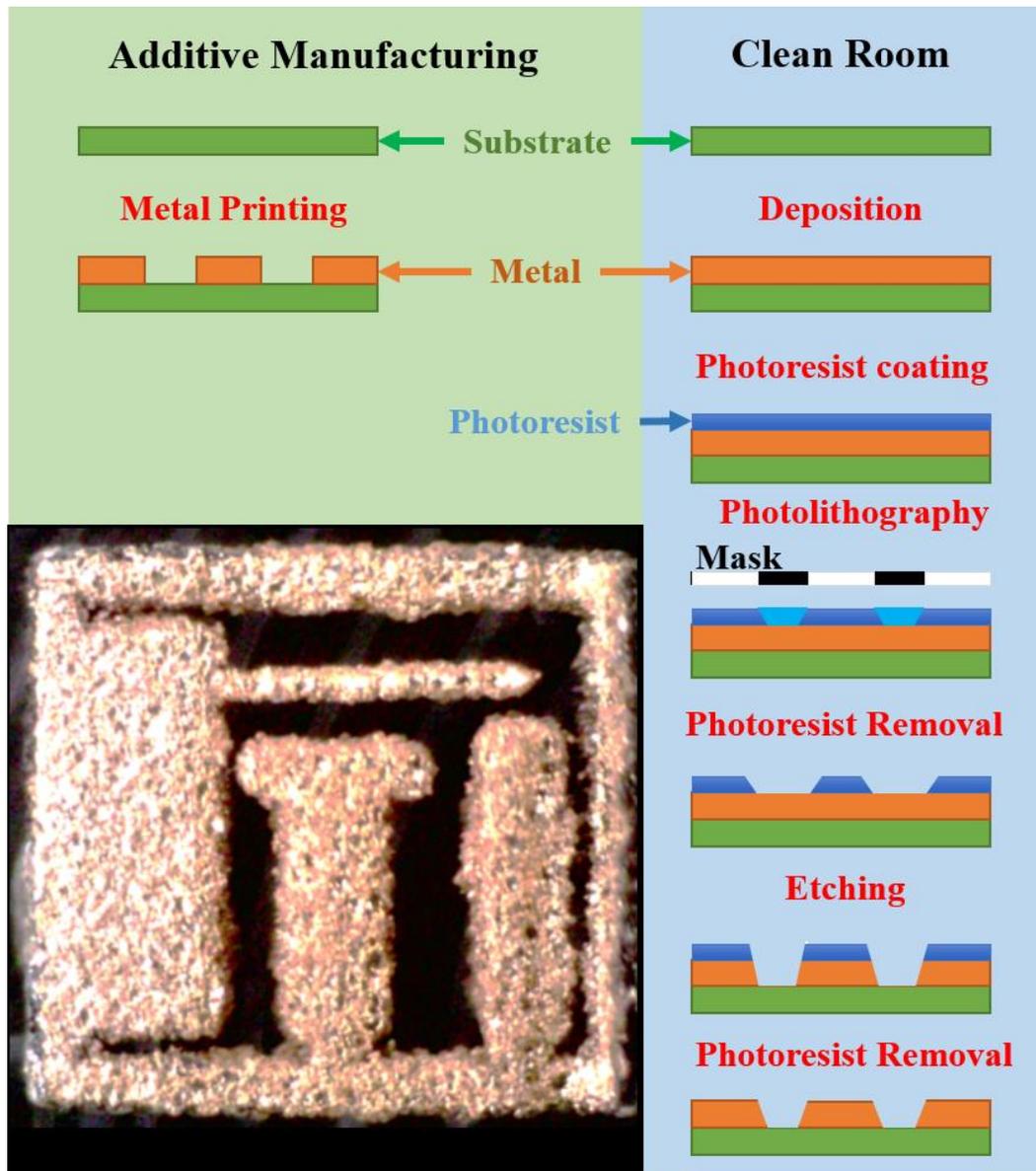


Figure 2.3: Complexity of additive manufacturing vs. conventional clean room process and final product from additive manufacturing (bottom left).

On top of that the machines involved for carrying out the processes are huge and very expensive. However, as can be seen for the additive manufacturing process, only single step of printing the metal parts onto the substrate is required which is straightforward. Also, the release of the devices is not mentioned for both cases but, use of wire Electrical Discharge Machining (EDM) would be easily used for AM whereas wet processes are required for clean room process. Just from the example above one can imagine the various advantages of AM over Conventional clean room process. The following are some of the advantages of AM over clean room process.

2.5.1. Flexibility in design:

As the components are built as per the CAD file in additive manufacturing processes, there is flexibility in geometry, and it makes it easier to create complex geometries which might not be possible with a conventional clean room process [113]. As the requirement might be different for different scenarios, the possibility of customization of the component in additive manufacturing makes it a cheaper alternative to conventional subtractive processes that require the change of masks for different devices [114]–[116]. Compared to expensive silicon substrates used in subtractive processes, the use of various inexpensive and flexible substrates like plastic [117]–[120], paper [121]–[125], glass [126]–[128], fabrics [129]–[132], metals [133]–[136], and more. These features of AM not only reduce the cost but also create flexible devices.

2.5.2. Cost reduction:

From the non-requirement of costly setups to expensive and huge clean room space with a controlled environment, AM has the advantage of lower cost compared to conventional subtractive manufacturing. The limited or reuse of raw materials also plays a major role in cost reduction in AM processes [137], [138]. Conventional subtractive processes are mostly based on a silicon

substrate which is expensive compared to cheaper substrates used for AM [139]. Minimized post-processing steps [140], lower energy usage due to the reduction of high energy-consuming equipment [141], and smaller volume of a controlled environment to be controlled are some of the other advantages of cost reduction for AM compared to conventional clean room processes [142]. Overall effects of all these lead to cost reduction in the additive manufacturing process.

2.5.3. Waste Reduction:

The process of additive manufacturing follows the selective placing of desired material at the ROI whereas the subtractive process starts with the deposition or implantation of bulk material and selective removal of unwanted material from outside of the ROI. During this process, much of the unwanted material is dissolved or removed using wet or dry processes comprising the etching processes [143]. The byproduct obtained from etching in the subtractive process is a compound of the desired material which is washed away and barely used [144], [145]. This causes a huge waste of raw material compared to AM where a very low amount of raw material waste and most of the time can be reused [146]–[148]. Not only are the raw materials wasted in the conventional subtractive process but there are other reagents and chemicals increasing the amount of waste. This is however not the case with additive manufacturing.

2.5.4. Cheaper prototype development:

The initial step of additive manufacturing is the 3D model design of the ultimate product. This has the advantage of the possibility of computer-based simulation of the final product even before the fabrication [149]–[151]. One can simulate the CAD design, make necessary changes to the model, and then fabricate the device to characterize it [152]. As the build time of a small sample

is faster, low-volume and cheaper prototype development in a small time is an advantage of additive manufacturing compared to traditional processes [153].

2.5.5. Smaller setup space:

The cleanrooms generally require a large space for set-up with a lot of equipment from oxidation chambers, several hoods for chemical processing, etching setups, ion implantation systems, deposition setups, packaging setups to sophisticated air conditioning systems, most of the time separate lithography room with the optical system and photoresist coater, and sometimes a separate air shower room. All these huge setups require plenty of space and with it comes their critical management. However, a 3D printer can take up to a maximum of a few thousand cubic meters of space.

2.5.6. Dimensional accuracy:

In an additive manufacturing process, a component is fabricated based on the dimension of the 3D model created on a CAD file. Except for the tolerance and resolution of the printing a 3D printer should be able to impart accurate dimensions to a component. The dimensional errors for various 3D printers have been found to be statistically insignificant in several studies [154]–[156]. Additive manufacturing could be considered superior in dimensional accuracy due to the absence of over and under-etching of desired materials.

2.5.7. Reduced or no use of hazardous chemicals:

In additive manufacturing, the components are directly fabricated on a build plate with or without support structures. They are designed such that their removal is as easy as hand-picking to Wire EDM cutting. During and after the process, the use of harmful chemicals is reduced or

avoided. The raw materials used might have some hazard to health, but they are confined to a small space and direct exposure is reduced using Personal Protective Equipment (PPE). PPEs are also used for clean room processes, but they do produce harmful chemicals from intermediate processes like unused photoresists, dissolved chemicals, acids, and more which require proper disposal considering their impact on the environment [157].

2.6.Challenges in additive manufacturing

Although, additive manufacturing has a huge prospect, it is not spared by the various challenges it faces [158]–[161]. The initial setup cost of a high-end 3D printer is high and also has a larger lead time. 3D printers have also been criticized for their limitation in fabricating large components and the number of raw materials available. The repeatability and consistency of printed parts are questioned by many. The large build time, lower resolution, and lower throughput are also some of the issues with additive manufacturing. The mechanical properties of printed parts are also most of the time altered due to the introduction of microstructures into parts leading to anisotropy. The absence of a proper standard for AM processes has also rendered lower industrial acceptance of the process. However, all these challenges require more research and work and can be overcome by collective approaches.

2.7.Future of additive manufacturing

Additive manufacturing has been considered an emerging technology with a lot of future prospects in various fields [162]–[167]. Developments and research works are ongoing in the fields of aerospace [168]–[170], space applications [171], [172], biomedical devices [173]–[177], bio-implants [178], [179], MEMS devices [60], [180]–[184], electronic devices [185]–[188], heterogeneous integration [189]–[191], and more. Major works are being done in the fields of

micro devices manufacturing for sensors, transducers, electronic devices, and packaging devices in the field of semiconductor industries. If all the challenges faced by present technologies are properly addressed, this technology has been considered to not only be a complement to present semiconductor manufacturing but also a competition to the same.

Chapter 3: Additive Manufacturing Technologies

Although the main focus additive manufacturing technology for this research is the Direct Metal Laser Sintering (DMLS), in this chapter few available 3D printing technologies are discussed in brief leading to the detailed discussion of the DMLS process.

3.1.Fused Deposition Modeling

Fused Deposition Modeling (FDM) works on the principle of melting and extruding a thermoplastic filament through a nozzle [192]. The thermoplastic material is melted and deposited onto the build platform in layers that match the CAD model. It then cools and solidifies. The end result is a sturdy 3D construction. Some of the thermoplastics commonly used as precursors include polyamide (PA), polylactic acid (PLA), acrylonitrile butadiene styrene (ABS), and polycarbonate (PC) [193]. While this method has the advantage of low material cost, the tradeoff is a compromise in both resolution and speed.

The setup for FDM consists of one or multiple nozzles, a build platform, material filaments, a heater, driver wheels for the nozzles, a supporting structure, and a platform motion system. Thermoplastic material is used in the form of thin filament. The filament is directed towards the nozzle, which would be pre-heated employing a heater present at that location. The heater melts the filament and releases it through the nozzle tip into finer molten filament. The molten material is fused and cooled on the surface of fabrication platform forming a 2D layer replicating the CAD model. The platform is lowered, or the nozzle is raised to allow the printing of another 2D layer on top of the previous one. The process is repeated till the final 3D prototype is completely fabricated. This is the most common type of 3D printer used. FDM has been used for the work to create test setups fabrications which will be discussed further in Chapter 5.

3.2.Direct Ink Writing

Direct Ink Writing (DIW) is a versatile technology that utilizes various types of inks, including ceramics, plastics, tissues, hydrogels, and more. [194], [195]. The printing nozzle of DIW is capable of extruding and depositing a highly viscous liquid form of ink onto the surface of fabrication. Various parameters like nozzle size, viscosity of ink, speed of deposition, etc. can be adjusted as per the requirement. In many cases, post-processing procedures such as heating, sintering, UV curing, and drying are necessary for achieving mechanical strength in this process. [196].

The process involves directing the material ink to the heater-nozzle setup where it is melted to a desired viscous molten state. The nozzle then extrudes the material directly onto the fabrication platform as per the CAD model of the desired shape. The controlled deposition of highly viscous molten ink onto the fabrication platform allows it to retain the desired shape. Various materials such as ceramics, plastics, foods, tissues, and hydrogels can be printed using this technology. The one drawback of this process is that the material created requires additional post-fabrication processes to harden it.

3.3.Photocuring

This process involves laying multiple layers of photosensitive liquid polymer resins in a sequential manner. Each layer is then treated with ultraviolet (UV) light of a specific intensity for a set amount of time based on the desired outcome [197]. Stereo lithography apparatus (SLA) and digital light processing (DLP) are two types of photocuring technologies [198]. In an SLA setup, a tank is filled with the liquid resin. This resin forms two dimensional (2D) layers on the platform surface as per the CAD model. Each layer is cured using UV light and the steps are repeated until

the desired 3D structure is formed [199]. DLP technology utilizes an extra digital mirror device to serve as a dynamic mask during exposure. While this technology can create precise structures, the limitation of using a single material for the entire process may be inhibiting its potential.

3.4.Laminated Object Manufacturing

In Laminated Object Manufacturing (LOM), the raw material consists of layers of laminated sheet material. [199]. According to the requirements, layers are cut using lasers or knives and stacked on top of each other. This process involves cutting one layer and stacking a new layer on top of the previous layer repeatedly until the desired structure is achieved. The layered sheets are bonded together through the application of heat and pressure by a roller. The sheet of the desired material is placed on the build plate of the printer. The sheet is then cut into desired 2D layer, and another sheet is added on top of it, ultimately forming the designed 3D structure. The scanner system uses the sliced 3D CAD file to instruct the laser to make cuts on the sheet metal in order to obtain the required shape of the sheet. Another sheet metal is placed on top of the first one, cut to the desired shape then the hot rod rolls over to create adhesion between layers.

3.5.Selective Laser Sintering (SLS) and Selective Laser Melting (SLM)

SLS uses powdered metals, metal alloys, plastics, ceramics, polymers, and waxes to fabricate a device [200]. In this method, the desired powdered material is laid on the fabrication surface. 2D layers of the desired pattern are melted and fused based on the CAD model. The fabrication surface is lowered, and another layer of powdered material is laid on top of the first layer, melted, and fused to the first layer [201]. The process is repeated until the final 3D structure is formed. In SLS the powder and the layers are consolidated using thermal energy of the focused laser beam [202] or by polymeric binding [203]. The binding in SLS might be solid state, chemically induced, partially melted, or fully melted [204].

A typical SLS consists of parts like scanning system, high power laser source, build chamber with build plate, powder bed with powdered material, a re-coater blade, setups for creating inert chamber for the build chamber and powder bed, and heating and cooling setups. The powdered material from the powder bed is moved to the build plate with the help of the re-coater blade depositing a thin (based on powder size) layer of powder material onto the build plate. The scanner system controls and instructs the laser to fuse together a desired 2D shape which is also fused to the build plate. The build plate then descends with the help of a fabrication piston to make room for the second layer. This second layer is then created similarly to the first. This process is repeated until the desired 3D structure with fused layers is built which is also fused to the build plate. The SLM works on similar principle but varies based on the consolidation process of the powder and layers [204]. The latter is the derivation of SLS where the material is completely melted. Based on whether the particles are bonded together directly or using an intermediate material/step to form the solid, SLS can be Direct SLS or Indirect SLS.

3.5.1. SLS types based on the bonding processes of materials.

Based on how the powdered raw materials are consolidated among each other and among different layers in an SLS process, there are two different approaches to this additive manufacturing technology. They are indirect SLS and direct SLS approaches and will be discussed further.

3.5.1.1. Indirect SLS approach

This process employs the use of sacrificial polymer binder along with the desired powdered raw material [205]. The raw material might be ceramic or metallic powder which are coated with a polymer and mixed with polymer binders. The laser energy provides enough temperature to develop bonds between polymer particles. These bonds cause the raw material powder to be held

on place creating a solid structure without any actual bonds between them. This overall solid structure consisting of unbound and loose raw material powder held together by polymeric bonding is called a green part [205]–[207]. As the raw material particles are loosely held together and not actually bound, the solid structure is fragile and porous. The green part is heated in a furnace for post-processing which not only binds the raw material particles together but also melts away the polymer binder used in the first place creating the final solid product [208]. A process known as infiltration might also be used where a low melting powder metal infills the gaps between different particles which is then melted to create a final dense solid [209]. However, this is a very complicated process lacking dimensional accuracy, time consuming, requiring post processing, and producing a composite product.

3.5.1.2. Direct SLS approach

This approach does not use polymeric bonding material rather, uses focused high-power laser beam to consolidate materials and layers [210]–[212]. Based on the temperature and bonding types Direct SLS might employ solid-state sintering, liquid-state sintering, or selective laser melting [213].

Solid-State Sintering

As a result of laser energy, particles' surface energy decreases due to higher temperature, creating a solid bond between them. The temperature of bonding lies somewhere between the half of the melting temperature to the melting temperature of the material. In order to increase the density of the powder and increase the contact between different particles, it is necessary to pack the powder tightly before bonding. Despite packaging, the end product would be porous compared to the products obtained from Liquid-Phase Sintering and Selective Laser Melting. This process is

also inferior to others due to the large amount of time it requires and the heavy post-processing needs.

Liquid-Phase Sintering

This process employs a binder material to sinter a main structural material. Binder has a lower melting point compared to the main material. The incident laser is set to increase the temperature to the melting point of binder and melts it. The molten binder then increases the solubility of un-melted main material to it via its capillary action. As powdered main material particles are bound by the binder, one can expect the spaces between powder particles are filled by the binder creating a very dense end product. Although, this process produces dense parts with good strength, the use of different material as binder will result into a composite metal instead of the material of interest.

Selective Laser Melting

Selective Laser Melting (SLM) is considered to be the superior of the other two methods. This process employs a complete selective melting and fusing of particles together without using any binder compared to Liquid-Phase as well as a dense part compared Solid-State Sintering processes. This is one of the processes widely used for metal additive manufacturing. Although SLM requires high laser power compared to the other two, it does produce a part that requires lesser post-processing steps, dense and rigid, and pure. Compared to other AM technology, this is a faster process as the laser beam takes very little to melt and fuse particles.

There are various other types of 3D printers like Photopolymer Jetting (Polyjet), Binder Jetting (3DP), Electron Beam Melting (EBM), Nanoparticle Jetting (NPJ) to name some with their own advantages in various field but will not be discussed here.

3.6. Direct Laser Metal Sintering

Direct Metal Laser Sintering (DMLS) will be the major Additive Manufacturing technology to be explored in this research. DMLS is a powder bed system of metal additive manufacturing where the metal powder is spread across a build area, exposed to laser energy to sinter the powder to desired shape and repeated to create a solid 3D component [214]. DMLS is an advanced SLS process in which raw metal powder are directly bound together using a laser beam to produce high density metal component [215]. The major difference between metal SLM and DMLS is that, in the former the metal powder is completely melted and fused together while in the later the metal powder is heated to a temperature below melting point to allow physical and chemical reactions like partial melting and diffusion to cause metal powder particle to fuse together [202].

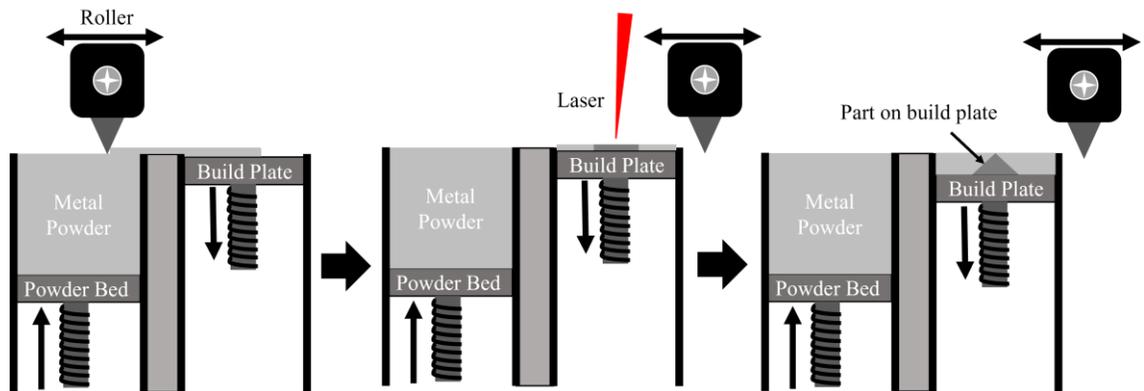


Figure 3.1: DMLS process flow; transfer of metal powder layer from powder bed to build plate (left), exposure and sintering of desired section of layer (middle), and final part on build plate after several left and middle steps (right).

The basic working principle of a DMLS system is the successive feeding, deposition, and sintering of metallic powder to form a solid 3D part. High-energy laser sources are used to deposit metallic layers on top of each other to build a final functional part. The process is carried out in an

inert environment to prevent the oxidation of the powder. Fig. 3.1., illustrates a basic working principle of a DMLS process. The powder from the powder bed is transported and raked upon the build plate by a roller or a re-coater blade. High energy laser sinters the first layer controlled, as per the sliced CAD file fusing only the desired region and leaving the rest of the powder un-sintered. Some of the un-sintered powder is deposited into the waste bin which can be filtered and reused later while some remain near the build layer and sometimes act as a support for overhangs in the print part. The roller or re-coater blade then moves back to the previous location, the powder bed is raised by a layer, while the build plate is lowered by the same amount. The roller then transports and deposits a new layer of fresh powder onto the first layer. The laser beam again using the instructions from the sliced CAD file fuses together a new layer on top of the previous one. The same process repeats in a loop until the whole structure as per the CAD file is sintered to form a solid 3D part.

Chapter 4: Electrostatic switch as a MEMS Device

In this chapter, the possibility of using microscale DMLS is studied with the design, simulation, fabrication, and characterization of a MEMS electrostatic switch. A journal paper titled “Dielectric Transfer Process for 3D Printed Metal Microsystems” has already been published in the “Journal of Microelectromechanical Systems”. One more paper titled “Additive Batch Microfabrication of 3D Metal Electrostatic Switches Towards 3D Printed Metal MEMS’ has been published by “Hilton Head 2022 Workshop”.

This work deals with the design, simulation, batch microfabrication, dielectric transfer, and characterization of 3D printed metal electrostatic micro switch. Micro Laser Sintering (MLS), a precision form of DMLS for microstructure fabrication, was employed to batch fabricate the switches. This work marks the initial milestone toward the direct fabrication of metal microsystems via additive manufacturing technology which might open up new doors toward the low-cost fabrication of prototypes and low-volume systems which was otherwise fabricated using expensive conventional cleanroom processes on a silicon substrate using processes like surface micromachining and bulk micromachining. This work presents the additive micro-fabrication of a single-piece metal system comprising electrodes with sacrificial metal frames bypassing the conventional cleanroom processes.

4.1.Literature Survey

MEMS devices have been considered to be an integral part of today’s electronic devices [216]–[221]. These devices are however mostly fabricated following conventional cleanroom processes on a silicon substrate using methods like surface micromachining and bulk micromachining [222]–[232]. High-end and expensive processes like deposition, lithography, etching and a lot of other physical and chemical processes are used to fabricate MEMS devices

[233]. These microfabricated MEMS devices will then be integrated into electronic systems as sensors, transducers, RF devices, etc. The wide range of applications of MEMS components has led researchers to focus on lower costs, faster processing speeds, and streamlined production processes. Additive manufacturing, a process that can directly fabricate components from design files fits all the features mentioned [234]. Initially designed for purely mechanical components, 3D printing, or additive manufacturing, has great potential for the fabrication of electronics, transducers [62], and sensors [235], [236]. The use of additive manufacturing techniques also permits the fabrication of metal devices, such as electrostatic switches, whose plasticity and conductivity are superior compared to their silicon counterparts fabricated by conventional cleanroom processes [62]. A newly developed metal 3D printing procedure, micro laser sintering (MLS), has made it possible to fabricate parts with a resolution of $15\mu\text{m}$ [237] out of metal powder [238]. MLS has also been found to have superior dimensional consistency and improved surface roughness over other additive tools [239]. Considering all these features, many researchers have dived into the study of metal microsystems fabrication, presenting a broader area of metal MEMS exploring the mechanical and electrical superiority of these metal parts compared to Silicon, using MLS [62], [240]–[246]. However, most of the works are dedicated to the review of MLS or the use of MLS for some molds. Based on the literature review done up to the writing of this dissertation, we can claim that this work is the first of its kind that uses the MLS process to microfabricate complete two/three electrodes 3D MEMS devices in the form of electrostatic switches.

The devices fabricated by this process are electrically non-isolated one-piece metal components. The process of MLS also fabricates the components as a single metal piece fused to the build plate. Therefore, there is a need for post-processing to release the device from the build plate, transfer the device onto a dielectric substrate, isolate the electrodes, and create proper electrical connections to test the device. The release of fabricated devices is straightforward with technologies like grinding and wire EDM (used in this work). However, this work additionally

presents the aligned and unconstrained transfer of the metal system onto a substrate to electrically isolate the electrodes for testing. This work takes cues from a similar transfer process demonstrated by researchers in the field of MEMS devices [247].

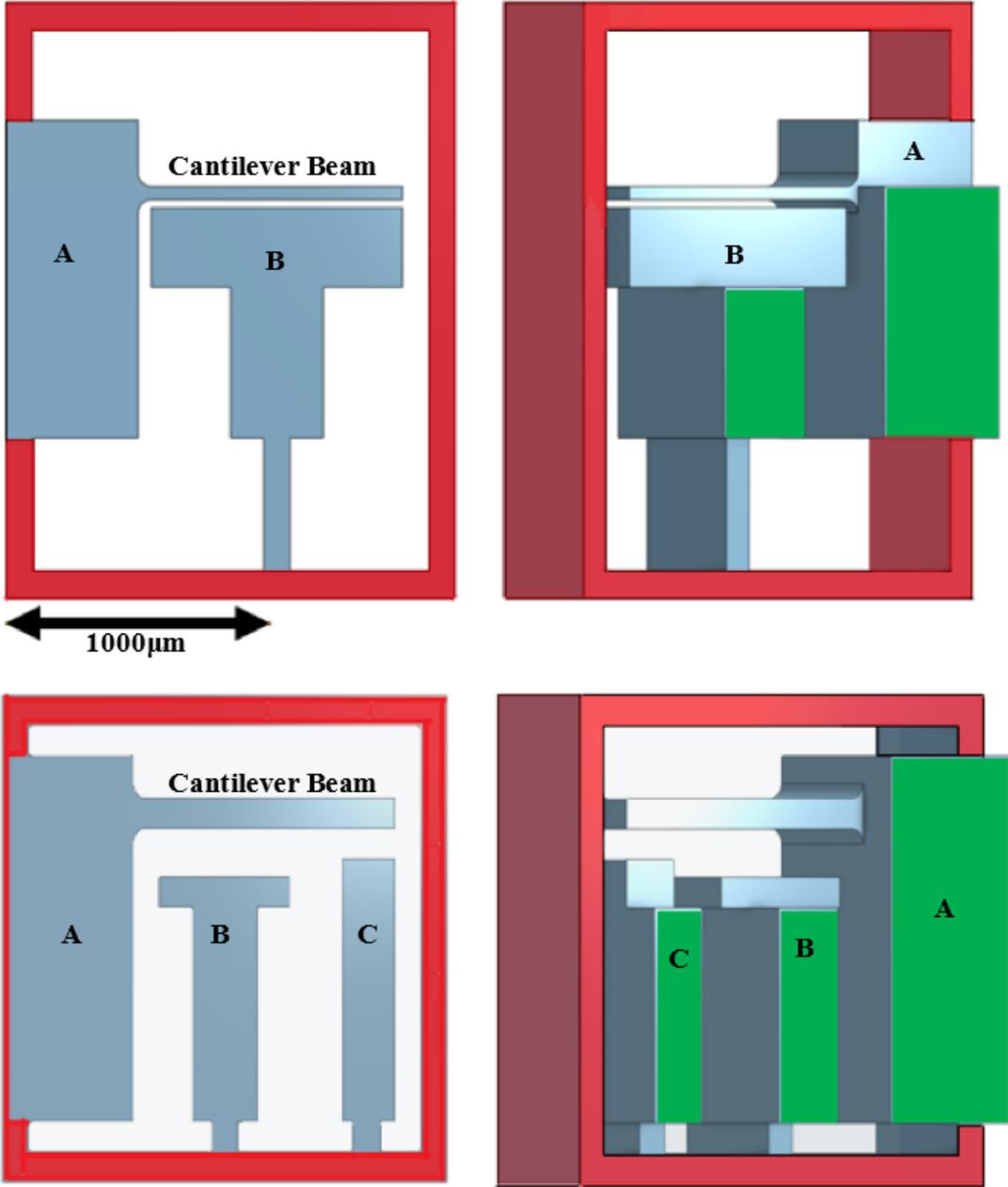


Figure 1.1: CAD Designs of the Microswitch: Optimized design with two electrodes (A and B) front view (top left) with sacrificial metal support in red, isometric view (top right) with attachment surfaces to the substrate in green, previous three electrodes (A, B, and C) design (bottom).

This dielectric transfer demonstrated here is a simple, inexpensive, and easily performed process compared to the likes of the focused ion beam (FBI) with complex and vibratory steps [248], and other processes like wedging method [249], polyvinyl alcohol (PVA) method [250], and Evalcrite method [251] all of which rely on wet chemical steps later-on requiring post-processing steps like a supercritical release. The transfer process described here is based on viscoelastic stamps which do not require wet chemistry, avoiding contamination of the freestanding structure as it will be free from capillary forces.

4.2.Design

Two different designs of the switches were analyzed in this work. The CAD design of the first switch with its top view (left) and 3D bottom view (right) is shown in the bottom half of Fig. 4.1, with a scale. As demonstrated in the figure, the single-piece MEMS switch has 3 electrodes (marked A, B, and C), a freely suspended cantilever beam as a part of electrode A, and sacrificial metal support (in red color) holding all the components together. The bottom of the electrodes for both switches are extended by 200 microns compared to the bottom of the cantilever beam as shown in Fig. 4.1., (top right and bottom right) with the points of contact to the substrate marked in green. This setup allows the cantilever beam to freely suspend with a clearance of 200 microns from the surface of the substrate.

The CAD design of the latest modified switch with its top view (right) and the 3D bottom view (right) is shown in the top half of Fig. 4.1. In this modified design, electrodes B and C are merged into one electrode (named B), the thickness of cantilever beam (a) is reduced compared to the first design, and the gap (X) between the cantilever beam and electrode B is also reduced, and the sacrificial support is extended (to allow easy severing later). The detailed reason for all the changes will be explained at the end of this section.

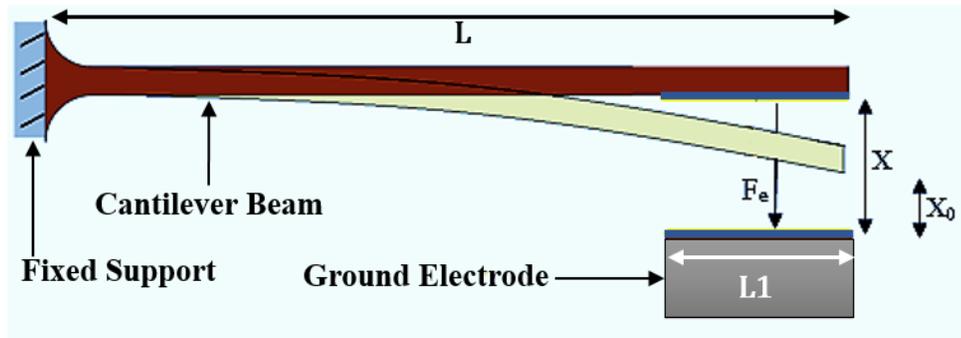


Figure 4.2: Illustration of electrostatic actuation of cantilever beam with electrostatic force (F_e) involved in the actuation due to the application of voltage. The initial gap (X) between the beam and the ground electrode changes to X_0 after voltage application.

Fig. 4.2., illustrates the working of an electrostatic cantilever beam with the normal (brown) and actuated (pale) states of the beam. The area of the application of electrostatic forces (highlighted blue) is 'A'. 'X' is the initial gap between cantilever beam and ground electrode (grey) while 'X₀' is the gap between the same two components after the application of an electrostatic force 'F_e' due to a voltage (V) applied on the positive electrode [248]–[250].

When the positive electrode (electrode A for our switches) with the cantilever beam is connected to a positive supply voltage and the ground electrode (electrode C for the first and B for the second switch) is grounded, the free-standing cantilever beam experience an electrostatic force due to applied voltage. This causes it to actuate towards the ground electrode due to the electrostatic force of attraction between unlike charges. This changes the gap between the tip of the cantilever beam and ground electrode to decrease compared to its initial gap 'X'. If 'X₀' is the new gap between the cantilever beam and the ground electrode after actuation and at equilibrium, the following equations will be obtained from the equilibrium analysis [251]–[253]. Equation 4.1 and 4.2 gives the values of spring constant (k_m) and pull-in voltage (V_{pullin}) respectively.

$$k_m = \frac{Ea^3b}{4L^3}$$

Equation 4.1

$$V_{\text{pullin}} = \sqrt{\frac{8k_m X^3}{27\epsilon_0 A}}$$

Equation 4.2

Where, ‘E’ Young’s Modulus of the material. ‘a’, and ‘b’ are the thickness and width of the cantilever beam. ‘L’ is the free length of the beam. The permittivity of the vacuum is given by ϵ_0 . Substituting (1) to (2), we get the final equation as:

$$V_{\text{pullin}} = \sqrt{\frac{2Ea^3 b X^3}{27\epsilon_0 AL^3}}$$

Equation 4.3

From equation 4.3 and the dimensions of the first switch, the pull-in voltage comes out to be 21 to 15 kVolts for a 100 microns thick cantilever beam with gaps of 100 to 40 microns fabricated using the previous MLS printer (DMP50GP). This creates a lot of problems to operate the switch as such an actuation voltage is impractical, not possible in a normal lab setting, and also causes the dielectric breakdown of air between the beam and the ground electrode as per Paschen’s Law [254]–[256]. Hence, the second switch was redesigned considering the various factors that affect the pull-in voltage and also the improved aspect ratio of the presently enhanced MLS printer (DMP64).

From equation 4.4 it becomes clear that V_{pullin} depends on various constants and dimensions. Young’s Modulus (E) is a constant for a given material and the other quantities, the V_{pullin} depends on are given below:

$$V_{\text{pullin}} \propto \frac{Ea^{3/2} X^{3/2} \sqrt{b}}{L^{3/2} \sqrt{A}}$$

Equation 4.4

V_{pullin} depends on the thickness of the cantilever beam 'a'. The present value can be reduced to $40\mu\text{m}$ based on the resolution of DMP64. However, the first switch cantilever beam has a thickness of $100\mu\text{m}$, which is already very thin. Decreasing this value to less than $40\mu\text{m}$, might not be printed properly by the MLS printer.

V_{pullin} depends on the square root of the width of the beam 'b'. The first switch has a beam width of 0.6 mm it can be reduced to half that value without violating the feature size. This will also decrease the area of the electrostatically separated plates. However, the effect of change in the area can be altered in the next point.

V_{pullin} depends on the product of beam length 'L' and the square root of area 'A'. They are interdependent as a change of one causes the change of another. A decrease of 'b' to half has already caused the decrease in the area but it should be increased for the desired performance. To achieve that, we have considered the service of the unused electrode B in Fig. 4.1. The unused electrode can be fused with the ground electrode to increase the area of the electrostatically separated plates. The fusion of electrodes B and C results in the increase of area by 0.450 mm^2 . This has led to the new design as illustrated by the top left (top view) and top right (3D bottom view) of Fig 4.1. The new switch is proposed to reduce the actuation voltage by a huge factor and will be discussed further in the next section. The new design, as shown in the top two sections of Fig. 4.1., has two electrodes: electrode A (which has the cantilever beam) and electrode B. Again, as seen in the top right image of Fig 4.1, the bottom of the electrodes A and B are extended by 200 microns compared to the bottom of the cantilever beam. The contact points to the substrate are marked in green. This setup again allows the cantilever beam to freely suspend with a clearance of 200 microns from the surface of the substrate. Electrode A acts as a positive electrode while electrode B acts as a ground electrode.

Table 4.1: Calculated and Simulated Pull-in Voltages values for switches with different gaps.

Gap in μm	Pull-in Voltage (in kVolts) for first switch (100 μm Beam width) Bronze		Pull-in Voltage (in kVolts) for new switch (40 μm Beam width) 17 -4PH	
	Calculated	Simulated	Calculated	Simulated
100	39.97	40.65	14.69	14.87
60	18.56	18.90	6.83	6.91
50	14.13	14.26	5.19	5.24
40	10.11	10.31	3.72	3.77
30	6.57	6.76	2.41	2.47
20	3.57	3.66	1.31	1.34
15	2.32	2.37	0.853	0.870
10	1.26	1.29	0.465	0.473
5	0.447	0.458	0.164	0.167

4.3.Simulation

The simulation was carried out on Ansys 2021 R1. The model was designed as per Fig. 4.1. Upon application of voltage to the electrodes it was possible to visualize actuation at different magnitudes of the voltage. Table 4.1 displays the pull-in voltage values obtained from the simulation for the present switch and the newer one with respect to the calculated values. As the

new switches were to be fabricated using 17-4PH Stainless steel, the simulation and Table 4.1 also take into account the change in Young's Modulus.

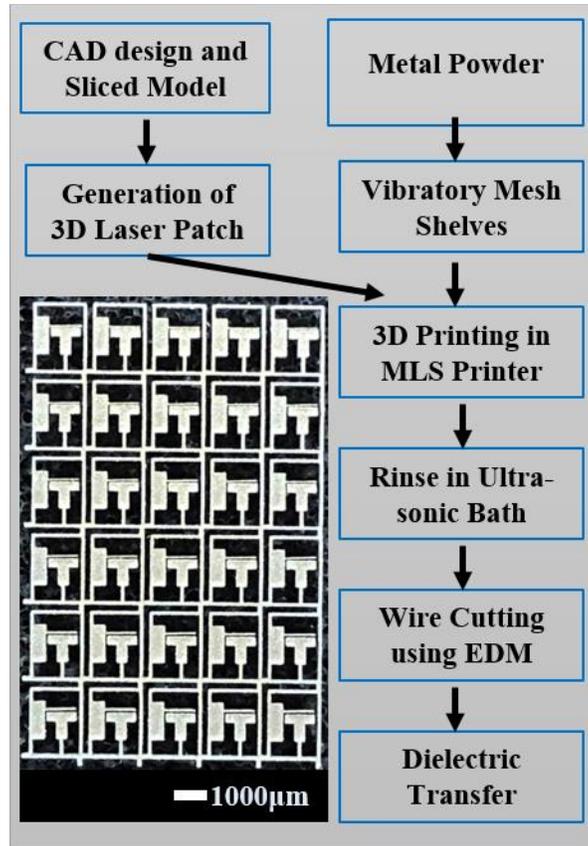


Figure 4.3: Graphical illustration of MLS Process flow with a released array of microswitches in the inset.

4.4.Fabrication

The first switch was batch microfabricated using a DMP50GP MLS 3D printer (from 3D Microprint GmbH, Germany). This printer used $<10\mu\text{m}$ metal powder as raw material and had high-precision optics both of which enabled high aspect ratio and fine component features. Each layer was $5\mu\text{m}$ thick and sintered using a laser with a spot size of $30\mu\text{m}$ at 40W CW power in an argon environment. The powder used was Bronze (90% Cu – 10%Sn) powder (D90 $6\mu\text{m}$) which was procured from Dongguan Hyper Powder Technology Co. Ltd.

The new switch was also batch microfabricated but using a newer version DMP64 MLS 3D printer (from 3D Microprint GmbH, Germany). The printer has a superior optics system leading to improved aspect ratio and resolution of the built part. This printer was employed to investigate the minimum possible feature size for the printed part as it has a resolution of $<15\mu\text{m}$. 17-4PH Stainless Steel powder was used as the raw material.

The fabrication process is illustrated in Fig. 4.3. At first, the device is designed and drafted in CAD software. The 3D model thus created is then processed using a laser manufacturing plan using software like AutoFab, Renishaw plc., and Netfabb to generate a laser path for the printer. Metal powder is filtered successively using vibratory mesh sieves of different sizes in an argon environment to remove contaminants. Filtered metal powder is then fed to the 3D printer, and the manufacturing plan is loaded. The system is then activated to initiate fabrication onto a pre-loaded and pre-heated stainless steel build plate. The first layer of $5\mu\text{m}$ thick powder is spread across the build plate by a recoater, which then gets melted and fused via laser beam as per the path generated by the manufacturing plan software. The first layer also gets fused to the hot build plate due to the laser energy. The build plate is then lowered by $5\mu\text{m}$, the powder bed is raised by the same height, and a new layer of metal powder is spread across by the recoater. The laser again acts on the new layer as per the design and fuses together the powder layer and also the new layer to the first layer. These processes repeat until the final 3D solid structure is built. Once the fabrication is completed, the build plate starts cooling down and once it reaches the room temperature, the devices fused onto the build plate can be removed from the printer. Most of the unused powder can be brushed or vacuumed off and filtered for future reuse. The build plate with the part is then rinsed in an ultrasonic bath for 30 minutes to remove any powder particles remaining. After this, wire EDM is employed to release devices from the build plate. The full process flow is illustrated in Fig. 4.3., with the released batch fabricated switches in the inset. The switches are then individually, separated to be transferred onto a dielectric substrate.

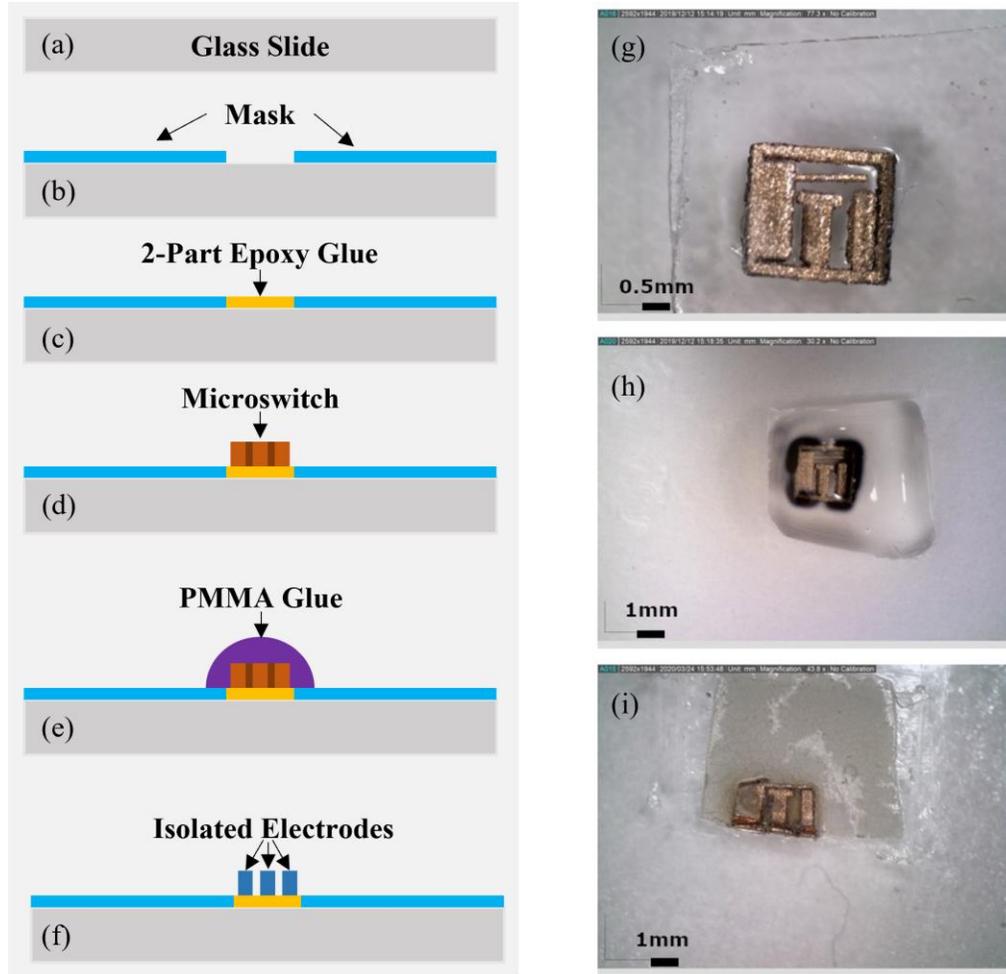


Figure 4.4: Dielectric Transfer of microswitch onto the substrate (left) involving scotch tape mask application (b) in clean glass slide (a), application of two-part epoxy into the unmasked area (c) and placement of microswitch (d), mechanical stabilization of the switch with PMMA glue (e) to remove sacrificial metal support to electrically isolate electrodes (f), different stages of the transfer of switch illustrated by cartoons in (d), (e), and (f) respectively demonstrated by (g), (h) and (i).

4.5. Dielectric Transfer

In this work, a simple, inexpensive, and easily performed dielectric transfer of each individual switch is detailed. The switches are small in size, and the electrodes are held together in place by the sacrificial metal frame. In other words, the switches are not electrically isolated

and is not ready for further connections. Hence, this work proposes the transfer of one-piece switches onto a dielectric substrate, electrical isolation of the electrodes, and final realization of a MEMS device. This process could also be used for other metal printed microsystem isolation. The process illustration (left) and the intermediate stages of switches (right) are shown in is shown in Fig. 4.4.

The first step would be the cleaning of the substrate (here, a soda-lime glass slide) and the MEMS device, which will be repeated after each and every step. The cleaning was carried out using isopropyl alcohol and water and dried using lab-grade cleaning paper. A 50 μ m thick polyamide tape is applied on the glass surface and a cut a little larger than the bottom area of the device was made onto it creating a mask as shown in the second step of the illustration. 2-part epoxy is then carefully applied to the opening and properly leveled to a 50 μ m thick layer using a doctor blade with polyamide tape as a reference which is shown in the third step of the illustration. Thereafter, the clean MEMS switches are placed anchor down as illustrated in step 4 and shown in Fig. 4.4., (top right). As the cantilever beam is designed to be located 50 μ m higher than the base of the switch, it will remain free-standing while the rest of the switch will be attached to the substrate by the epoxy. The setup is then left to cure in ambient condition for 24 hours.

The next step would be to cut off the sacrificial metal support frame for electric isolation. However, as the switches are very small, extra mechanical support is required so that the electrodes and beam do not move out of position during the isolation process. For this, polymethyl methacrylate (PMMA) glue is used to encapsulate the whole switch (shown in the 5th step and middle right in Fig. 4.4.,) and let cure for 10-12 hours again in ambient conditions resulting in mechanical support for the device. This step is optional depending on the microsystem to be transferred and the use of PMMA glue because of its solubility with easily available acetone. In the next step, the sacrificial metal support frame is carefully severed and the whole setup is drooped carefully into an acetone bath to dissolve away the PMMA glue. This step will not only dissolve

the glue but also clean away any debris left on the device while cutting off the sacrificial metal frame. The final product will be clean and electrically isolated electrodes on a dielectric substrate attached with epoxy glue (shown in the last step of the illustration and bottom right of Fig. 4.4.). Although the epoxy glue does not dissolve in acetone but is rendered soft, hence it is best practice to let the final setup cure for 10-12 hours before making electrical connections. Further cleaning with water and isopropyl alcohol could be done after this step. This process will be useful in affixing similar microsystems for electrical isolation. After the appropriate time lead wires could be connected to each electrode using conductive glue and soldering produces heat that can burn the epoxy glue holding the electrodes to the substrate.

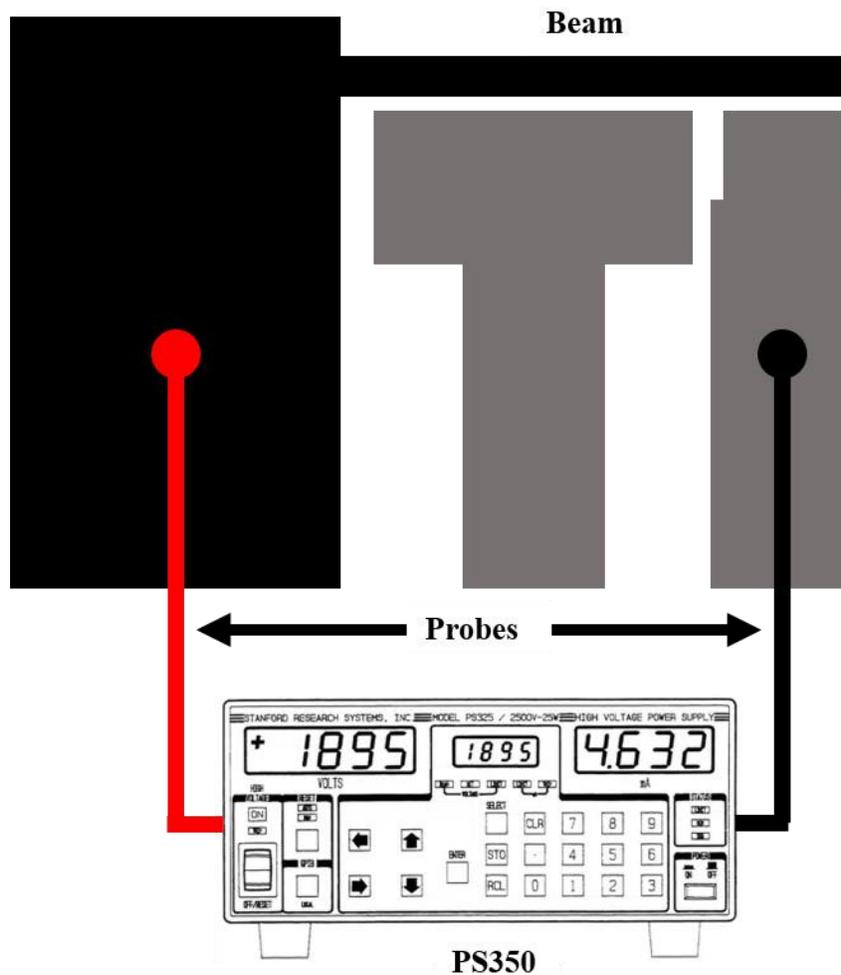


Figure 4.5: Test setup for the electrostatic characterization of the MEMS Switch.

4.6.Characterization and Results

The MEMS switches transferred onto the substrates were probed electrically on a Micromanipulator probe station and demonstrated by Fig. 4.5. The electrode with cantilever beam (positive electrode) was connected to the positive terminal of the power supply and the ground electrode was connected to the negative supply. Multiple devices were tested using a high voltage power supply (PS350, Stanford Research). However, as the gaps were bigger such that dielectric breakdown occurred before the pull-in voltage was reached. This, however, demonstrated the electrical isolation of the components was achieved. This was verified as per the occurrence if breakdown voltages almost matched the expected based on the measured dimensions and Paschen's law. Thus, the experimental setup used to determine the pull-in voltage led to an arc formation between the isolated positive and ground electrodes before the pull-in was reached.

This breakdown is explained by Paschen's law, which is a mathematical expression for the relationship between the breakdown voltage between the electrodes and the product of pressure and the gap between them [254]. The switches built to this date have a minimum gap of 10 μ m, implying that the breakdown calculations will not deviate from Paschen's law [255]. Equations 4.5 and 4.6 will give the breakdown voltages (V_{BD}), where A and B are constant, P is the pressure, X_0 is the initial gap between the cantilever beam and the fixed ground electrode, γ is the secondary ionization coefficient, and k is obtained by Townsend equation 4.6 and the calculation is tabulated in Table 4.2 if the medium is air, the values of A and B are also given by Table 4.2. Fig. 4.6., gives the simulated pull-in voltage values of the first and second switches with respect to gap and corresponding breakdown voltages.

$$V_{BD} = \frac{B * PX_0}{(\ln(PX_0) + k)}$$

Equation 4.5

$$k = \ln \left[\frac{A}{\ln \left(1 + \frac{1}{\gamma} \right)} \right]$$

Equation 4.6

Table 4.2: Values of A, B (in air) and k for different products of P and X0 [206].

Gap Medium	PX_0 (kPa-cm)	k	A (ionization/kPa-cm)	B (V/kPa-cm)
Air	0.0133-0.2	$2.0583 \times (PX_0)^{-0.1724}$	112.50	2737.50
	0.2-100	$3.5134 \times (PX_0)^{-0.0599}$		
	100-1400	4.6295		

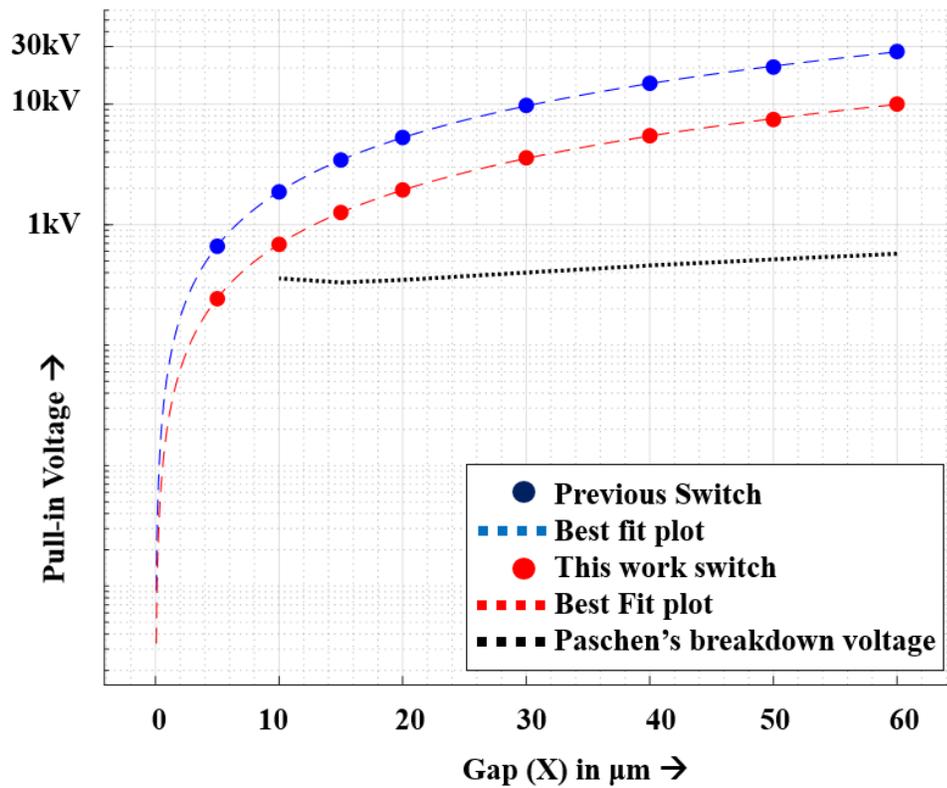


Figure 4.6: Pull-in voltage vs gap and Paschen's breakdown voltages for the gaps for the MEMS switches in this study.

Chapter 5: System-in-Package with Embedded Thermal Management

In this chapter, microfabricated packages featuring microfluidic pin-fin and microchannel for thermal management of semiconductor devices are presented. A presentation on "Additive Microfabrication of System in Package for Heterogeneous Integration with Semiconductor Dies" was given at the Electronic Material Conference (EMC) 2022 in Columbus, OH. A full journal paper with material characteristics has been published in the Journal of Electronic Materials. A paper titled "Metal Additive Microfabrication for Integrated Thermal Management in Power Applications" has been published by "Power MEMS 2022" in Salt Lake City, UT. Another paper titled "Metal Additively Microfabricated SiPs with Embedded Microfluidic Cooling for Heterogeneous Integration with SoCs" has also been published by "2023 Electronic Components and Technology Conference" in Orlando, Florida.

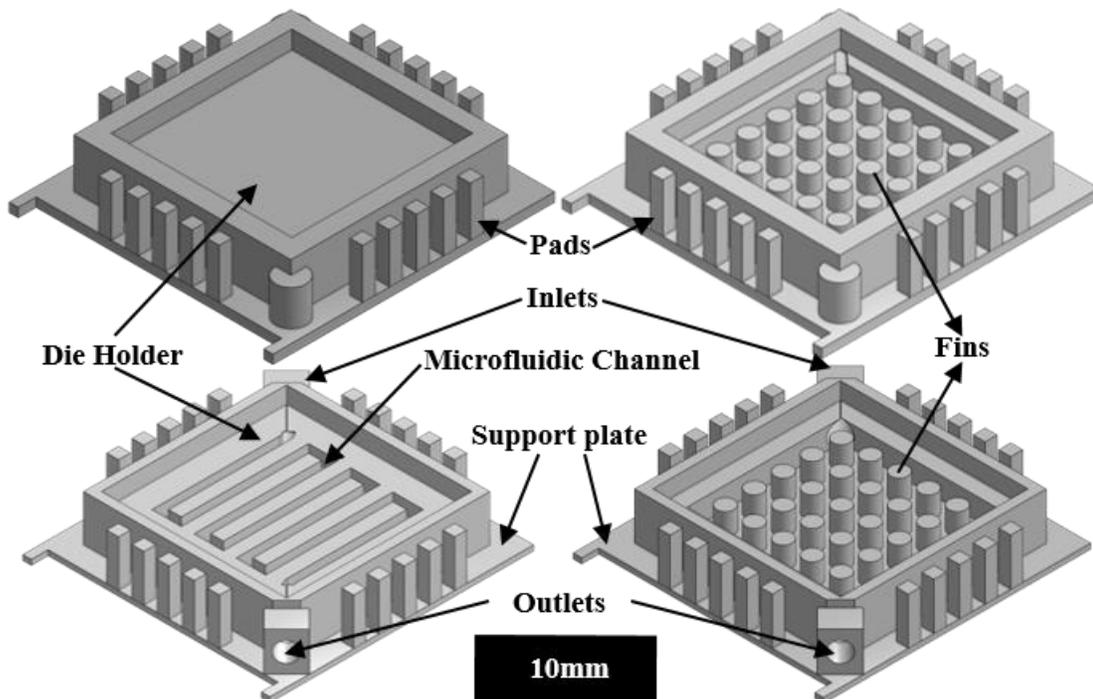


Figure 5.1: CAD Designs of packaging devices (top left: original package, top right: Package with fins, bottom left: package with microchannel, and bottom right: fins with inlet and outlets [250])

This work study investigates the use of metal additive microfabrication of system in package (SiP) with embedded heat sinks for thermal management and leadframe with multiple pads for QFN packaging. This will allow the heterogeneous integration of SiP and System-on-Chip (SoC). The work also opens up doors to the new fabrication and integration of metal microsystems using DMLS to be used as complementing processes to semiconductor manufacturing and packaging. The SiPs were fabricated using 316L stainless steel powder as a raw material and employing a relatively less expensive DMLS system. The affordability of metal additive manufacturing systems is expected to drive research on their potential for use in heterogeneous integration within the semiconductor industry.

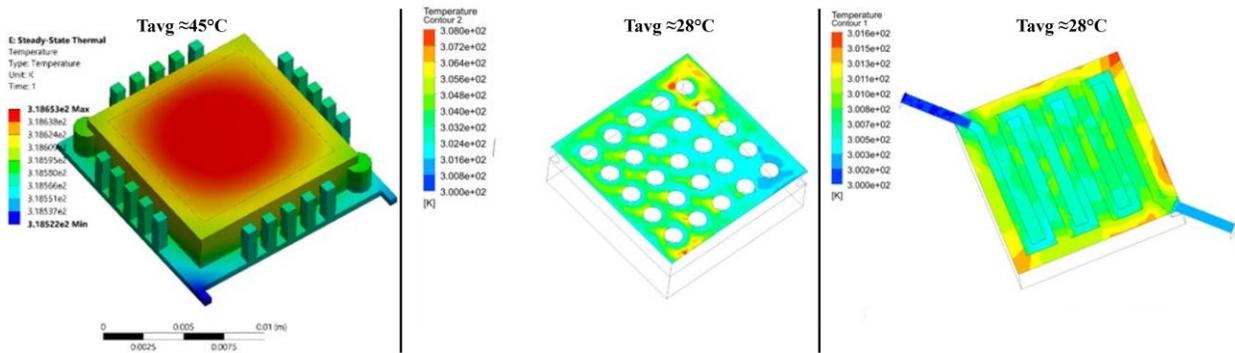


Figure 5.2: ANSYS Thermo-Electric Simulation for conventional package (left), Computational Fluid Dynamics (CFD) simulation for package with micro-pin fins (middle) and the one with serpentine microchannel (right) with water flow where microfluidic water flow decreased the average surface temperature to around 28°C from around 45°C for the conventional package.

5.1.Literature Survey

The semiconductor industry has addressed the need for high-performance electronic devices to process increasing data [1], [2] by adding more miniaturized components onto a single chip [3], [4]. In the same way, wide-bandgap devices have been utilized to enhance the power efficiency of power electronics [7], [8]. Both of these trends have been increasing the power

density of the chip, leading to the localized hotspots generation in the channel of the chip [11], [12], [14], [15], [257]. The Heterogeneous Integration Roadmap has predicted that the hotspot power density of chips will rise to 900 W/cm^2 by the end of 2023 and has also provided the cooling regimes for the different heat fluxes of the hotspots [16]. Today's semiconductor industry requires heterogeneous integration for System-on-Chip with SiP, including embedded thermal management systems. The 2012 International Technology Roadmap for Semiconductors (ITRS) stressed the significance of integrating system-on-chip (SoC) and system-in-package (SiP) [258] and the Heterogeneous Integration Roadmap (HIR) seconds ITRS [16]. Due to a lack of embedded thermal management, current heterogeneous integration is only feasible for low-power dies.

Individual high-power chips typically require large heat sinks and fans for thermal management [259]. These Conventional cooling systems/heat sinks for chips include a conductive interface, heat exchangers for quicker thermal energy transport, and thermal energy-releasing systems such as high-speed fans. This can be termed as system-level thermal management. Most devices, from Raspberry Pi to computers and vehicle parts, use this level of thermal management that employs forced air cooling for heat dissipation. Thermal management systems at the system-level are commercially successful due to their established fabrication methods and lower cost. However, as most heat transport occurs by conduction, except for the final stage with several interfaces in this level. This results in higher contact thermal resistance, decreasing thermal management efficacy [260]. Their large size also makes them sub-optimal. Cooling systems can be microfabricated onto the back of semiconductor dies, allowing for die-level integration with electronic components on the front, as demonstrated in literature [33], [55], [56], [261]–[263]. Microchannel or Pin-fin heat sinks have been created on the back side of the die to cool down hotspots created at the front of it, and this could be termed die-level thermal management. However, integrating at this level adds complexity to the chip manufacturing process, which is already intricate.

There is a third location where the cooling system could be integrated: the packaging level. This method of thermal management at the package level is believed to be more compact and efficient in transferring heat compared to the conventional system-level method. It is also nearly as effective as die-level thermal management in terms of heat transfer efficiency, without adding to the cost or complexity of IC fabrication. In this dissertation, we present an additively microfabricated SiP that addresses the thermal management issue, with a performance and size comparable to die-level integration, without adding complexity to chip fabrication. Additionally, it has a significantly smaller size compared to sub-optimal system-level heat sinks. DMLS is used due to its outstanding customization capabilities [62], as the parts are directly fabricated from a CAD file. DMLS has been considered superior to its plastic or resin-based counterparts in certain applications requiring conductive parts with better accuracy and strength [112]. All these features of customizability to conductivity and strength make DMLS process a viable option for designing SiPs with functionalities like heat sinks and connectivity. The use of this process to design heat sinks has been studied [63] but without integration. One of the grand challenges of the International Roadmap for Devices and Systems (IRDS) is 3D packaging and heat extraction for the die [238], [264]. This work showcases various QFN lead frames, some of which include cooling systems and others that do not. The conventional lead frame design with only the pads serves as a comparison reference for the other three systems. The QFN lead frames in this work come in three variations: one with a microchannel, inlet, and outlet for fluid flow; one with arrays of fins below the die location; and one with fins as well as an additional inlet and outlet for optional fluid flow. Fig. 5.1., shows the CAD isometric views of all four proposed package systems. Each package system can hold a 1cm-by-1cm semiconductor die for testing purposes. The microchannels are square-shaped channels that measure $500\mu\text{m}$ in width and $800\mu\text{m}$ in depth, while the fins have a diameter of $1000\mu\text{m}$. Affordability comes with the trade-off of resolution and the present in-house system can faithfully produce the mentioned dimensions with compatible features for the channels and fins.

5.2.Design

The first step in bringing the packages to life is creating a CAD design and simulating it. The CAD model for the packages were designed in Onshape. Four unique designs were first realized and are demonstrated in Fig. 5.1. The first design of the package as shown in Fig.5.1., (top left) is based on a conventional lead frame package with a die holder and 20 leads or pads for die connectivity. The pads and die holder are designed on a support plate so that the parts will be fabricated and held in place, which can be ground off later, isolating the pads and die holder for electrical isolation. The die holder in the second design in Fig. 5.1., (top right) has been modified to feature an array of 25 micro pin-fins, each with a diameter of $1000\mu\text{m}$, but without flow inlet and outlet. The other design as in Fig.5.1., (bottom right) is a version of the former one with flow inlet and outlet. The design shown in Fig.5.1., (bottom left) features a modified die holder with a serpentine microchannel measuring $500\mu\text{m}$ in width and $800\mu\text{m}$ in depth, as well as flow inlet and outlet. These four designs are the initial designs fabricated and evaluated in this work. It is worth noting that the microfluidic structures are open at the top end, where the die will be placed. This open-on-top arrangement supports direct convective cooling and bypasses thermal resistance between the silicon die, package, and thermal interface material (TIM) by allowing direct contact with the backside of the die on the holder, which will not be the case if the microfluidic structures are designed as closed structures at the top.

Each design was simulated to study thermal management performance before the fabrication of the package. ANSYS 2019 Thermal-Electric and Computational Fluid Dynamics (CFD) analysis system was used to simulate the thermal management properties of the packages. Fig. 5.2., shows the results for the ANSYS simulation where the average surface temperature was reduced to around 28°C for packages with micro pin-fins and with microfluidic channels with water flow of around $120\text{ml}/\text{min}$ compared to conventional package at 45°C .

5.3.Fabrication

The initial step of fabrication involved the processing of the CAD design discussed in the previous subsection. The CAD design was sliced using the slicing software Netfabb™. The slicing software then created a laser path for the fabrication which was fed to the Xact Metal XM200C™ 3D printer pre-loaded with 316L Stainless Steel powder. The fabrication proceeds as soon as the printer starts, and the process is like Fig. 4.3. The microfabrication process involves melting and fusing multiple layers of 30µm powder together until the final 3D part is built according to a CAD file. The part gets fused to the built plate as well. EDM wire cutting or grinding can be employed to detach the parts from the build plate after the creation of support structures. In this work due to larger sizes of devices, each single packages are supported on a 1mm thin metal plate to hold the pads and die holder in place and have tapered wedges 4mm tall on the bottom, which will be the easy base fused on build plate to be removed using grinding tools for electrical isolation of pads and die holder.

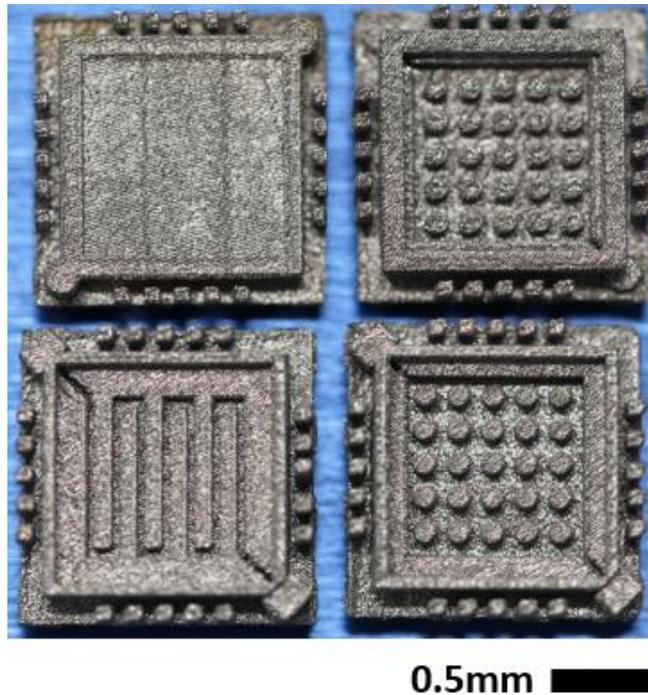


Figure 5.3: Microfabricated packaging devices in same order as Figure 7.1. Conventional Package (top left), package with micro fins (top right with only micro fins, bottom right with fins, inlet, and outlet), package with microchannel (bottom left).

The individual packaging devices are shown in Fig. 5.3. On each part, 1cm by 1cm semiconductor dies will be carefully placed. Wire bonding will be used to connect the via to the leadframe pads. The inlets and outlets, if present, will be extended and the cooling liquid supply will be connected. The entire system will then be covered with epoxy and left to cure. The final step will be to grind off the back end of to remove support metal plate on the bottom of the packaging parts, as shown in Fig. 5.4. Currently, the only cooling systems added to the SiP are microchannel with inlet and outlet, fins, and fins with inlet and outlet. As future work, radiation shielding, and other microsystems could be incorporated.

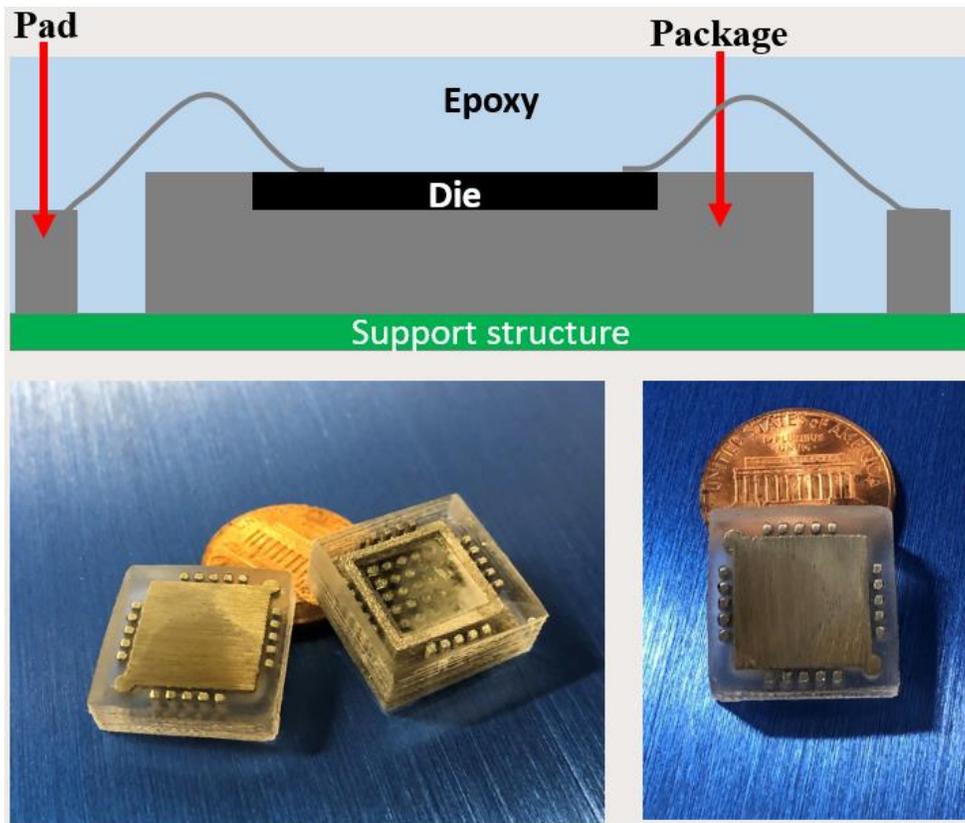


Figure 5.4: Proposed post processing steps for final package include die placement, wire bonding, and epoxy curing (top). The sacrificial support structure in green will be ground off after epoxy curing to electrically isolate leads and package to finally create a surface-mount package as demonstrated in the bottom (left and right).

5.4. Material Characterization

A thorough analysis was conducted on the characteristics of the as-built parts and additional samples. In order to understand how the fabrication process aligned the powder particles, a close examination of the microstructures was carried out. While micro-voids were present, no micro-cracks were observed during the analysis. The optical micrographs of a printed package without post-processing were carefully analyzed and the results are shown in Fig. 5.5. Some voids are circled in red, which were in the range of powder particle diameter. If these voids accumulate and create a leakage path, it can affect coolant flow. However, no such leakage was observed during the testing. The use of smaller powder or post-processing steps may be helpful in solving the problem of micro-voids and extra melted powder. The overall microstructures were dense enough to allow further processing. Extra melted powder sticking around the pad is also visible, which might form an electrical leakage path. Again, this could be solved using finer powder or employing post-processing steps. However, for this design, each pad is spaced much apart from the other compared to the powder size, and further processing is possible.

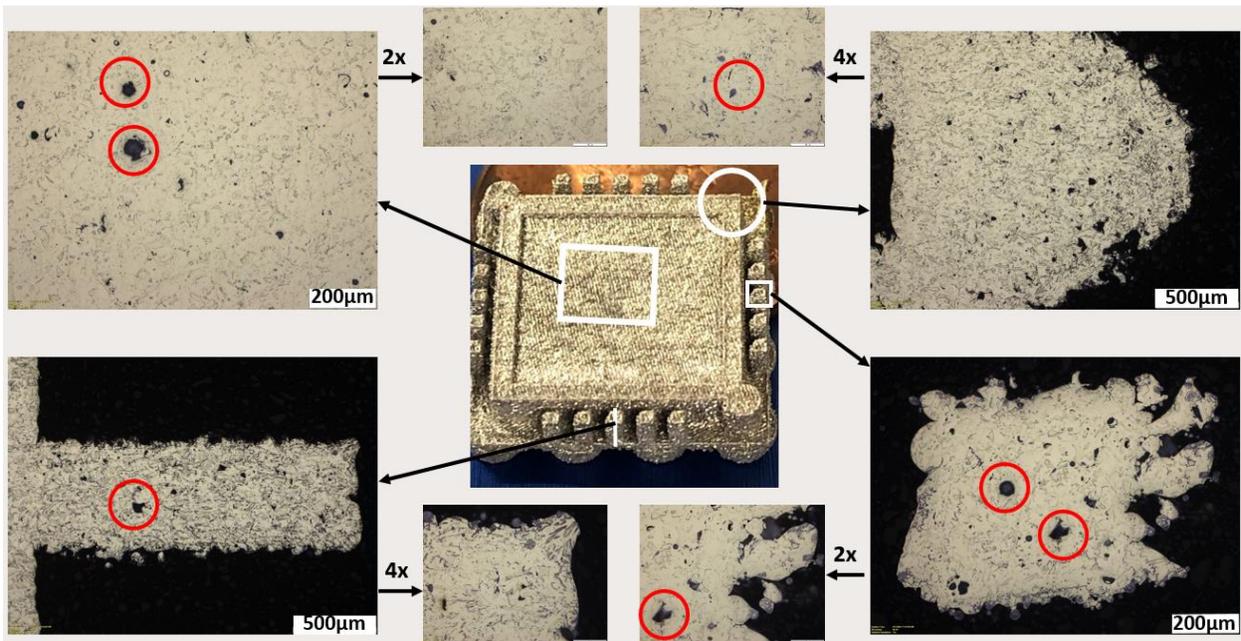


Figure 5.5: Optical micrographs of as printed package obtained at the regions indicated by the central image showing micro-voids introduced by DMLS process.

The surface roughness of fabricated devices has been determined using the Bruker DektakXT stylus profiler on multiple samples pre-post-processing. The top surface of the fabricated devices was scanned to around 7500 μm to study the presence of bumps and valleys. A comprehensive profilometry analysis of three samples is presented in Fig. 5.6. The scan direction and profiler utilized have been illustrated in the bottom right corner of the figure, while the top left, top right, and bottom left correspond to the three samples that have been examined. The average surface roughness falls within one powder size range, but the maximum surface roughness is twice the size of the powder. This may adversely affect wire bonding performance and thermal transport at the interfaces. However, these issues can be resolved by post-processing like polishing or using finer powders thereby enhancing the functional performance of the fabricated devices.

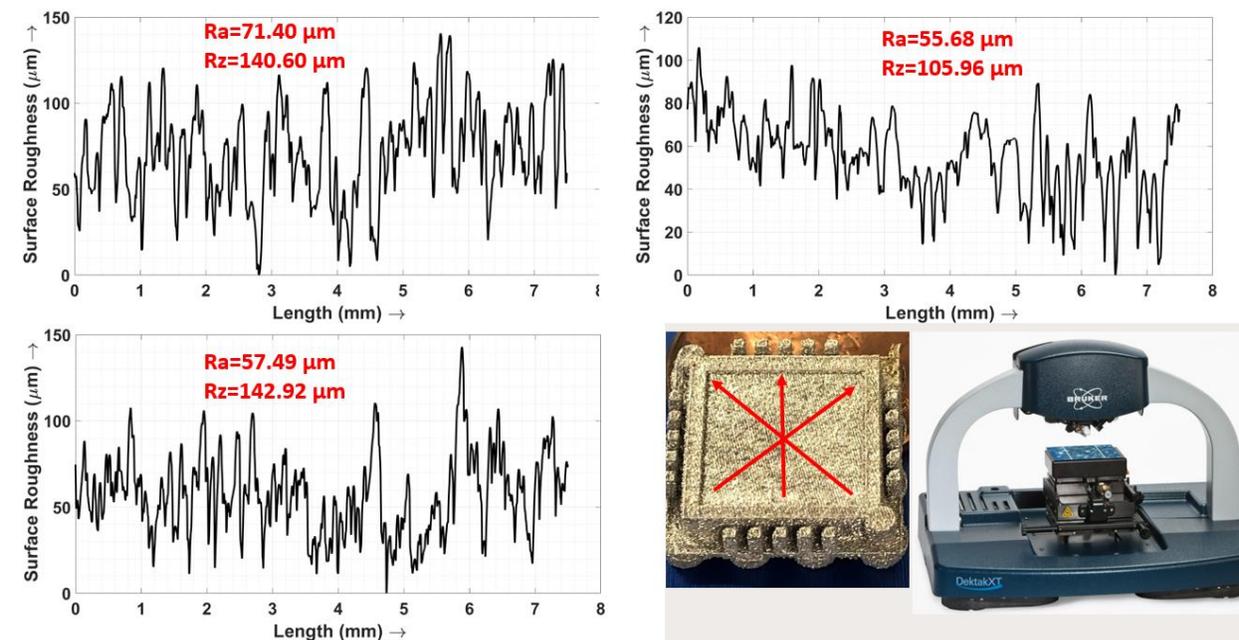


Figure 5.6: Profilometric graph for the analysis of as build package surface roughness. Sample with scan line (bottom middle) and Bruker DektakXT stylus profiler (bottom right) used for the analysis.

The samples with fins and microchannels were also analyzed for their dimensional accuracy. Fig.5.7., shows the 3D surface profile of the package with micro pin-fin (top) and microchannel (bottom) on the left and Scanning Electron Microscope (SEM) micrograph of the

samples on the right with the same setup as the former. Upon examining the SEM analysis, the average diameter of the fin is found to be $1046 \pm 52 \mu\text{m}$, which is a slight deviation from the $1000 \mu\text{m}$ diameter present in the CAD file. Similarly, the SEM microchannel width is determined to be $506.83 \pm 36 \mu\text{m}$, whereas the CAD file indicates $500 \mu\text{m}$. The margin of error is relatively small, and it could be attributed to the cumulative effects of print resolution, powder diameter variability, and manual measurement error. The 3D surface profile further demonstrates the consistency in dimensions across the samples. The DMLS process used here showcases superior dimensional accuracy. It is possible that even greater dimensional accuracy could be achieved through the optimization of resolution and print parameters with finer powder. Overall, the results of this analysis demonstrate the value of utilizing DMLS technology for the creation of highly precise and accurate parts.

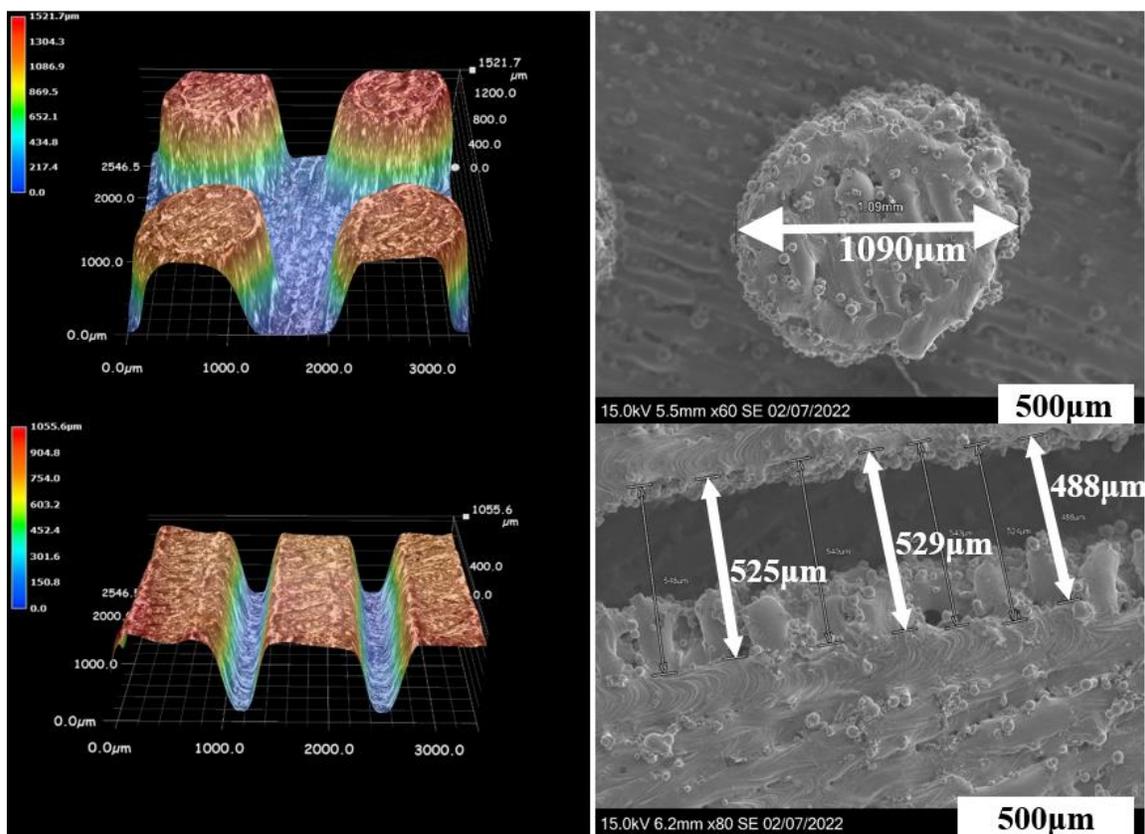


Figure 5.7: 3D depth profile of pin-fin package (top left), microchannel (bottom left). SEM micrograph of pin-fin (top right) and microchannel (bottom right).

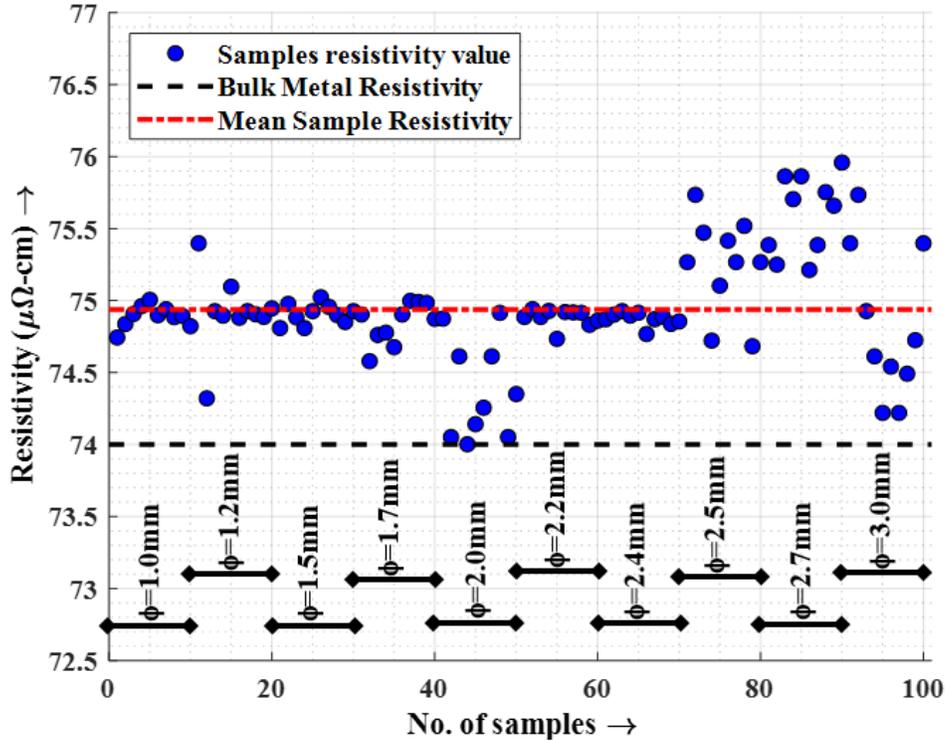


Figure 5.8: Resistivity of 100 samples, along with 316L stainless steel bulk metal resistivity and mean sample resistivity with the diameter (ϕ) ranges of the samples.

The determination of the resistivity of the printed material was conducted through the fabrication and four-wire resistance measurement of one hundred cylindrical rods. These rods were made using the DMLS process and 316L stainless steel powder, which is also utilized in SiP fabrication. The rods had varying diameters, ranging from 1mm to 3mm, and lengths ranging from 6mm to 15mm, with increments of 1mm. The resistance values of these samples were measured using the Keithley 2450 SourceMeter® and a four-wire (Kelvin) technique along the entire length of each sample. The four-wire resistance measurement technique involves passing a 1A current through the Force Hi probe, which is connected to one end of the sample. The circuit is then completed by connecting the other end of the sample to the Force Lo probe. The voltage drop across the sample ends will be measured by the Sense Hi and Lo probes. This method allows for precise measurements by eliminating any potential errors caused by the resistance of the connecting wires. The Keithley SourceMeter automatically determines the ratio of voltage and

current to display the value of the resistance for the sample. The material's resistivity is calculated using the resistance, length, and diameter of each sample using the laws of resistance. This reading will be of importance as it relates to the resistance value of the lead between the vias and the pads on the PCB. The lower the resistance, the better the electrical connectivity with the vias, which in turn ensures a seamless flow of current without any loss. Fig. 5.8, displays the resistivity measurements of one hundred samples, including the mean sample resistivity and the bulk metal resistivity from literature [265], [266]. All the values are considered at room temperature. The mean sample resistivity value of the samples was determined to be $74.94\mu\Omega\text{-cm} \pm 0.39$, which is approximately $1\mu\Omega\text{-cm}$ higher than expected bulk metal resistivity.

5.5. Experiment and Results

A preliminary study was conducted to demonstrate the movement of fluid within packages that incorporated both channels and fins. The flow of water, with added food coloring to enhance visibility, in the microfluidic structures is shown in Fig. 5.9., (top left: microchannel with coolant, bottom left: channeled fins with coolant) with a 1cm-by-1cm glass glued on top of the die holder for individual package. These two devices along with the conventional package and the one with only fins (all of them with 1 cm-by-1cm glass cover) had their respective glass cover heated with a hot-gun to a temperature of 40°C and allowed to cool down to ambient temperature.

For similar environmental conditions, based on the thermal images obtained, it was observed that the packaging devices equipped with fins and coolant flow exhibited a higher rate of cooling compared to the conventional package. This indicates that the incorporation of these features has a significant impact on the cooling performance of the package. The packaging device with only fins and no cooling water is the last to reach the ambient temperature. This is demonstrated by the thermal images in Fig. 5.9., (right). The cooling delay in the later type of package can be well explained through the basic concept of heat transfer. As the conventional

device and the one with only fins and no flow could lose heat just by conductive heat transfer to the heat sink, the package, which was solely composed of fins without any flow, underwent an extended period of cooling. This is likely due to the decreased conductive interface, compared to the conventional package that resulted from the presence of fins, which reduces the rate of heat transfer. The microchannel on the other hand, although had stagnant water as coolant, its convective cooling capability is greater than that of stagnant air and was the second one to cool faster. As the cooling system with fins and stagnant coolant, can transfer heat via conductive and stagnant water convective cooling with larger surface area, it cooled the faster.

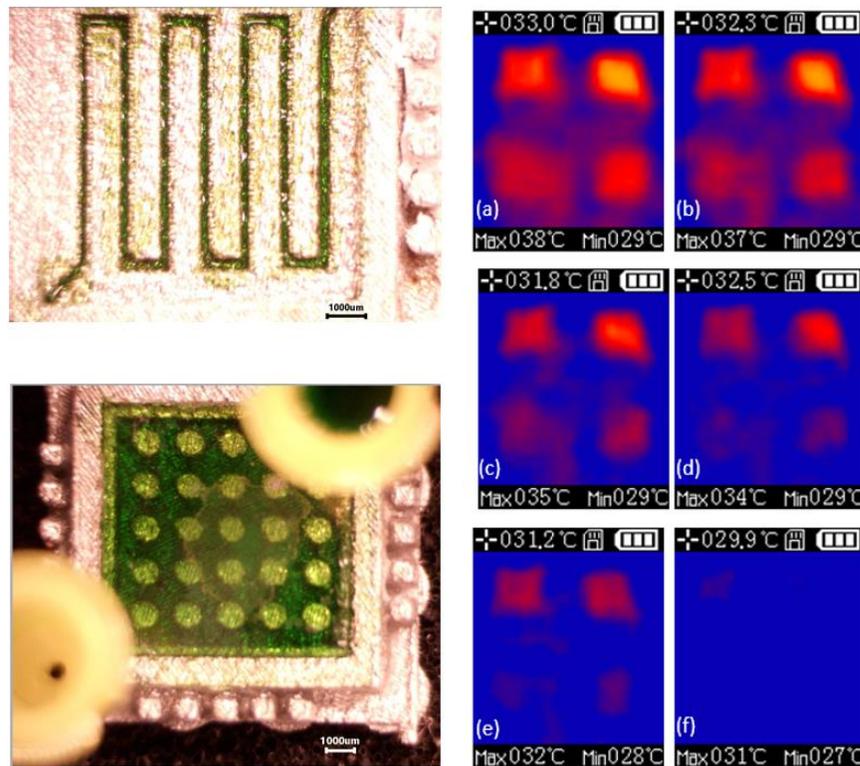


Figure 5.9: Microchannel (top left) filled with coolant, finned heatsink filled with coolant (bottom left), and Heat map for all four devices (right) left to cool down in ambient environment after heating the glass slide on top of each device to 40°C (a-f). The devices were set up in a similar fashion to Fig. 5.3.

Another experiment was performed, where the glass slides were placed on top of various samples and were heated using a heater. The slides were then allowed to cool naturally under

ambient conditions as shown in Fig.5.10 (right). A thermal camera was used to record the average temperature, while a stopwatch was used to note the time taken for each sample to cool down. The results, as shown in Fig. 5.10 (left), demonstrate the impact of air and water flow on the cooling process. The package with pin-fins and water flow was found to have the shortest cooling time to reach ambient temperature, taking only 3.3 minutes. The microchannel package with the same flow rate followed closely behind, taking 4.2 minutes to cool down. In comparison, the pin-fin and microchannel packages with similar air flow rates took significantly longer to cool down, with times of 10.6 minutes and 13.9 minutes, respectively. The original package and the package with pin-fins but no flow took even longer to cool down, with times of 25.5 minutes and 32 minutes, respectively. These findings demonstrate the ability of these packaging devices to achieve effective cooling, even with higher flow rates of air.

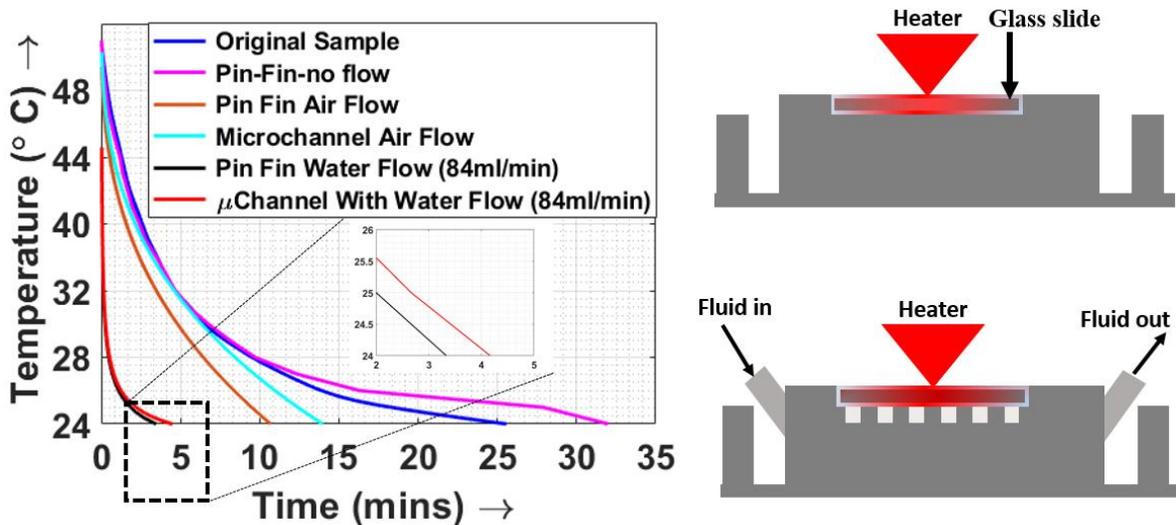


Fig. 5.10: Experimental set for transient thermal performance analysis of the packages: Original sample (top right), samples with coolant flow (bottom right). Transient thermal performance of different samples illustrating the time taken to cool down to ambient while heated to 48°C and let to cool down to ambient temperature.

A third experiment was conducted to analyze the steady-state thermal performance of each package. The top surface of the glass slides was exposed to a heat flux of 4.5W generated by a cartridge heater, with flow turned on for flow-capable devices. A set of four NTC temperature

sensors recorded the temperature of four points on the top surface of the glass slide. Two more temperature sensors recorded the temperature of the inlet and outlet coolant. The data from sensors were read using a microcontroller calibrated using the manufacturer data for the thermistor. The entire setup is illustrated in Fig. 5.11., (left). The steady-state surface temperature and thermal resistances are shown in Fig. 5.11., (right), with measured thermal resistances of $2.02^{\circ}\text{C}/\text{W}$ (pins) and $2.20^{\circ}\text{C}/\text{W}$ (channel) for a flow rate of $84\text{ml}/\text{min}$ compared to $5.25^{\circ}\text{C}/\text{W}$ for the original package.

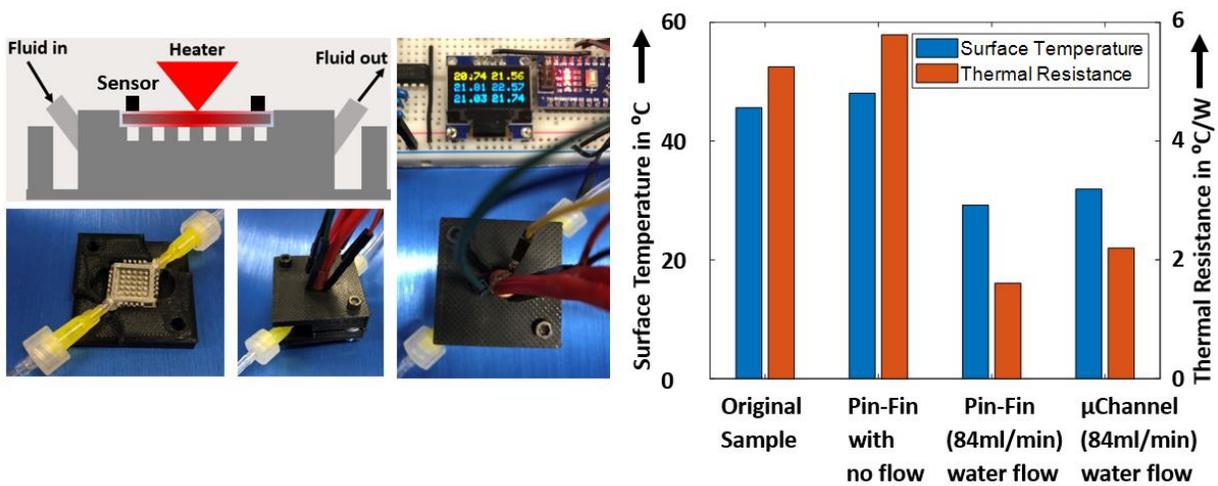


Figure 5.11: Experimental set for steady state thermal performance analysis of the packages: Experimental setup (right) with cartridge heater ($P=4.5\text{W}$) and temperature sensor with full data acquisition system. Steady state thermal performance of different samples illustrating the final average surface temperature and thermal resistance of each sample when subjected to same heat flux.

Further increase in the water flow rate, there was a significant decrease in thermal resistance to about $1.57^{\circ}\text{C}/\text{W}$ and a reduction in the average surface temperature to approximately 27.5°C , as depicted in Fig. 5.12. When comparing micro pin-fin to microchannel, it was found that the former outperformed the latter in terms of flow rate and thermal performance at a similar pump power.

However, it was observed that thermal performance did not improve significantly beyond a flow rate of approximately $40\text{ ml}/\text{min}$ in both cases. Thus, there is a need for further optimization,

which will be discussed in Chapter 6. The optimized microchannel includes new wavy structures to improve hydrodynamics for better thermal performance. On the other hand, in the case of micro pin-fin, the diameter of each pin is decreased to allow number of pins, ultimately increasing the convection surface area for better thermal performance. Additionally, changing the shape to ovate/teardrop enhances hydrodynamic performance. The wavy microchannel is around 500 μm wide and 800 μm deep, whereas the tear-drop shaped micro pin-fins are 2500 μm in circumference and 800 μm high. The detailed design, fabrication, and the rationale for the optimization along with the reduction in the thermal resistance and final surface temperature, which will be inspected and discussed in the next chapter.

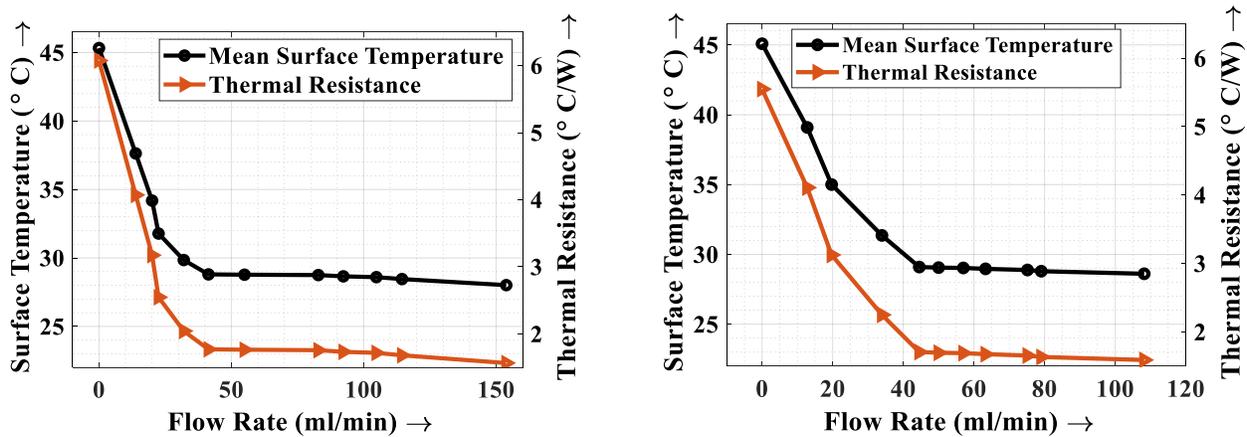


Figure 5.12: Mean surface temperature and thermal resistance for micro pin-fin heat sink for different water flow rates (left) and mean surface temperature and thermal resistance for microchannel heat sink for different water flow rates (left)

5.6. Discussions

Initial tests have revealed that when it comes to cooling, pin-fin followed by microchannel SiPs paired with water flow is a highly effective method. In comparison to traditional packages, these heat sinks have a significantly greater cooling rate. However, the thermal performance of these SiPs is contingent on several factors, including the size of the pin-fin and microchannel, their

number, and the flow rate. It's worth noting that if water isn't a feasible coolant, air-cooling heat sinks can be applied to SiPs. That being said, for high-performance devices and power electronics, water cooling systems are a more viable solution. The following chapter will provide an in-depth exploration of all these topics, including the heterogeneous integration of these SiPs with dies to additively microfabricate low-cost SiPs with improved electrical and thermal performance.

The thermal performance of various heat sinks used in previous studies has been summarized in Table 5.1. Die-level thermal management systems have been found to exhibit lower ranges of thermal resistances. Two-phase cooling has been advocated for its superior thermal performance; however, it is not within the scope of this study. Hydraulic diameter and flow rate are other parameters that affect thermal performance. This study presents systems with larger hydraulic diameters compared to those listed in Table 5.1. It is important to note that this work utilizes soda-lime glass instead of silicon, resulting in a higher overall thermal resistance due to the lower thermal conductivity of soda-lime glass. Despite this, package-level thermal management performs similarly to die-level thermal management, but there is still room for improvement.

Table. 5. 1. Comparison of present work with various works in literature with their fabrication processes, hydraulic diameter (D_h) if the work relates to microfluidic channel or Pin-fin diameter (D_p) if the work relates to micro pin-fin (also indicated with (P) in front of values, flow rates and corresponding thermal resistances (R_θ), the coolant used, and the mode indicating if phase change phenomenon was utilized or not.

Work by	Fabrication	D_h or D_p (μm)	Flow rate (ml/min)	R_θ ($^\circ\text{C}/\text{W}$)	Coolant	Mode
Agostini et al. [54]	Silicon back-side etch (Die-level)	122	490	0.013	R-236fa	Two-phase
Tuckerman and Pease[27]	Silicon back-side etch (Die-level)	92	516	0.1	Water	Single-phase
Sarvey et al.[267]	Silicon back-side etch (Die-level)	(P) 30	100	0.33	Water	Single-phase
van Erp et al.[56]	Silicon back-side etch (Die-level)	166.7	60	0.43	Water	Single-phase
Kong et al.[58]	Precision machining on copper	(P) 400	66	0.53	Water	Two-phase
Liu et al.[58]	Fabrication on a copper block	(P) 445	953.75	0.88	Water	Single-Phase
Peles et al.[57]	Silicon back-side etch (Die-level)	(P) 100	3.2	~ 5	Water	Single Phase
This work (1)	Package-level	615.38	84	1.59	Water	Single-Phase
This work (2)	Package level	(P)1000	84	1.57	Water	Single Phase

Chapter 6: Optimization of Microfluidics and Silicon Integration to SiPs

Chapter 5 discussed the requirements of die-level thermal management for electronics. The chapter also provided a complete solution in the form of straight serpentine microfluidic channel (SSMFC) and circular pin-fins (CPF) on the die holder, open towards the back of the die for direct convective cooling of the semiconductor die placed on the die holder. The SSMFC and CPF microfluidic structure performed well when tested with the glass slide and it was possible to reduce the thermal resistance of the whole package to around $2.02 \text{ W}/^\circ\text{C}$ for package with CPF, which is a good enhancement compared to the conventional package ($5.25 \text{ W}/^\circ\text{C}$) as per the graph in Fig.5.11., and Table 5.1. If the graph is analyzed properly, it seems like the thermal resistance decreases considerably till the flow rate is increased to around $40 \text{ ml}/\text{min}$ for both SSMFC and CPF, implying the reciprocal relation between the flow rate and thermal resistance. However, contrary to the popular belief [268], a big jump in flow rate from 40 to $150 \text{ ml}/\text{min}$, the decrease in the thermal resistance is very minimal. There are two reasons that might explain this anomaly.

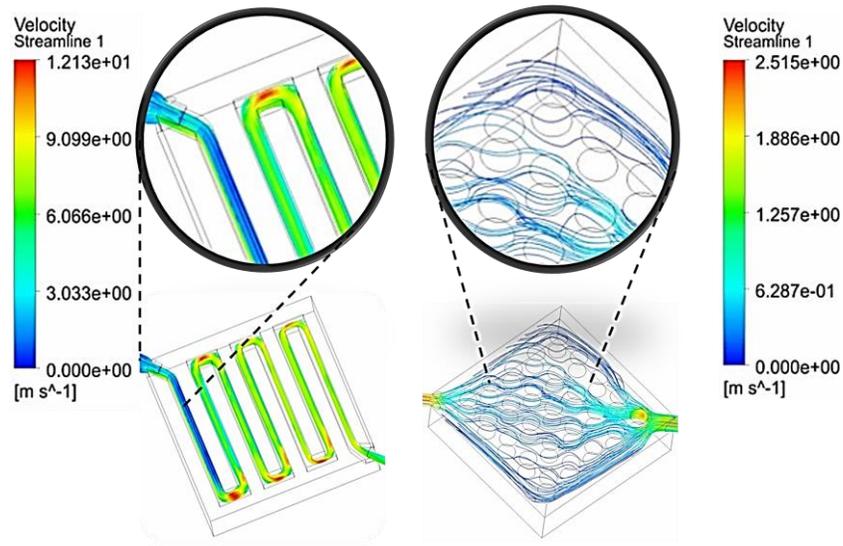


Figure. 6.1. ANSYS CFD simulation of water flow in SSMFC (bottom left) and CPF (bottom right) illustrating the flow behavior/ hydrodynamic nature. Enlarged sections showing the regions showing decrease in water contact area due to poor hydrodynamic nature of SSMFC (top left circle) and CPF (top right circle).

One of the reasons, of course, being the hydraulic diameter as the heat transfer coefficient increases with decreasing hydraulic diameter. In this work hydraulic diameter for the microchannel is limited by the DMLS resolution and, the microchannel in this work has been designed considering the lowest possible resolution. Hence in the case of microchannel, the hydraulic diameter cannot be decreased any more unless the DMLS resolution is decreased. However, in the case of micro pin-fin (with the diameter of $1000\mu\text{m}$), it can still be decreased.

Another reason is the hydrodynamic inefficiency of the SSMFC and CPF which causes improper flow of water in the microfluidic regions as shown in Fig.6.1. Due to the improper flow of fluid leading to the decrease in the total surface area of fluid contact with the back side of the die, ultimately decreasing the hydraulic diameter compared to what is expected. There is room for the improvement of both the microfluidic structure to enhance the hydrodynamic nature of the flowing water and will be discussed in upcoming subsections.

6.1. Optimization of Microfluidic Structures

In this section the optimization of both microfluidic microchannel and microfluidic micro pin-fins will be discussed. To improve the hydrodynamic flow in the microfluidic channel, the serpentine straight design (SSMFC) as discussed in previous chapter has been upgraded to the serpentine wavy design (SWMFC). [269]–[271]. One more orientation of channel namely Parallel Straight Microfluidic Channel (PSMFC) will also be studied in the subsection. Similarly, in comparison to the previous chapter, the circular pin-fin (CPF) is optimized to a teardrop/ovate micro pin-fin based on literature and on hydrodynamics [272], [273]. The size of the microchannel feature remains the same according to the printer resolution, only the shape is adjusted to impart hydrodynamics. Fig. 6.2., shows all the three CAD models of the packages with microfluidic channels contained in this. However, in addition to enhancement of the hydrodynamic nature of

the teardrop pin-fin (TDPF), the reduction in the diameter for pin-fins also allows for more pins to be placed within the same volume increasing the hydraulic diameter. Another design, namely the Square Pin Fin (SPF) has also been incorporated in this study of optimization. Fig. 6.3., illustrates all the three designs studied in the optimization of the microfluidic pin-fins.

6.1.1. Hydrodynamic Optimization of Microfluidic Channel

The hydrodynamic optimization of microfluidic channel comes from the fact that there is just the possibility of optimizing the shape of the microchannel as the size is already limited by the DMLS resolution. In this work three different hydrodynamic shapes are compared for their flow rate and thermal management efficiency. Three shapes are straight serpentine microfluidic channel (SSMFC), parallel straight microfluidic channel (PSMFC), and serpentine wavy microfluidic microchannel (SWMFC) with their respective CAD models (from left to right) on Fig.6.2., (top) and the fabricated packages on Fig.6.2., (bottom). The dimensions of all the microchannels are unaltered and are 500 μm wide and 800 μm deep. As in the previous chapter, the microchannels are left open towards the top to impart direct convective cooling of the back surface of the die.

Although, the dimension of the channel in the SWMFC is unaltered and is the same as the others, some modifications are added to impart better hydrodynamic nature of the channel. The modification comes in the form of change of straight edge of the SSMFC to wavy edge following a sine wave with an amplitude of 125 μm as illustrated in the detailed design illustration in Fig.6.3. The introduction of the equal and opposite wavy edges to the channel leaves the total wide of the SWMFC the same as the SSMFC, which is 500 μm . The introduction of wavy channel is dictated from literature where the design is considered hydrodynamically more efficient compared to the straight edged channels [269]. The PSMFC however has the same channel dimension with straight

edges but the 9 parallel microchannel extended from the input to the output instead of a single serial serpentine channel. The fluid flow and thermal management performance of these modifications will be compared and studied in subsection 6.2.

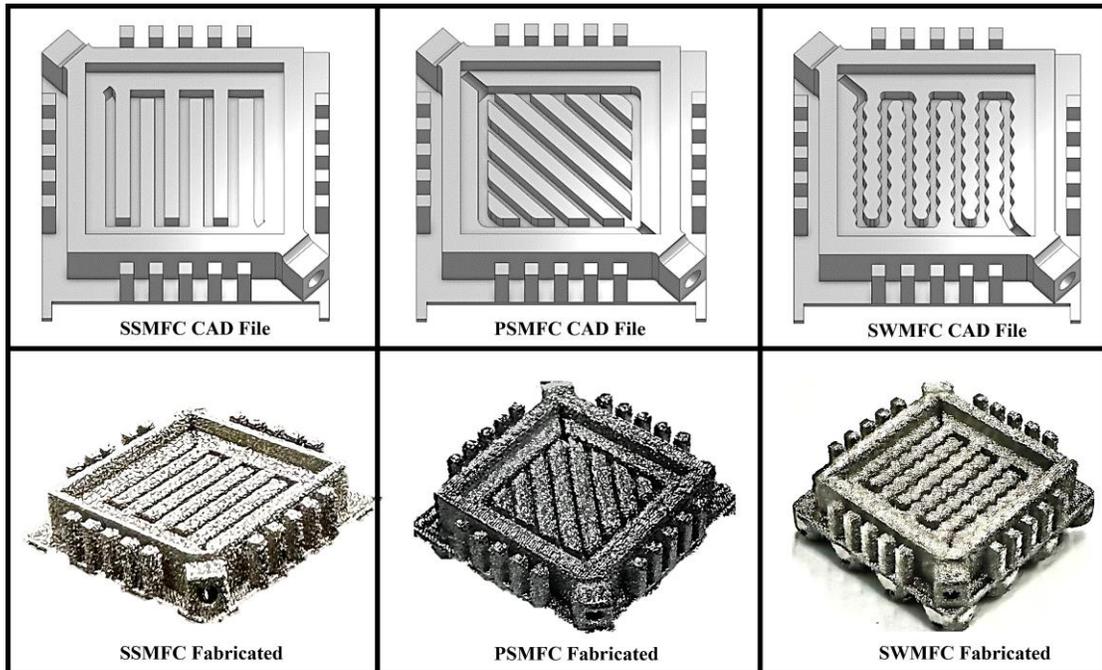


Figure 6.2. CAD models of packages with different shapes of microchannel (top) viz SSMFC, PSMFC, and SWMFC (from left to right respectively), and the fabricated packages with different shapes (bottom) following the same order as the top.

6.1.2. Hydrodynamic and Hydraulic Optimization of Microfluidic Pin-Fins

The hydrodynamic and hydraulic optimization of the microfluidic pin-fin comes from the fact that there is a possibility of optimizing both the shape and the size of the pin-fins. In this work three different hydrodynamic shapes are compared for their flow rate and thermal management efficiency. Three shapes are circular pin-fins (CPF), square pin-fins (SPF), and Teardrop pin-fins (TDPF) with their respective CAD models (from left to right) on Fig.6.4., (top) and the fabricated

packages on Fig.6.4., (bottom). As in the previous chapter, the microfluidic regions are left open towards the top to impart direct convective cooling of the back surface of the die.

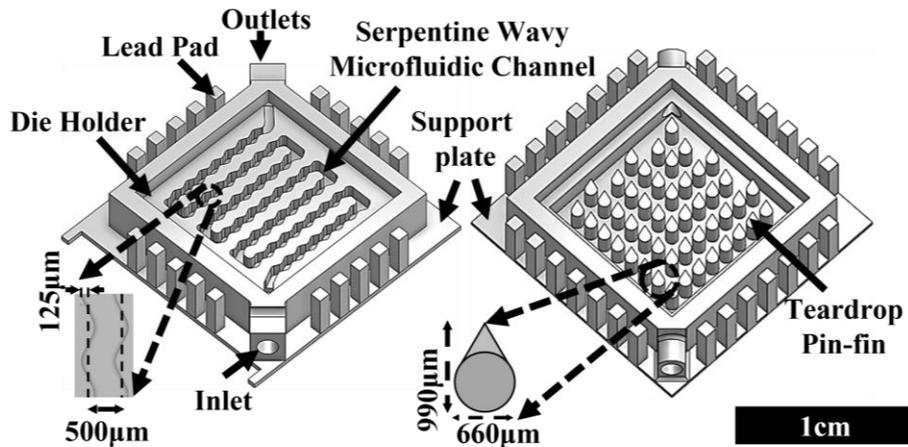


Figure 6.3. Detailed CAD models of packages with SWMFC (left) and TDPF (right). The inset gives the dimension of the channel and the amplitude of the wavy edge as well as the design dimension of the teardrop pin.

The dimension of each of the 25 circular pin-fins in the CPF is $1000\mu\text{m}$ as discussed in the previous chapter. The square pin-fins are designed to study the difference in the hydrodynamic nature of these structures compared to the CPF. Each of the 25 pin-fins in SPF are $800\mu\text{m}$ -by- $800\mu\text{m}$ in size which is comparable to a $1000\mu\text{m}$ circular shape. The modification in the shape and the number of pin-fins in TDPF comes in the form of change of circular shape of the pins to a more hydrodynamic shape of the pin as illustrated in the detailed design illustration in Fig.6.3. The decrease in the size of the pin-fins is possible in this case, due to printer resolution, making room for a greater number of the pins (48 in TDPF compared to 25 in CPF and SPF). The introduction of tear-drop shape is borrowed from airfoil structure of planes and is dictated from literature where the design is considered hydrodynamically more efficient compared to the circular or square pins [274]. The fluid flow and thermal management performance of these modifications will be studied and compared in subsection 6.2.

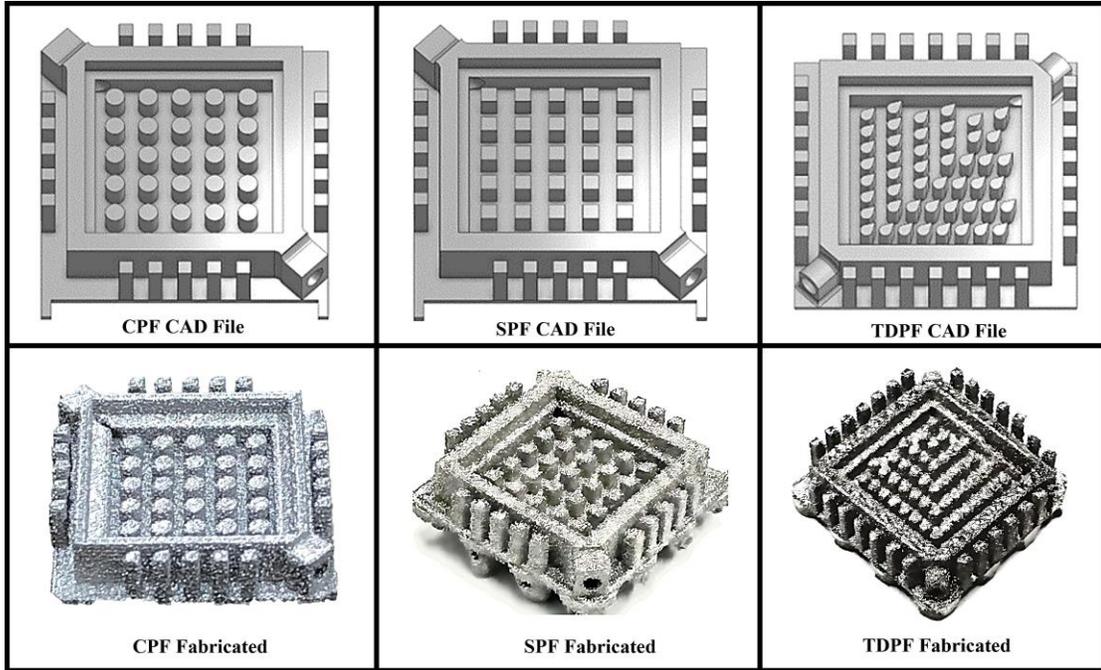


Figure 6.4. CAD models of packages with different shapes of microfluidic pin-fins (top) viz CPF, SPF, and TDPF (from left to right respectively), and the fabricated packages with different shapes (bottom) following the same order as the top.

6.2. Comparative Study of Optimized Structures with silicon integration

The comparative study in this subsection is done with the same experimental test-setup and data analysis methods as described in Chapter 5, subsection 5.5. In this study, the glass slides used in the previous chapter are replaced by the 1cm-by-1cm silicon die to create real life scenario of operation of these packages. As mentioned in the discussion section of Chapter 5, the introduction silicon die will certainly decrease the overall thermal resistance of the package as silicon has lower thermal resistance compared to glass. The comparative study of flow rates and thermal resistance of all the packages discussed previously is performed and is discussed in detail in the upcoming sections.

$$R_{\theta} = \frac{\Delta T}{q} = \frac{T_{savg} - T_{\infty}}{q}$$

Equation 6.1

6.2.1. Optimization Study for Microfluidic Channels (MFCs)

All the packages with different microfluidic channel structures were subjected to the thermal resistance test using the same setup demonstrated in Fig.5.11. Flow rate of water flow for different pump power were also determined for each package by recording the time it took for 50ml (measured at the outlet using a volumetric tube. The thermal resistance (R_{θ}) was also determined for each packages using equation 6.1., where ΔT is the rise in temperature with respect to the ambient temperature (T_{∞}) and q is the power of the heater. The average surface temperature (T_{avg}) was the average of four temperatures measured by the four thermistors from the setup.

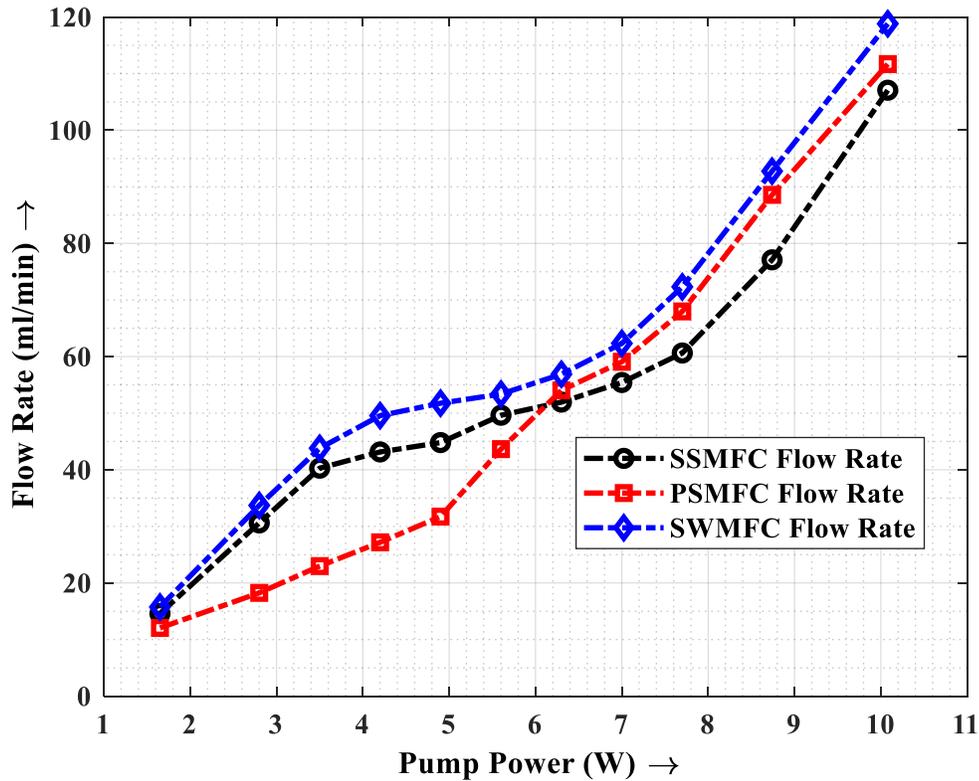


Figure 6.5. Plot of flow rate vs pump power for SSMFC, PSMFC, and SWMFC showing the superior performance of SWMFC compared to the rest.

Fig. 6.5., is a plot for the flow rate of water vs pump power required for packages with different designs of microfluidic channels. As seen in the figure, the flow rates for the PSMFC are the lowest with respect to the pump power compared to the rest till the pump power of around 6W

is reached. After that pump power, the flow rate for the SSMFC does not increase as do the other two. This is due to the fact that for the PSMFC, at lower flow rates, the water chooses straighter path with lower flow resistance and barely flow through the outer parallel channels with greater flow resistance reducing the total flow rates at lower pump power [275], [276]. As the pump power goes up, all the channels will be used for flow increasing the total flow rate compared to the SSMFC. However, for the SWMFC the flow rates with respect to pump power are the best (118.8 ml/min being the highest flow rate possible for the pump used) out of the three because the wavy channels have better hydrodynamic features as compared to the two rest.

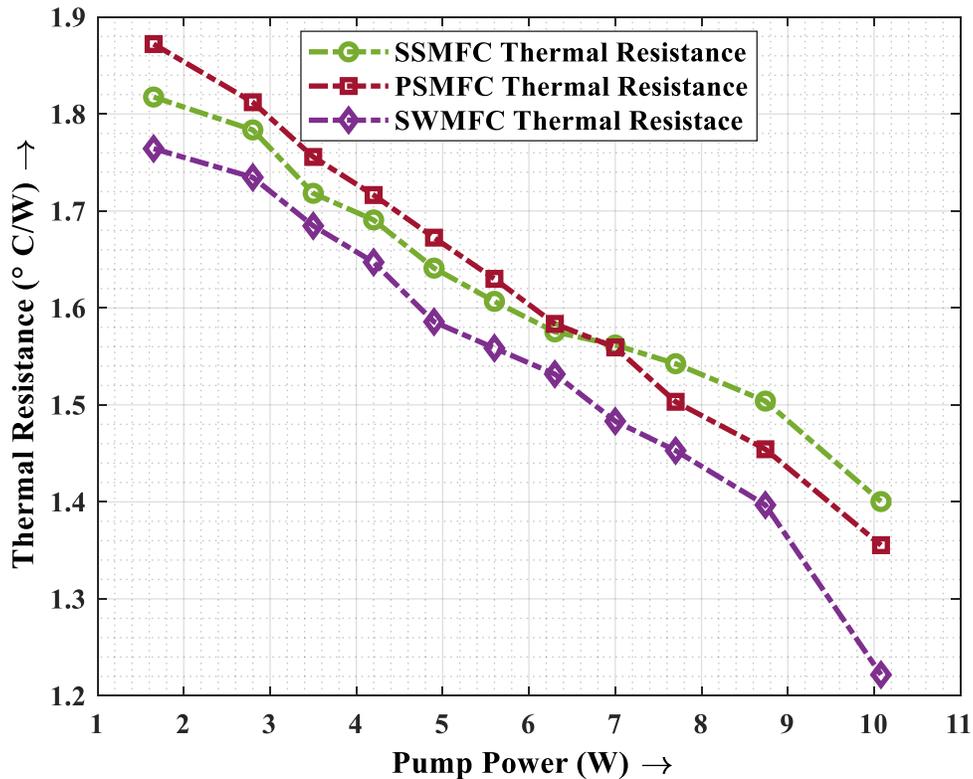


Figure 6.6. Plot of thermal resistance vs pump power for SSMFC, PSMFC, and SWMFC showing the superior performance of SWMFC compared to the rest.

The thermal resistance for different pump power or flow rates also tells a similar story. As the flow rate, the thermal resistances for different channels shapes follow similar fate as illustrated

in Fig. 6.6. For lower pump power implying lower flow rates, the thermal efficacy of the PSMFC is the lowest till the pump power of around 6W. However, for the SWMFC, the thermal resistance is the lowest (1.22°C/W being the lowest thermal resistance for the highest flow rate possible for SWMFC) compared to the rest. This leads to the fact that introduction of hydrodynamically suitable microfluidic channel imparts better heat transfer efficacy.

6.2.1. Optimization Study for Microfluidic Pin-Fins (MPFs)

Similar analysis as in the MFCs has also been done in the case of MPFs. The flow rate vs pump power as well as the thermal resistance vs pump power has been studied for CPF, SPF, and TDPF. Once again, the packages are integrated with 1cm-by-1cm silicon dies. The flow rates and thermal resistance with respect to the pump power were also calculated like the previous section.

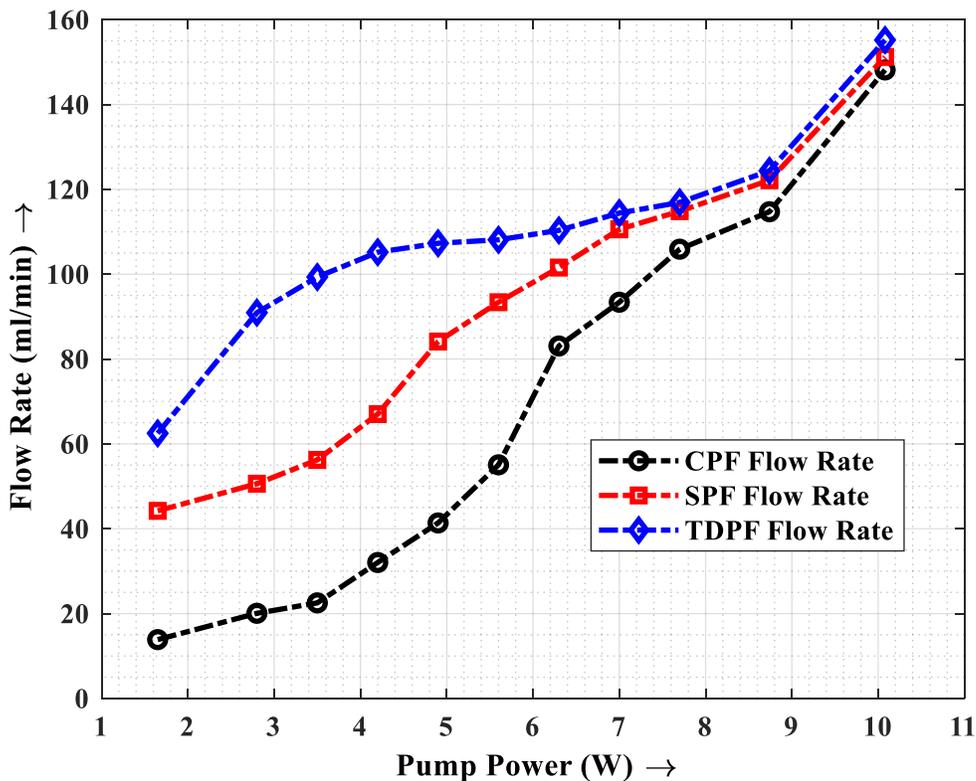


Figure 6.7. Plot of flow rate vs pump power for CPF, SPF, and TDPF showing the superior performance of TDPF compared to the rest.

Fig. 6.7., is a plot for the flow rate of water vs pump power required for packages with different designs of microfluidic pin-fins. As seen in the figure, the flow rates for the CPF are the lowest with respect to the pump power compared to the rest. The flow rate of water for SPF looks a little improved compared to the CPF. This also means, the square pins (with the orientation in this work) are better hydrodynamically compared to circular pins. However, for the TDPF the flow rates with respect to pump power are the best (155.2 ml/min being the highest flow rate possible for the pump used) out of the three because the tear-drop shape has better hydrodynamic features as compared to the two rest.

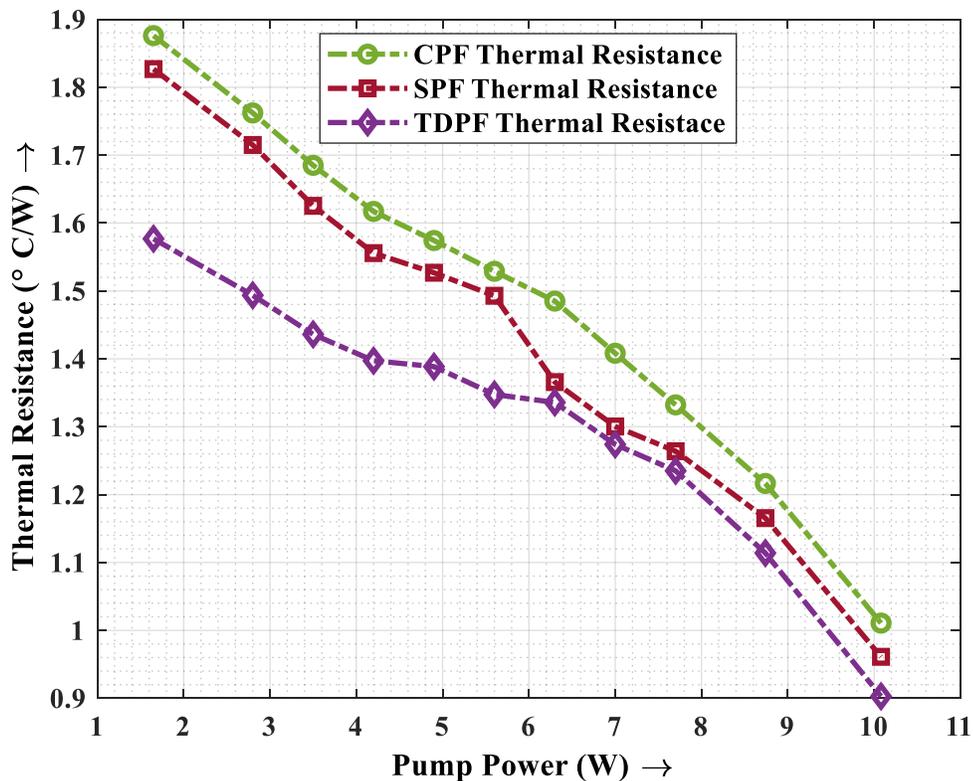


Figure 6.8. Plot of thermal resistance vs pump power for SSMFC, PSMFC, and SWMFC showing the superior performance of SWMFC compared to the rest.

The thermal resistance for different pump power or flow rates also tells a similar story. As the flow rate, the thermal resistances for different pin shapes follow similar fate as illustrated in Fig. 6.8. For lower pump power implying lower flow rates, the thermal efficacy of the SPF is a little lower than CPF till the pump power of around 6W is reached. After 6W, the thermal

resistance of SPF package goes close to (but lower than) the TDPF. However, for the TDPF, the thermal resistance is the lowest compared to the rest ($0.90^{\circ}\text{C}/\text{W}$ being the lowest thermal resistance for the highest flow rate possible for TDPF). This again leads to the fact that introduction of hydrodynamically suitable microfluidic channel imparts better heat transfer efficacy.

To obtain an understanding of the maximum heat flux that can be removed by one of the packages in this work, the TDPF package, it was simulated on ANSYS CFD for different heat fluxes and flow rates. Fig. 6.9. illustrates the heat flux removal capability for the mentioned package. For an integrated circuit chip to operate without much degradation, at temperatures below 90°C , the TDFP packages presented in this work can take in up to a maximum of $191.1\text{W}/\text{cm}^2$ of heat flux.

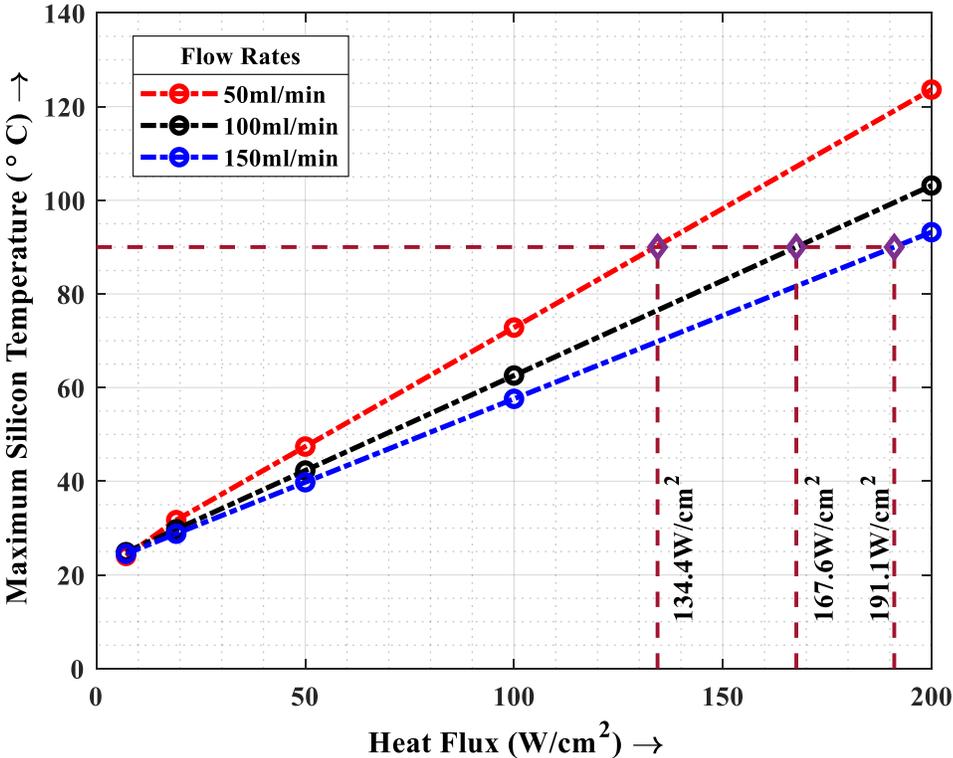


Figure 6.9. Average Silicon Temperature vs Heat flux from the hotspot obtained from simulation for different flow rates of water showing the maximum heat flux the package can handle before the maximum silicon temperature reaches 90°C , the temperature at which most of the electronics start operating differently than intended.

Simulations were also performed by changing the package materials for the tear-drop Pin fin package. Copper, Stainless steel, and glass with thermal conductivities of 397.7, 16.7, and 0.8 W/ K-m respectively were employed in simulation along with the state-of-practice conventional copper-based packages without microfluidic cooling to analyze the effects of materials used for this work. ANSYS CFD simulation for all these materials showed that the heat transfer efficacy of the microfluidic packages in this work has been reduced significantly compared to conventional lead frame packages as seen by the steady state average die temperature demonstrated in Fig. 6.10. At lower heat fluxes all the materials behaved similarly in terms of heat transfer efficiency but at higher heat fluxes the higher conductivity microfluidic package, made of copper, performed better.

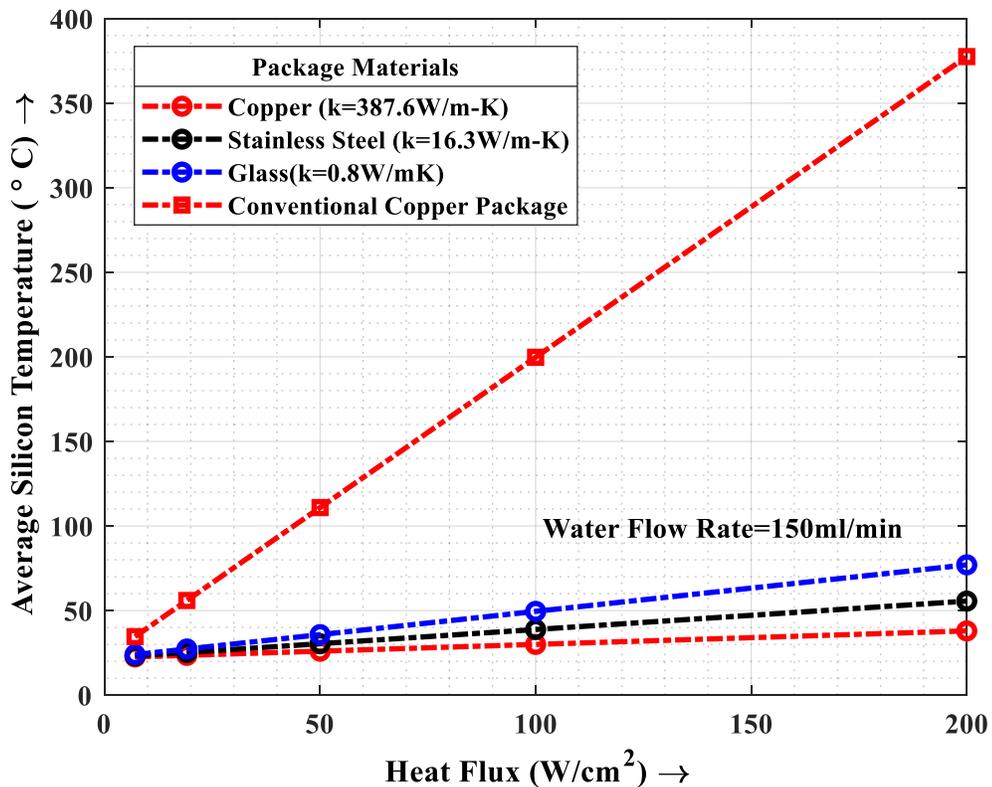


Figure 6.10. Simulated Average Silicon Temperature vs heat flux applied on the Silicon for a TDPF package realized out of different materials as indicated on the legend for a water flow rate of 150ml/min.

6.3. Comparative Study of Optimized Structures with State-of-the-art

The dissertation thoroughly examines and contrasts the proposed thermal management system with state-of-the-art alternatives. Specifically, Table 6.1., presents a detailed comparison of the proposed system with die-level thermal management systems featured in the literature with respect to the hydraulic diameter of a microchannel or diameter of the pin-fin, flow rates, type of fluid, phase of the coolant, and finally the thermal resistance of the thermal management system.

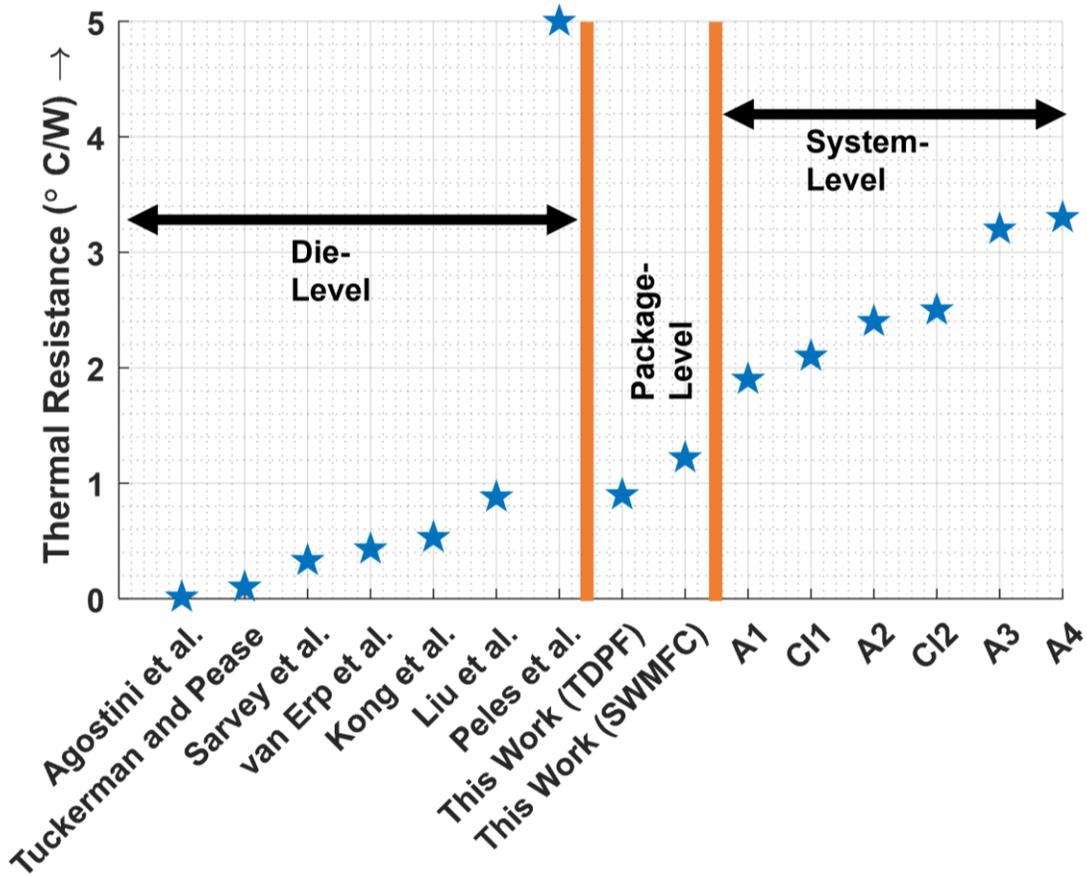


Figure 6.11. Comparative study of different levels of thermal management clearly showing the prospect of package-level thermal management being the one that can be an advanced replacement for the system-level without the cost and complexities that comes with the die-level thermal management solutions.

Notably, the majority of die-level thermal management systems have utilized hydraulic or pin-fin diameters that are considerably smaller [27], [54]–[57] than those implemented in the proposed work. Furthermore, advanced flow pumps are frequently deployed in studies that utilize higher flow rates [27], [54], [58]. Some works have also incorporated a complex mode of two-phase cooling that has resulted in a higher heat transfer efficacy [54], [58]. In light of these advanced features, the proposed work has introduced a package-level thermal management system that is nearly equivalent to die-level thermal management systems [58], [59]. In addition, Fig. 6.11., provides a detailed comparison of the proposed package-level thermal management system with die-level systems in table 6.1, as well as several system-level thermal management devices. The figure demonstrates that, for comparable dimensions of microfluidic structures, flow rates, and mode of flow, the package-level thermal management system is almost on par with die-level thermal management systems and significantly superior to conventional system-level thermal management setups.

Table. 6. 1. Comparison of optimized work with various works in literature with their fabrication processes, hydraulic diameter (D_h) if the work relates to microfluidic channel or Pin-fin diameter (D_p) if the work relates to micro pin-fin (also indicated with (P) in front of values, flow rates and corresponding thermal resistances (R_θ), the coolant used, and the mode indicating if phase change phenomenon was utilized or not.

Work by	Fabrication	D_h or D_p (μm)	Flow rate (ml/min)	R_θ ($^\circ\text{C}/\text{W}$)	Coolant	Mode
Agostini et al. [54]	Silicon back-side etch (Die-level)	122	490	0.013	R-236fa	Two-phase
Tuckerman and Pease[27]	Silicon back-side etch (Die-level)	92	516	0.1	Water	Single-phase
Sarvey et al.[267]	Silicon back-side etch (Die-level)	(P) 30	100	0.33	Water	Single-phase
van Erp et al.[56]	Silicon back-side etch (Die-level)	166.7	60	0.43	Water	Single-phase
Kong et al.[58]	Precision machining on copper	(P) 400	66	0.53	Water	Two-phase
Liu et al.[58]	Fabrication on a copper block	(P) 445	953.75	0.88	Water	Single-Phase
Peles et al.[57]	Silicon back-side etch (Die-level)	(P) 100	3.2	~5	Water	Single Phase
This work (1)	Package-level	615.38	118.8	1.22	Water	Single-Phase
This work (2)	Package level	(P)1000	155	0.90	Water	Single Phase

Chapter 7: Conclusion

7.1.Package-Level Thermal Management

This study demonstrates the potential of utilizing metal additive manufacturing for creating electronic packages with thermal management. These packages are designed as modifications of current packages made by stamping or etching, making them compatible with existing processing methods. The package can be customized with the desired number of leads for connection to the die. Microfluidic structures can be added beneath the die location to introduce embedded package-level thermal management. The effectiveness of these cooling structures depends on several parameters, such as hydraulic diameter, hydrodynamic features, flow rates, and coolant phases. By properly considering these design parameters, competent package-level thermal management can be introduced to electronic packages.

In conclusion, the concept of additive microfabrication of System in Package (SiP) with embedded thermal management of semiconductor dies has emerged as a promising solution for package-level integration with System on Chip (SoC). These SiPs have been designed to be smaller in size and offer lower thermal resistance as compared to the currently available system-level heat sinks. Additionally, they perform at a level that is comparable to die-level thermal management systems but without the high cost and complexity that is often associated with the latter. This innovative technology has the potential to revolutionize the field of semiconductor packaging by offering a more efficient and cost-effective solution for thermal management.

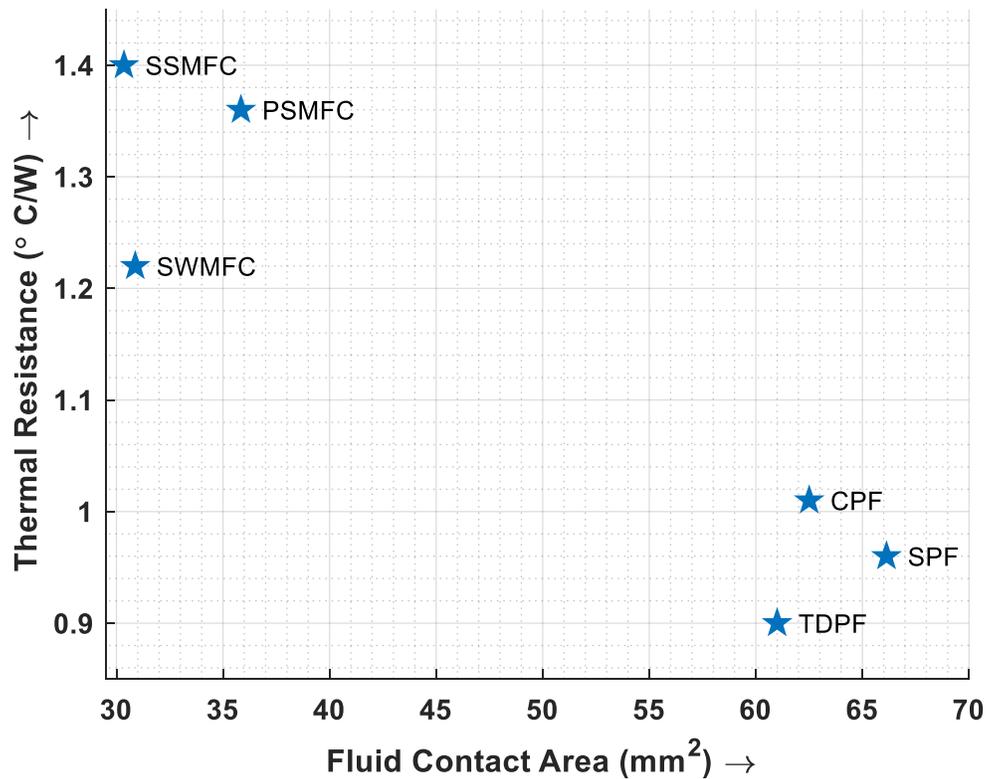


Figure 7.1. Comparative study of all the six different packages with different microfluidic structures indicated by the abbreviated texts besides each data point with respect to the total fluid contact area with the backend of the die.

7.2. Comparison of different microfluidic structures

The dissertation focuses on two main microfluidic structures: microfluidic microchannels and micro pin-fins, along with their optimized designs. Based on the preceding chapter's findings, it has been determined that the different variations of micro pin-fins have proven to be superior when compared to their microchannel counterparts. The apparent reason for this is the convective heat transfer contact area. This is well illustrated in Fig. 7.1., where the total convective heat transfer contact area of microchannel structures is about half that of the micro pin-fin packages. Due to the limitation of printer resolution, the design of microfluidic microchannel structures had

to be adjusted to avoid channel fusion by reducing the area of fluid contact. If similar hydraulic diameter and fluid contact area can be realized, these two structures might perform in an almost similar manner. As seen in Fig. 7.1., the package with hydrodynamically optimized microfluidic channel performed a lot better thermally compared to the other microchannel structures and would be similar in heat efficacy to the microfluidic pin-fins if similar coolant contact area could be designed. However, from this study, it can be concluded that for a certain resolution of the laser light used in the metal microfabrication, the micro pin-fins designs are more optimized and perform better compared to the microchannel.

7.3.Contributions of this work

This work presents one of the initial works done in the field of package-level thermal management. A complete SiP with embedded thermal management has been proposed in this work. This work made it possible to reduce the thermal resistance of a complete die and package combination from $5.25^{\circ}\text{C}/\text{W}$ for a conventional package to $0.9^{\circ}\text{C}/\text{W}$ for an optimized tear-drop pin fin microfluidic package. An overall of around 83% decrease in thermal resistance was seen between a conventional and TDPF package with water as flowing fluid. Different optimized structures were also studied in this dissertation. It has been determined that there are two forms of optimization possible for this kind of microfluidic device, hydrodynamic and hydraulic. The hydrodynamic optimization of microfluidic channels from serpentine straight to serpentine wavy increased the flow rate by around 11% consequently decreasing the thermal resistance by 13% for the same pump power. The hydraulic as well as hydrodynamic optimization of the micro pin fin package from circular pin fin to tear-drop pin fin increased the flow rate by 5% hence decreasing

the thermal resistance by 11%. The optimized microfluidic pin-fin package had a thermal resistance, which was around 26% lower than the optimized microfluidic channel. In summary, the introduction of microfluidic cooling structures was demonstrated in this dissertation. The introduction of thermal management in the packaging domain will open new avenues for the development of the packaging industries. The use of metal additive microfabrication addresses the HIR's call for heterogeneously integrated SoCs and SiPs. Also, the use of metal additive microfabrication reduces the strains in chip manufacturing in terms of microfluidic cooling systems designs as performed in die-level thermal management. This cutting-edge technology has the potential to transform the field of packaging industries, as it offers a superior solution that can effectively eliminate the drawbacks of as well as eradicate the use of suboptimal system-level thermal management techniques which take up most of the space of our present devices like computers and laptops. Nevertheless, this work can also serve as a foundation for optimizing microfluidic structures in thermal management at the die-level. With proper design and fabrication parameter optimization, and with the higher customization possibilities with additive manufacturing, this technology can be a complementary or competitive fabrication technology to the cleanroom processes.

7.4.Possible Future Work

The present study is a pioneering work in the domain of packaging and thermal management. It highlights the introduction of thermal management in the packaging field, which is a crucial aspect of modern-day electronics. The study holds great potential for further research and development. One of the areas that require optimization is the resolution of the printer used in the study. By decreasing the laser spot size, the printer can fabricate smaller microchannels and micro pin-fins, which would result in a reduction of the hydraulic diameter. This, in turn, would

improve the thermal management effectiveness of the packages. The use of finer metal powder as a precursor powder would also help enhance the resolution of the microfluidic structures. In addition to this, adaptive design of optimized microfluidic structures beneath the expected hotspots could further enhance the thermal management of the packages. This approach could ensure that the heat generated at hotspots is efficiently dissipated, thus preventing the overheating of the electronic components. Moreover, these metal packages could also serve as a shield against different types of radiation, such as beta radiation and heavy ion radiation. This aspect makes them highly valuable for use in space and other high radiation environments. Overall, this work lays a strong foundation for future research and development in the domain of packaging and thermal management. The findings of this study could be crucial in the development of more efficient and reliable electronic systems in the future.

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Appendix

Publications:

1. **(J)** Metal Additive Microfabrication of System-in-Package with embedded microfluidic thermal management for Heterogeneous Integration with Semiconductor Dies (**Published** by the Journal of Electronic Materials-2022)
2. **(J)** Dielectric Transfer Process for 3D Printed Metal Microsystems (**Published** by Journal of Microelectromechanical Systems-2020)
3. **(C)** Metal Additively Microfabricated SiPs with Embedded Microfluidic Cooling Towards Heterogeneous Integration with SoCs (**Published** by the 73rd Electronic Components and Technology Conference (ECTC)-2023)
4. **(C)** Metal Additive Microfabricated Microfluidic Packages for Integrated Thermal Management In Power Application (**Published** on 21st International Conference on Micro and Nanotechnology for Power Generation and Energy Conversion Application (PowerMEMS)- 2022)

5. **(C)** Additive Microfabrication of System in Package for Heterogeneous Integration with Semiconductor Dies (**Presented** at The 64th MRS Electronic Materials Conference (EMC)-2022)

6. **(C)** Additive Batch Microfabrication of 3D Metal Electrostatic Switched Towards 3D Printed Metal MEMS (**Published** at the Hilton Head: Solid-State Sensor, Actuator and Microsystems Workshop (Hilton Head)-2022)

Vita

Bhushan Lohani completed his Bachelor of Technology in Electronic and Communication Engineering from Jawaharlal Nehru Technology University in 2014. He completed his Master of Science in Electrical and Electronic Engineering from The University of Texas at Tyler in 2018. He joined The University of Texas at El Paso in the Fall of 2019.

Bhushan has worked as an Electrical Maintenance Engineer at the Upper Madi Hydropower Company Limited during the period of 2015 till the end of 2016. He then started as a Teaching Assistant, conducting labs and lectures for several courses like Linear System Analysis, Real-Time Systems, Digital Communications, Microprocessors, Electronics I and II, Electric Circuits and Introduction to Electrical and Computer Engineering. During the period from 2021 to 2023 he was assigned as the Assistant Instructor for the course of Introduction to Electrical and Computer Engineering teaching basic concepts to freshmen engineering students.

Contact Information: blohani@miners.utep.edu