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Development Of A Mems Fabrication Process On Soi To Study High Strain In Transition-Metal Dichalcogenides

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DEVELOPMENT OF A MEMS FABRICATION PROCESS ON SOI TO STUDY HIGH STRAIN IN TRANSITION-METAL DICHALCOGENIDES

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Dedication

I want to dedicate this work to my fiancé, my family, and specially Dr. Zubia for all the support and advice during this journey.

DEVELOPMENT OF A MEMS FABRICATION PROCESS ON SOI TO STUDY HIGH STRAIN IN TRANSITION-METAL DICHALCOGENIDES

By

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THESIS

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Abstract

Over the recent years there has been an increasing demand of better performing electronics. However, as the semiconductor industry keeps on improving and scaling the technology to the nanometer regime, the passive power density has overcome the overall power consumption of transistors. The inability to reduce the power alongside the scaling of transistors has led the scientific community in the search for alternatives or different solutions to overcome this power crisis. The use of two-dimensional Transition-Metal Dichalcogenides (TMDCS) and Micro-Electro-Mechanical System (MEMS) actuators, in conjunction, has been proposed as an alternative solution [1]. Recent studies of TMDCS have shown a very promising potential for future use in electronics. One very interesting property in particular of TMDCs is that they are highly sensitive to strain [2, 3]. On the other side, MEMS offer excellent on/off ratios with very steep transitions as it has been demonstrated in [4, 5, 6, 7, 8]. Devices, which exploit the bandgap tunability of the TMDCs to enhance their conductivity, have not been explored thoroughly. As a result, a MEMS device that takes full advantage of the TMDCS strain properties has been proposed, and shown a potential future for electronic devices [1]. Furthermore, such a device needs a reliable, reproducible, scalable, and ability to offer a promise for future research. In this thesis, the effort to design, fabricate, and characterize a double anchor beam actuator will be discussed. This work is an important footstep to understand, analyze, and promote the simplification of the fabrication processes involved in a research environment, as well as, the use of Silicon On Insulator (SOI) for this type of application. Finally, this work developed a MEMS fabrication process at UTEP's Nanofabrication Facility for the first time.

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Chapter 1: Introduction & Motivation

Electronic devices have changed our lives significantly over the last seven decades. Over this time, the research community has continually scaled the devices to smaller dimensions by studying the amazing properties of complementary metal oxide semiconductors (CMOS) and developing new processes. Thanks to the enormous effort of the industry, it has fulfilled Moore's Law over the past several decades [9]. Although this technology development has opened a new world of possibilities in device performance, these same technologies are reaching some fundamental limits and creating completely new sets of challenges for engineers to overcome. One of the major challenges is the increased power consumption in highly scaled devices. Several approaches are being investigated by the research community to address this problem. One approach is to use nanoscale-sized micro-electro-mechanical-systems (MEMS) since they have the potential to reduce standby and dynamic power dissipation and established processes can be used to fabricate MEMS switches.

This thesis focuses on the MEMS approach and describes the design and fabrication of a MEMS actuator on silicon-on-insulator (SOI) substrates to strain thin layers of transition-metal dichalcogenides (TMDC). The motivation for straining thin TMDC layers with a MEMS actuator is to make an electronic switch [1, 10, 11, 12] with lower energy consumption and lower turn-on voltage compared to a metal oxide semiconductor field effect transistor (MOSFET). This thesis describes the development of the major processes needed to make a MEMS actuator on an SOI substrate.

1.1 The limits of current CMOS

The rise and integration of transistors has revolutionized modern electronics. This revolution started in the late 1950s due to the invention of the resonant transistor [13].

Additionally, the famous "There is plenty of room at the bottom" seminar by Dr. Feynman inspired researchers to push innovation to the nanometer regime. Furthermore, the push for planar silicon processes [14, 15] to fabricate integrated electronic circuits created an exponential growth in our daily electronic devices. This technological success is the foundation of the continual advancements in the performance of electronic devices.

The success of scaling down transistors created huge new opportunities for other related fields and industries such as: the introduction of smart phones, machine learning, and cloud computing. Consequently, scaling down transistors created accelerated growth in demand for semiconductors and electronics as shown in Figure 1. As electronics started becoming a part of our daily routines, the sales of electronics significantly increased and surpassed the sales of automobiles in 2000. In addition, the general semiconductor industry surpassed the steel industry in 2010 with nearly $400 billion in sales. The growth in sales occurred as a result of scaling and the ability to pack more transistors into a single electronic die.

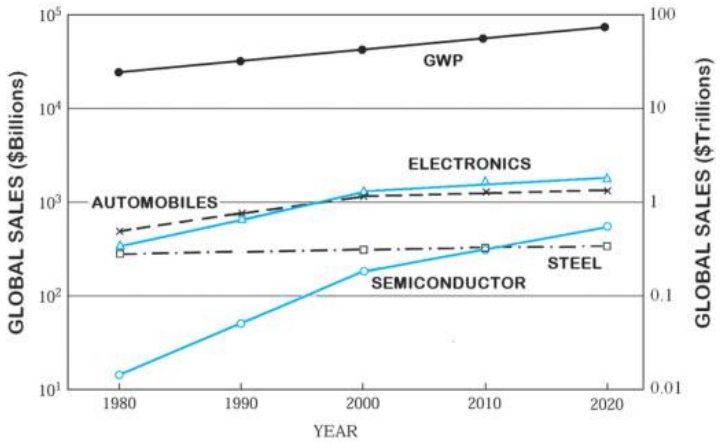

Figure 1. Volume sales of electronics, automobile, semiconductor, and steel industries from 1980 to 2000 and projected to 2010 [16].

The size of transistors is still being aggressively reduced each year. For example, although it was estimated that the 10 nm scale would be reach in 2020 [16], it was actually reached sooner

than predicted. There is current work being done in the sub 10-nm regime, and technology is still being developed to scale down even further. However, as the density of transistors increases by reducing their size, leakage current and heat dissipation has become a major problem [17].

As the number of transistors in use around the world increases, the percentage of electricity needed to power the devices is also increasing, and this is creating a global energy consumption problem. This issue leads to huge power consumption that provokes a big concern in today's modern world where it is structured by cloud computing, mobile internet, and data analytics. At the core of this problem is the fundamental operating principle of MOSFETs and the energy consumed by the devices in both standby and switching operation.

MOS transistors are known to work as electrical switches, by applying a voltage difference between gate and source (V_{GS}), permitting it to turn on at a threshold voltage (V_T) [18]. One possible solution to reduce the active power consumption is trying to reduce its threshold voltage. Turning the transistor ON at a lower voltage, translates to less voltage required to charge and discharge the wires that interconnect transistors and therefore less power consumption. Although this sounds very promising, it comes with its own limitations. One of the limitations of CMOS technology is its theoretical minimum subthreshold swing (SS) of 60 mV/dec governed by the Boltzmann constant and the thermal limit kT/q [19]. However, with a swing of 60 mV/dec a voltage of 360 mV (60 mV/dec × 6 decades) is needed to have an on/off current ratio of six decades (10^6). The SS, as shown in Figure 2, can be observed to be gradual and not abrupt. This SS is a key parameters for power consumption, and the necessity to reduce the swing has become one of the most challenging technological issues [20]. Moreover, by simply reducing V_T, it creates the effect of exponentially increasing the leakage current (I_{OFF}) which is set by non-scaling physical constants [12] as described by the relation,

$$I_{OFF} \propto 10^{\frac{-V_T}{SS}} \tag{1}$$

Where I_{OFF} is not equal to zero when the voltage between gate and source (V_{GS}) is zero (as seen in Figure 2). Physically, as the transistor is scaled down, its dimensions become smaller, thus, reducing the channel length and its oxide thickness, promoting the increase of I_{off} due to short channel effects and charges trapped in the oxide. Therefore, the MOSFET transistor cannot be completely turned OFF.

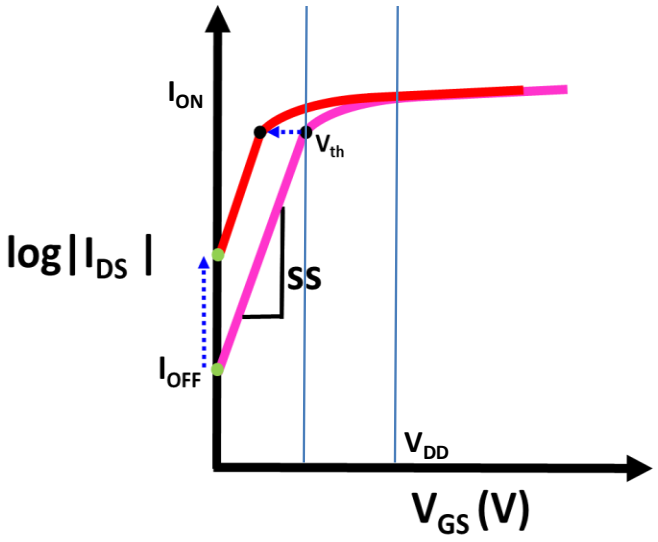

Figure 2. Semi-log plot of a characteristic I-V curve of a CMOS transistor [12].

The net effect of scaling CMOS devices down is that it contributes to an increase in the passive power consumption through leakage current. This can be observed in Figure 3 where the passive power has increased faster than the dynamic power as devices were scaled down. In the 10 nm regime, the passive power is essentially equal to the active power dissipation.

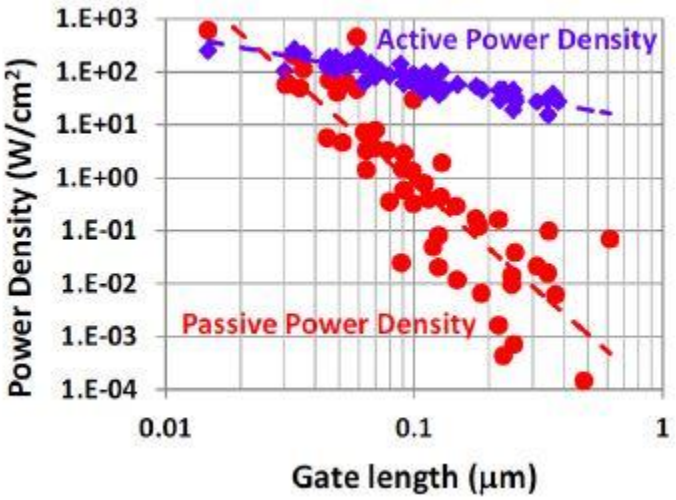

Figure 3. Active power vs passive power comparison as gate length decreases [17].

Hence, the scientific community and industry have been looking into different ways to tackle this problem. An approach to maintain low standby power dissipation is to keep an on/off current ratio of six orders of magnitude (10^6) [12]. This will ensure that very little leakage current will flow when a device is in the "off" state to reduce passive power consumption. In contrast, a large portion of dynamic power dissipation is attributed to the charging and discharging of interconnecting metal lines in integrated circuits. For example, a reduction in the "turn on" voltage from 360 mV (minimum for CMOS) to 3.6 mV translates to a reduction in power consumption of 10^4 since power scales as V^2! Some of the promising approaches to achieve high on/off ratios and low turn-on voltage are nano-mechanics, nano-photonics, nano-magnetics, and nano-electronics [21]. All these approaches have pros and cons, however a highly attractive aspect of nano-mechanics is that CMOS processing technology can be used to create integrated MEMS switches with on/off ratios greater than 10^6. Moreover, MEMS switches can be interconnected to make logic gates. However, the issues with MEMS switches are their high turn-on voltage and low endurance due to degradation of the contact. The focus of this thesis is the development of a MEMS process

to fabricate a new switch that was recently proposed to operate at low voltages (10 mV) and achieve a high on/off current ratio (10^6).

1.2 MEMS IN A TRANSISTOR WORLD

The study of Kurt Peterson to understand the capabilities of silicon as a mechanical material [22] spurred research into studying the use of silicon as a mechanical structure itself. In addition, in 1983, some of the first micromechanical beams were fabricated utilizing MOS planar process [23]. This opened the road for MEMS. Over time, fabrication techniques have become more sophisticated and optimized providing the ability to fabricate MEMS more efficiently. Nowadays, MEMS have a wide variety of applications such as micro sensors, accelerometers, optoelectronics and digital logic [8, 4]. MEMS are very promising due to their ability to use the same fabrication procedures developed for CMOS technology and its capability to work in conjunction with other electronic devices [19].

1.2.1 MEMS as Switches

Electronic switches can be made from MEMS very similar in operation to MOSFETS which have 4 terminals; namely the gate, drain, source and body electrodes. This similarity can emulate and relate to the operation of a MOSFET by applying a voltage difference between the gate and source attracting the source (being the movable part) to the drain (being anchored) as shown in Figure 4 [24]. Figure 4 shows a schematic of a MEMS switch with 3 of the 4 terminals. The principle of operation is that an electric field between the source and gate (due to V_{GS}) causes a flexible beam (source) to bend down until it contacts the drain electrode. This causes the switch to turn on. Recent MEMS research has focused on making logic relays and gates similar in operation to CMOS logic gates. One aspect of this research is to make switches and gates for low-voltage applications as seen in [4, 5, 6, 7]. Referring to Figure 4 again, a fourth terminal (body electrode) would exist next to the gate to act a DC biasing electrode to pre-bend the beam. The

effect of pre-biasing is to reduce voltage needed at the gate (V_{GS}) to turn on the switch. The electrostatic behavior of MEMS has been improved over the last decade by making them more reliable, improving the effective stiffness by designing different spring architectures, improving adhesion forces between the contact electrodes by implementing different contact materials, and creating fabrication processes compatible with CMOS technology, making this a promising alternative [8, 24, 25, 26].

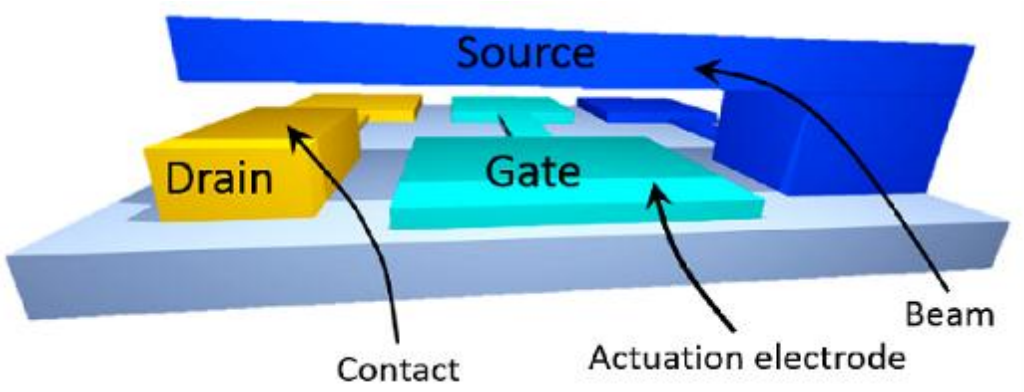

Figure 4. Cantilever Beam MEMS design concept with its different electrodes and structural names [24].

MEMS switches possess several properties that make them very attractive for low power applications. They present zero leakage current, very steep ON/OFF ratios, low actuation voltage [13-19]. For example, a characteristic I-V curve of 4 terminal device designed and fabricated at UC Berkeley for low-voltage applications is shown in Figure 5 [5]. An abrupt switching can be observed, having a subthreshold swing of ~33.33mV/dec, demonstrating a lower swing than current CMOS technology.

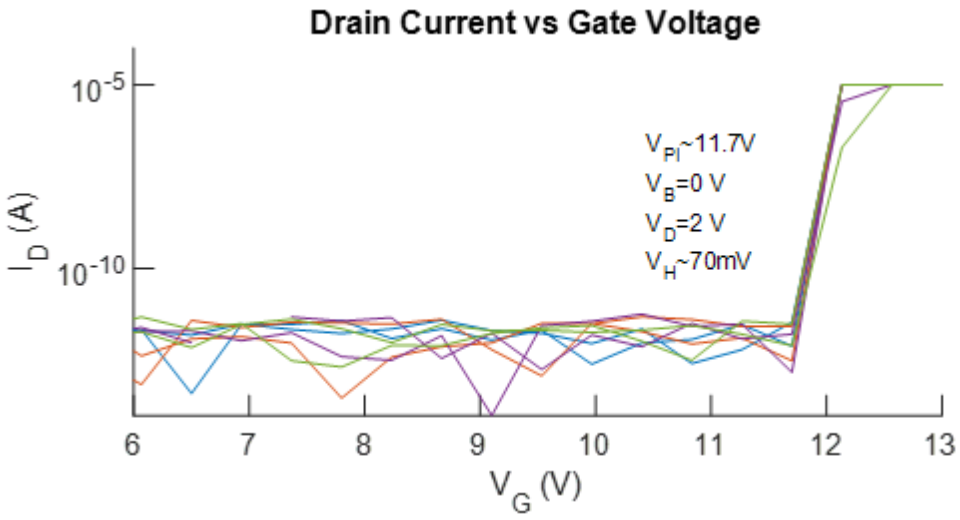

Figure 5. I-V characteristic of a N/MEMS acting as a switch.

Although the subthreshold swing is low, the turn-on voltage is still very high (V_{PI} = 11.7 V). The architecture of the N/MEMS is shown in Figure 6. The 4 terminal device takes advantage of the parallel plate capacitor electrostatic model, and by using flexed structures to actuate out of plane. By applying a body bias voltage (V_B), the V_{PI} can be reduced. Using the parallel plate concept, the V_B will attract the body structure to the substrate reducing the actuation gap, therefore the a reduction in V_{PI}

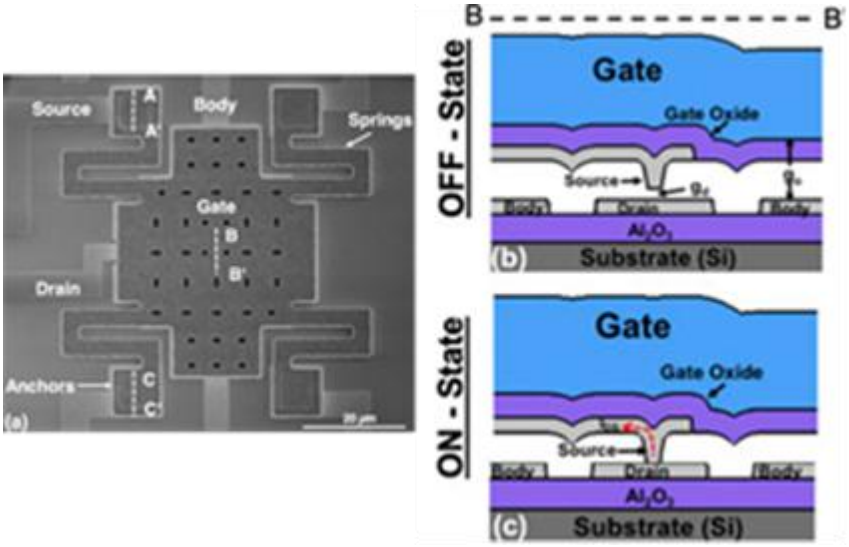

Figure 6. (a) SEM Image of 4 Terminal MEMS design concept, (b) cross-section of B-B' showing source and drain in off state, (c) and showing the contact mechanism between drain and source in the on state [27].

However, MEMS have their own limitations. For example, limited endurance, limited to their pull in gap ratio, and stiction. This last one is a big challenge [25, 26], since the adhesion forces become larger than the spring restoring force, giving rise to problems like hysteresis as observed in Figure 5, where a 70mV hysteresis exists. As promising MEMS are for switching applications, different approaches are being explored to overcome some of the aforementioned issues. Amongst these approaches are the use of molecular coatings, known as Self-Assembled-Molecules (SAM), to reduce the adhesion force [27], and utilizing different designs and materials to improve their performance [5, 6].

1.3 Transitional Metal Dichalcogenides in 2-Dimensions

Ever since the introduction of graphene as a 2-D material, there has been a large interest into studying other 2-D materials. One huge motivation for studying other 2-D materials is that graphene does not have a bandgap and this has limited its application. As an alternative, extensive work has been done to study the electrical, optical, mechanical, and material properties of Transitional-Metal Dichalcogenides (TMDCs) [28, 3, 29, 30, 31, 2]. One of the advantages of these TMDCs is that they have a bandgap, permitting the scientific community to utilize these materials as sensors, FET devices, and photovoltaic applications [3, 32, 2, 33].

Several TMDCs have been studied and discovered. Amongst these TMDCs, molybdenum disulfide (MoS_2) is one of the most studied materials. These TMDCs consist of a sandwich like structure, as seen in Figure 7, where a metal atom is in between two chalcogenide atoms [3, 29]. The atoms within each layer (or sheet) form strong covalent bonds. In contrast, the bonds between sheets are made of weak van der Waals interaction. This difference in bonding strengths within and across sheets permits the extraction of single atomic layers [3].

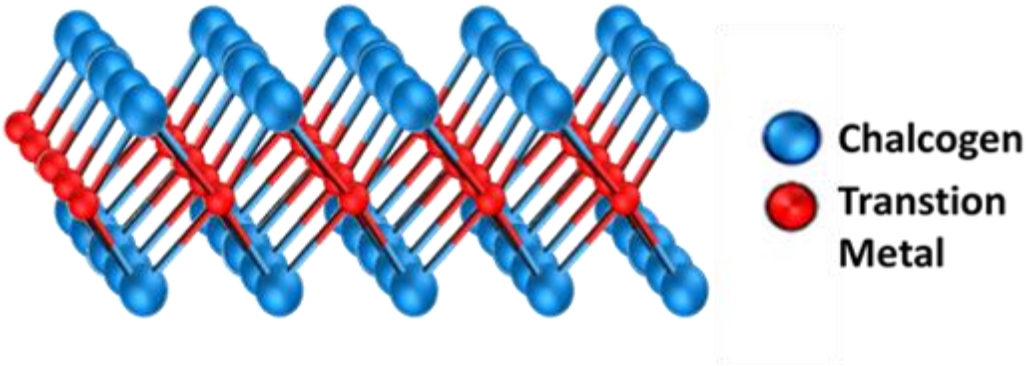

Figure 7. TMDC monolayer showing sandwich-like structure of transition metal in between chalcogen atoms.

One particular property, called "deformation potential", has attracted great interest. This property consists of a linear change of the band gap due to mechanical strain. In the case of MoS_2, as tensile strain is applied in the planar direction, the distance between atomic layers is reduced, and for a 2L MoS_2, where there are two Mo planes, there is a stronger interaction between its d_z^2 orbitals [31], causing the reduction of its bandgap and increase of conductivity. This bandgap vs strain behavior is shown in Figure 8. Work like [31, 30, 3] have shown some of the relationships between its mechanical and electrical properties, as well as its fractural point.

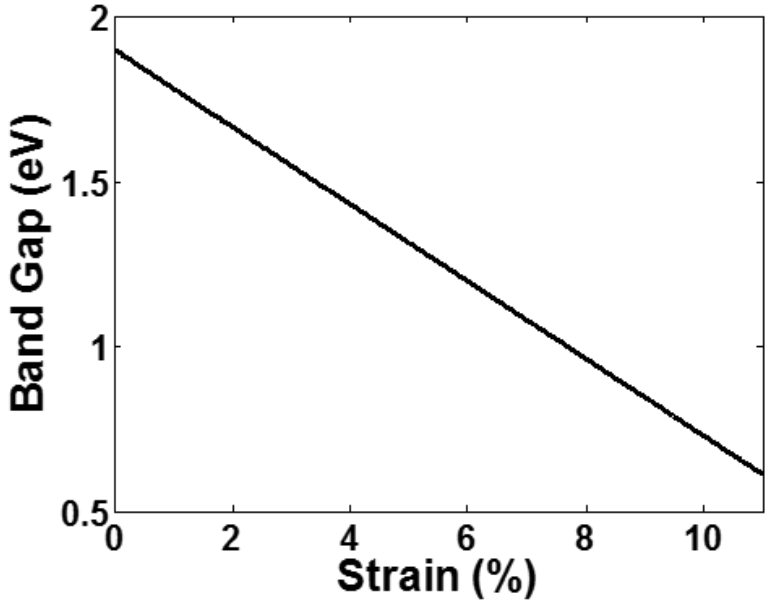

Figure 8. Linear relationship between tensile strain and band gap change for MoS_2 [12].

The property of deformation potential opens the opportunity to explore various applications like flexible electronics, strain-engineered sensors, photovoltaic applications, and switching

applications [1, 10, 28, 3, 2, 29]. A linear reduction in the bandgap leads an exponential increase in conductivity of the 2-D materials [12, 11, 10, 34]. From Figure 9, it is observable that a 6 orders of magnitude increase in conductivity can be achieved by applying ~6% strain to a bi-layer MoS_2 flake. This property then becomes very attractive to use 2-D materials as switches by applying and releasing the strain to modulate the conductivity by a factor of one million. Due to their small size, a MEMS actuator is a natural device to strain a 2-D material and investigate the possibility of making a low-voltage, low-power switch.

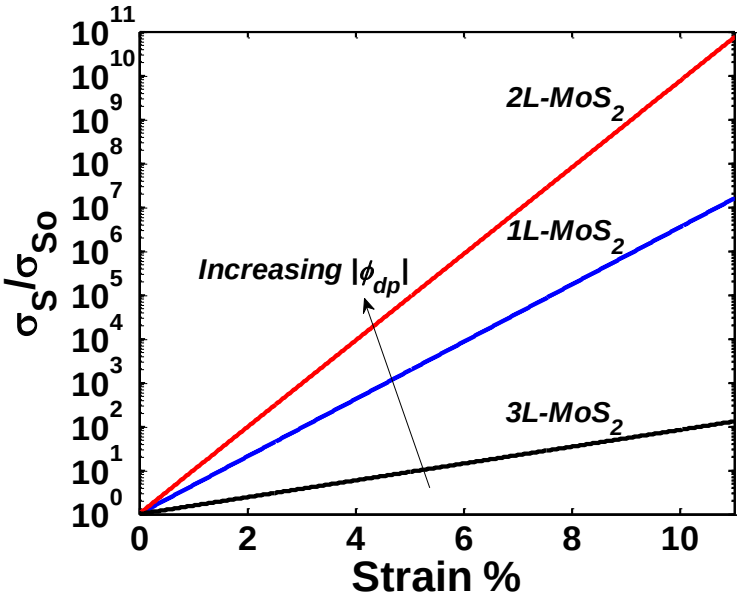

Figure 9. Conductivity ratio for different MoS_2 layer as a function of strain [12].

1.4 The TMDC-MEMS Switch

To address the high-voltage and low-endurance issues related to MEMS switches, a new device was proposed with combines the electromechanical behavior of MEMS with the deformation potential property of TMDC's as shown in Figure 10. This combination of MEMS-TMDC has been proposed for ultra-low power applications [1]. The device can be modeled similarly to a transistor with electrodes the have analogous functions such as the gate, drain, and source. In this device, a thin TMDC layer is clamped between the drain and source. When a voltage is applied to the gate, the TMDC is strained causing an exponential increase in its conductivity.

One of the advantages is this device is that it can be designed and fabricated in such a way that the strain applied can be controlled via electrostatic force, thus facilitating the study of the electrical properties of materials under tensile strain. By applying an electrostatic force, the MEMS will uniaxially strain the TMDC, linearly reducing its band gap, and in turn exponentially increasing its conductivity.

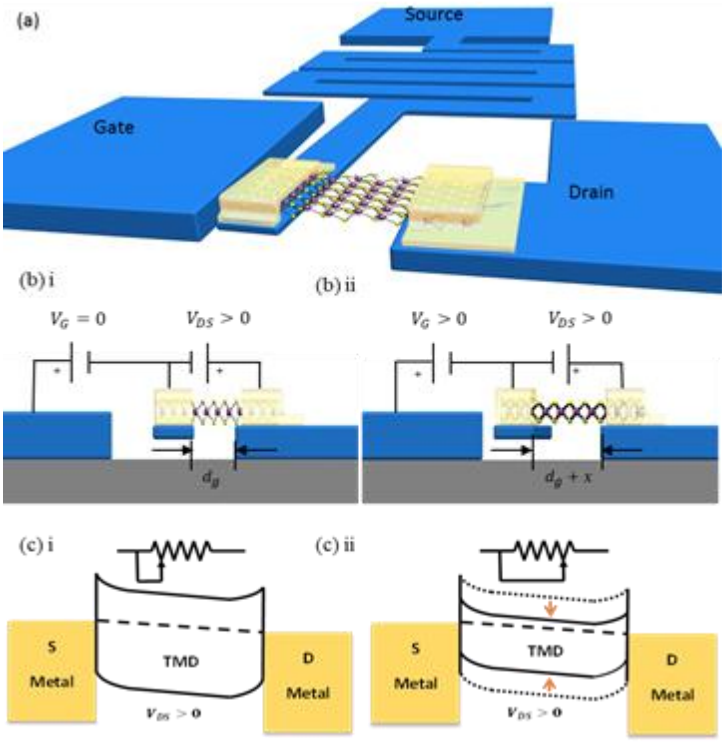

Figure 10. (a) Isometric view of the device, (b) cross-section view of off and on, and (c) representation view of the device at Off and On state respectively change [12].

As a proof of concept, MEMS-TMDC switches using simple cantilevers were fabricated and tested. The conductivity ratio (σ_S/σ_{S_O}) versus gate-to-source voltage (V_{GS}) characteristics of two experimental switches are shown in Figure 11 [1]. The switches were tested by applying a constant V_{DS} of 200 mV, and sweeping V_{GS} from 0-28 V and 0-31.5 V for each device, respectively [1, 12]. The strain in the TMDC was calculated to be up to 2.7% using the following relation,

$$\varepsilon = \frac{-\ln(\sigma_S/\sigma_{S_O})2kT}{\phi_{dp}}. \quad (2)$$

Although the turn-on voltage of the MEMS-TMDC was high (~30 V), and the conductivity ratio was ~600, the results were very encouraging because they demonstrated an exponential increase in conductivity. Moreover, the MEMS actuator used in this experiment was not optimized for this application but was simply a MEMS cantilever actuator that was readily available for proof-of concept experimentation. Figure 11 also shows the theoretical characteristic curves of a MOSFET and an optimized MEMS-TMDC switch. Notice the steeper subthreshold swing of the MEMS-TMDC device compared to the MOSFET. The turn-on voltage of a scaled MEMS-TMDC switch is predicted to be 70 mV compared to 360 mV for the MOSFET.

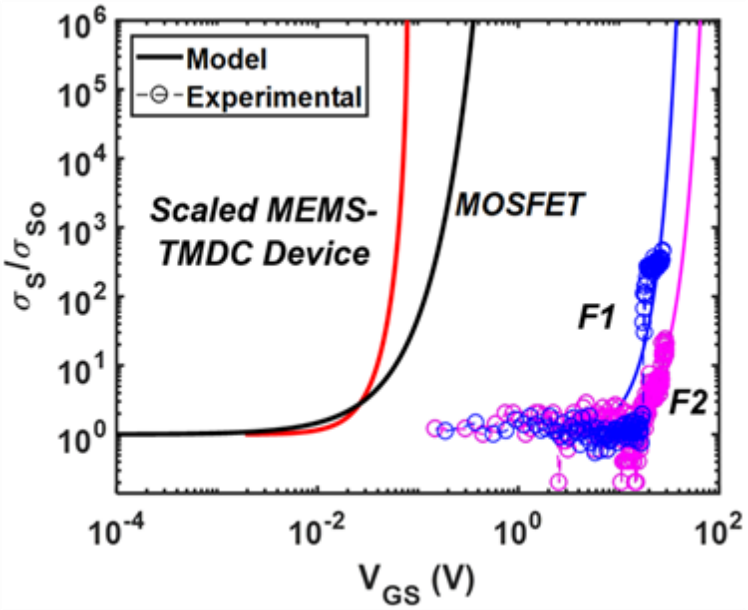

Figure 11. Measured 1st generation cantilever devices (circles) and theoretical TMDC-MEMS comparison to MOSFET [12].

Encouraged by the proof-of-concept results, a second generation MEMS-TMDC switch was designed, fabricated and tested with the goal to achieve larger conductivity ratios. The 2nd generation comb-drive actuator was proposed to overcome some of the instability issues of the previous 1st generation cantilever design, as well as, considering the large actuation capabilities that comb-drives can achieve trying to meet the 6% strain goal. A poly-SiGe comb-drive actuator was fabricated and tested. Figure 12 shows some of the experimental results of the 2nd generation

comb-drive actuator with the TMDC integrated into the device. Although the 2nd generation comb-drive device achieved a ~3% strain which is a world record, it is only incrementally better results compared the 1st generation cantilever approach. The reasons for not achieving high strain were attributed to issue associated with the design and fabrication the comb-drive. One major problem was residual stress from the poly-SiGe structure, bending the comb-drive fingers creating the inability to actuate in the desirable in-plane mode. Instead, the large area that the substrate creates with the structure was taken into advantage to actuate the device in out of plane and this geometrically limited the degree of strain to 3%.

In addition to the performance issues of the MEMS device, there were other issues hindering research progress. One of the issues was that the poly-SiGe comb-drives where fabricated at UC Berkeley making it expensive and time consuming due to traveling and high costs for the fabrication. Secondly, because of the complexity the comb-drive design presented, low yield was observed, which created a low throughput in the results that could be obtained. As a consequence of these issues and taking into account the goal shown in Figure 12, a new MEMS design approach had to be implemented.

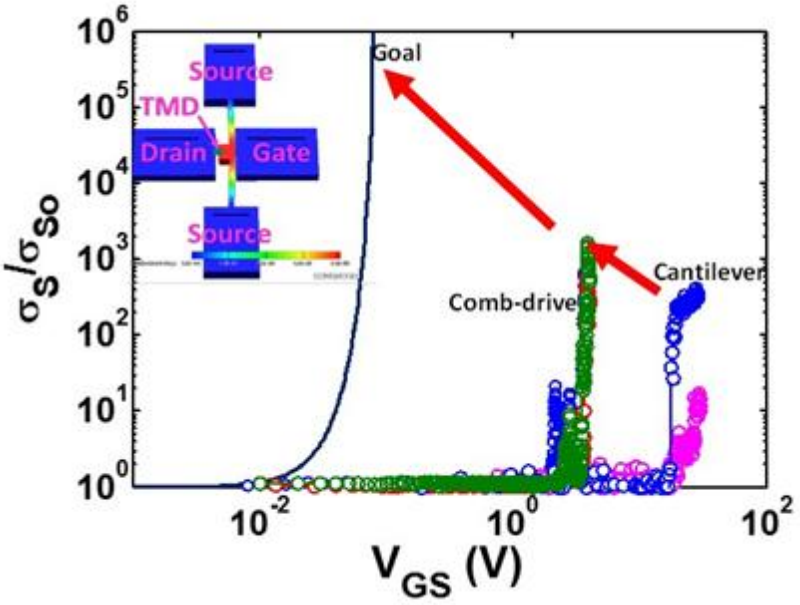

Figure 12. Comparison between 1st generation cantilever, 2nd generation comb-drive actuator results, and 3rd generation double-anchor desirable goal [12].

This became a very important goal to meet for the research. By fabricating the TMDC-MEMS devices at UTEP, it would allow the team to reduce the cost of fabrication, and the time required to obtain the devices. In addition, by developing a proper fabrication process, a higher yield could be obtained, and consequently providing a higher throughput in the results. However, in order to meet all these goals, understanding the fabrication capabilities available at UTEP had to be taken into account. Of equal importance, a simple design had to be proposed, where the team could avoid as much issues as possible for the fabrication development. Keeping the device simple would also contribute to have a scalable design that would eventually meet the desirable goal as the fabrication technologies improved. All the issues associated the design and fabrication of the 2nd generation comb-drive are shown in Table 1. Considering the previous successes and issues, a decision was made to transfer and develop a MEMS fabrication technology at the University of Texas at El Paso.

Table 1: Primary issues encountered from previous TMDC-MEMS generations

Issues
Expensive
Time Consuming
Complex Design
Low Yield
Low Throughput

The result of this analysis is the 3rd generation double-anchor MEMS design shown in Figure 13. The design consists of a long flexible silicon beam anchored at both ends. An electrostatic force is applied in the middle of the beam to deflect it. Finally, a TMDC is clamped across a fixed (gate) electrode and the middle of the beam.

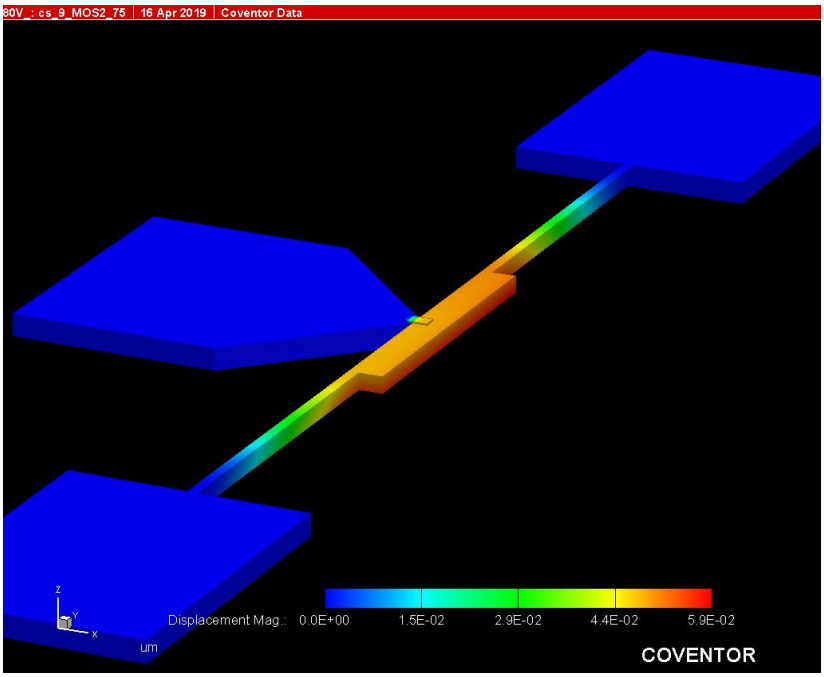

Figure 13. New design simulated using Coventorware software to show functionality of the device, omitting gate electrode for computational purposes.

1.5 Contribution of This Thesis

The contribution of this thesis is the development of a process to fabricate the 3rd generation double-anchor MEMS device. The thesis also discusses key factors that are crucial for the proposed double-anchor switch. Amongst some of the key factors that will be discussed are the design considerations, including verification of simulation work, and the importance of selecting an SOI substrate. The design of a mask and the proper interaction with other materials is also discussed. This is followed by a discussion of the fabrication flow. Lastly, the process development that is needed to fabricate the SOI MEMS is discussed including; lithography, deposition, lift-off and plasma etching.

Chapter 2: Design Considerations

To meet all the proposed goals and overcome the issues from the previous generation TMDC-MEMS, a new design was proposed. This section will discuss some of the considerations for the design and its implementation for fabrication.

2.1 Analysis of Double Anchored Beam

Different MEMS designs exist and depending on the application, a certain design may be more suitable for a particular application. One of the most common designs which have found wide application are the cantilever beams. The cantilever beam has been fully analyzed and basic models have been developed which makes its analysis and functionality as simple as possible. For example, this structure can be examined using a movable plate capacitor, which is why it is a very attractive model for N/MEMS applications. One common method of operating the beam is by actuating the cantilever in the out-of-plane direction. In this method, a fixed gate electrode is used to attract a flexible beam (source) in the out-of-plane direction (usually down) until it makes contact with a fixed drain electrode. When the beam makes direct contact with the drain electrode, good electrical continuity is established between the source and drain. However, the out-of-plane actuation configuration makes it somewhat complicated to attach a 2-D material since it would have to be attached to the sidewalls of the source and drain. Fortunately, the 1st generation cantilever beam moved in the in-plane direction making it more suitable for attaching TMDCs using planar processing as was demonstrated in [1]. However, the 1st generation cantilever presented many fabrication and operation issues since it was not particularly designed to attach and strain TMDCs.

To address these issues, a double-anchored beam was then proposed considering that this design can still utilize some of the concepts of a single beam due to the fact that it can be modeled basically as two beams working in unison instead of one. This design permits to have more control of the actuation of the device and to simplify the structure where it becomes easier to analyze and fabricate. The double-anchor design is shown in Figures 13 and 14. In this design, the suspended

flexible beam will act as the source and the 2-D material is suspended between the drain and source. The gate electrode is used to attract the beam.

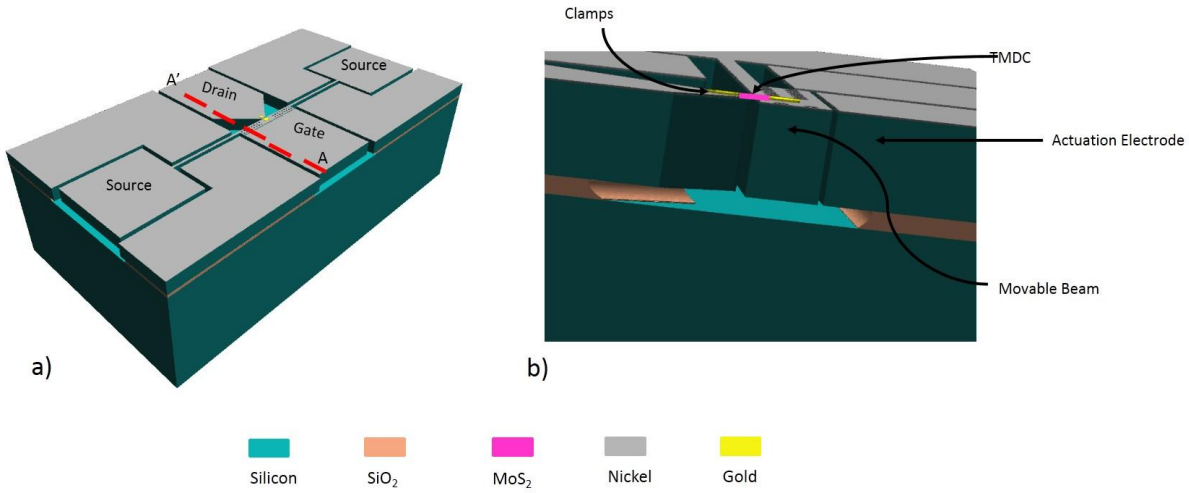

Figure 14. a) Double-anchored beam design and b) magnified cross-sectional view from A'A showing details.

A force balance model can be used to understand the static electro-mechanical relationship of a cantilever beam. Fortunately, the force balance model can also be applied to model the 3rd generation double-anchor design as depicted in Figure 15 by using the appropriate stiffness and restraining forces of the beam (F_{CAN}) and TMDC (F_{TMD}), the electro-static force (F_E), and the Van der Waals forces (F_{VW1}, F_{VW2}). The force balance equation is given as,

$$F_E = F_{CAN} + F_{TMD} + F_{VW_2} - F_{VW_1} \tag{3}$$

A very important characteristic parameter of this design is the distance between the drain and source (labeled as x_o) when there is no strain in the beam ($\varepsilon = 0$). This characteristic parameter is shown in Figure 15. Each force in Equation 3 can be expanded further to show the dimensional relationship of x_o on each force as follows,

$$\frac{\epsilon_o A V_{GS}^2}{2x_0^2(1-\varepsilon)^2} = k_{CAN} x_o \varepsilon + k_{TMD} x_o \varepsilon + \frac{HA_{VW}}{6\pi x_o^3(1+\varepsilon)^3} - \frac{HA_{VW}}{6\pi x_0^3(1-\varepsilon)^3} \tag{4}$$

where ϵ_o is the permittivity of free space, A is the actuation area between the source and the gate electrodes, k_{CAN} and k_{TMD} are the stiffness of the beam and TMDC, respectively, H is the Hamaker constant, and A_{VW} is the activation area for the Van der Waals forces.

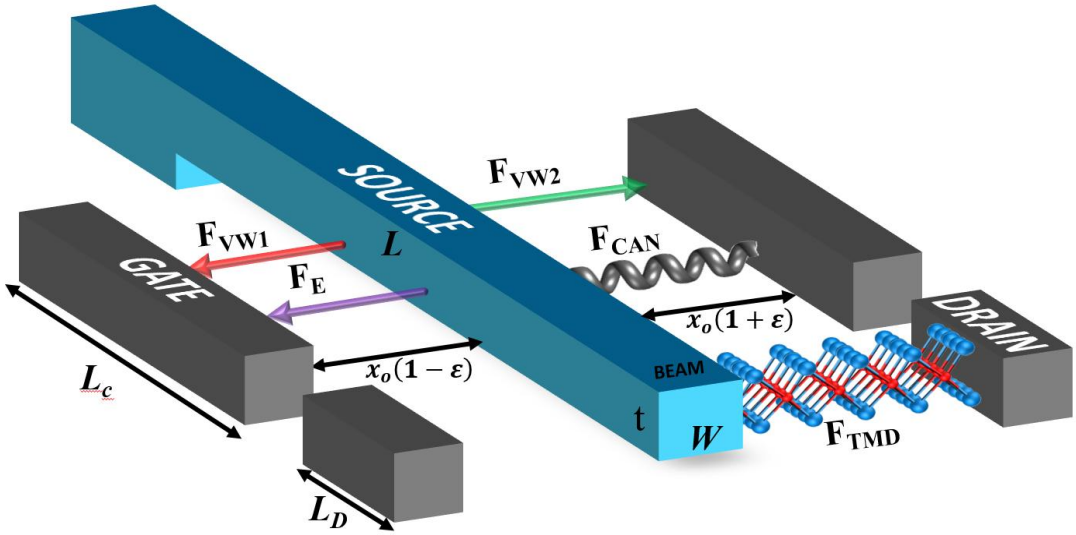

Figure 15. Force balance model for beam-TMDC concept showing all acting forces [12].

To use this device for low-voltage (low V_{GS}) application, the characteristic length x_o is reduced so that F_E is increased while F_{CAN} and F_{TMD} are decreased. These relationships are shown in Figure 16 where F_E (green trace), F_{CAN} (dotted black), and F_{TMD} (solid black) are plotted as a function of x_o. Interestingly, as the device is scaled down to $x_o < 15$ nm, the Van Der Waals forces start becoming significant. At this small scale, F_{VW1} assists F_E so that the voltage required to strain the TMDC (and increase its conductivity by six order of magnitude) is reduced to 72 mV [12, 34].

The previous analysis showed the importance of having a small gap size ($x_o < 15$ nm) to reduce the operational voltage to V_{GS} =72 mV. However, since the technology to achieve such small dimensions is presently not available at UTEP's nanofabrication facility, a very important aspect of the double anchor design is that it is scalable in the sense that x_o can be easily reduced overtime as the technology to print smaller features is developed at UTEP, or through collaboration with other research centers.

Even though the approach was to make a relatively large MEMS and then scale down over time, several constraints had to be met even at the larger size. One design consideration was that F_{TMD} needed be at least 10 times larger than F_{CAN} so that the voltage needed to strain the device was primarily for the TMDC and not the beam. This aspect of the design can be observed in Figure 16 where$F_{TMD} \geq 10 \cdot F_{CAN}$. This will ensure that the switching voltage will be minimal. Another constraint was that 4% strain needed to be achieved in the TMD at a voltage of 80 V or less. This meant that four orders of magnitude increase in the conductivity needed to be achieved with the application of ≤ 80 V. The voltage constraint was implemented for safety and due to the limitation of the Keithley 4200A-SCS parameter analyzer available for this research.

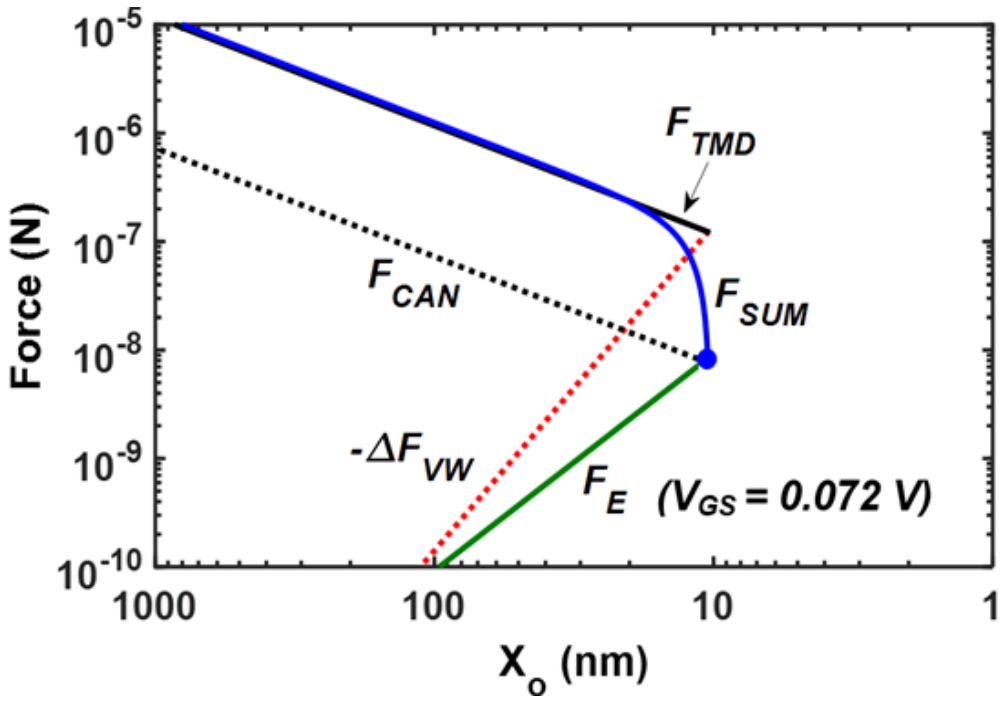

Figure 16. Forces in a theoretical MEMS-actuated TMDC switching device as a function of x_o at a tensile strain of ε=0.061 [12].

2.2 Calculation of MEMS Dimensions

All the design considerations and constraints listed in the previous section had to be taken into account to calculate the physical dimensions of a silicon-based MEMS to be fabricated at

UTEP's Nanofabrication Facility. Important physical dimensions as indicated in Figure 15 were the beam thickness (t), width (W) and length (L). These are important in establishing the stiffness of the beam. Equally important were the gaps (x_o) and actuation areas between the source and drain ($L_D \times t$), and the source and gate ($L_C \times t$). These are important for establishing the strength of the electro-static force as a function of voltage as well as the length of the TMDC.

A starting point of the analysis to determine the various dimensions of the MEMS actuator was the stiffness of the TMDC. This was determined by the chosen material's Young's modulus, thickness and size (length and width). The material selected was a MoS_2 bi-layer due to its large deformation potential as discussed in Section 1.3. The Young's modulus of 2L-MoS_2 is $E = 140 \times 10^9$ N/m^2. To determine the stiffness, the size of the 2L-MoS_2 flake was approximated to be 3 μm wide × 3 μm long based typical sizes of exfoliated flakes. Using Hooke's Law, this gives a stiffness of $k_{TMD} = 193.2$ N/m., which determined that $k_{CAN} \leq 19$ N/m to satisfy the requirement that$F_{TMD} \geq 10 \cdot F_{CAN}$.

Another very important constraint was the aspect ratio of the silicon trenches that were needed to be etched to define the device ($A_r = t/x_o$). It was decided to limit the aspect ratio to <10 to ensure manufacturability using standard DRIE technology. Since the resolution available at UTEP's Nanofabrication Facility is ~0.5 μm, this meant that $x_o \geq 0.5$ μm. It was decided to have devices with 3 gaps as follows; $x_o = 0.5, 0.75$ and 1.0 μm. This meant that the maximum thickness of the beam had to be $t = x_o A_r = 0.5 \times 10 = 5$ μm.

The next parameters to determine were the length (L) and width (W) of the beam. Equation 5 describes the restoring force of the beam as product of k_{CAN} (spring constant) and x (displacement of the beam).

$$F = k_{CAN} x = \left[\frac{2EW^3 t}{3L^3}\left[\frac{3}{8-6(L_C/L)+(L_C/L)^2}\right]\right] x, \tag{5}$$

where E is the Young's modulus of silicon. It can be observed that k_{CAN} is highly dependent on the physical dimensions of the beam. In Equation 5, L_C and W were set to 85 μm and 3 μm, respectively.

This meant that the only underdetermined parameter was L. In order to verify that the $F_{TMD} \geq 10 \cdot F_{CAN}$ constraint was being met, k_{CAN} is plotted as a function of t for two values of L (27.2 and 40.8 μm) in Figure 17. Notice that the force constraint indicated by the lower blue line is met when $t = 5\ \mu m$ and $L = 40.8\ \mu m$ but *not* when $t = 5\ \mu m$ and $L = 27.2\ \mu m$.

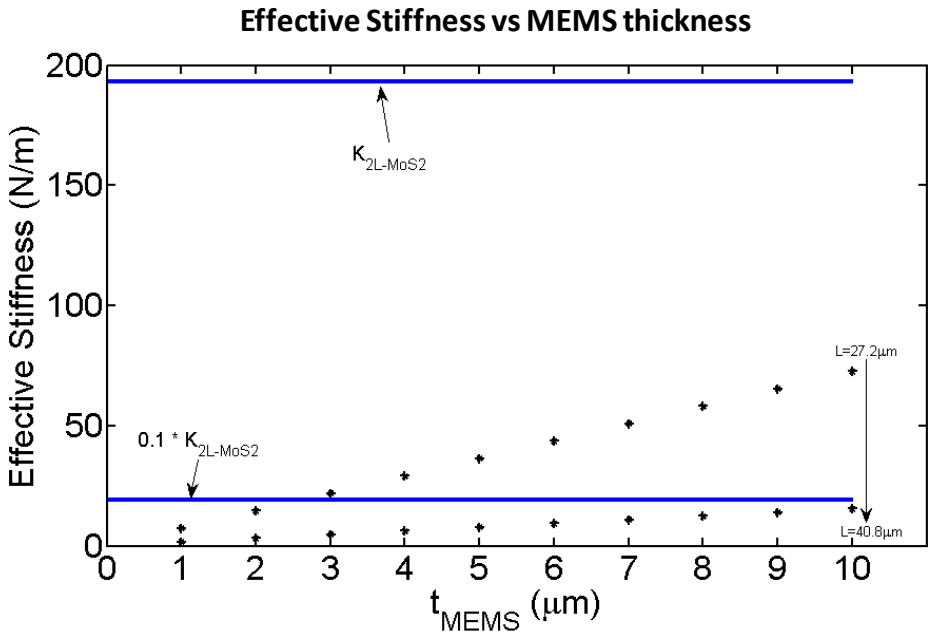

Figure 17. Preliminary analysis to show the change of stiffness with beam length and thickness to determine device parameters

Once the device parameters where determined by analyzing Equations 3 to 5, these were used to stablish the voltage range required to achieve 4% strain. Equation 4 was solved for voltage as shown in Equation 6. In this case, the Van der Waals forces are ignored for the larger version of the 3rd generation double-anchor SOI concept.

$$V_{GS} = \sqrt{\frac{2{x_o}^2(1-d)^2(k_{TMD}x_o\varepsilon + k_{MEMS}x_o\varepsilon)}{\epsilon_o A}} \tag{6}$$

In Equation 6, x_o is the initial gap and d is the displacement considering the 4% strain into the equation. The voltage vs displacement analytical relationship was used to compare and verify the strain-voltage curves obtained from simulation of the device using Coventorware as shown in Figure 18. In this comparison two different gap sizes, 0.5 μm and 0.75 μm, were used to show how the gap plays an important role, and to compare the simulation results with the mathematical model

(Equation 6). The voltage is reduced from 80 V to 50V to achieve ~3% strain for devices with 0.75 μm to 0.5 μm gaps, respectively. This voltage reduction highlighted the importance of scalability and effect of the gap for future generations. In addition, Figure 18 shows an inset of a 0.75 μm gap device demonstrating the displacement and strain percentage of the TMDC at 80 V. The inset shows that 3.33% strain could be achieved at the mentioned voltage, and the analytical model (Equation 6) correlates with a 3.11% strain.

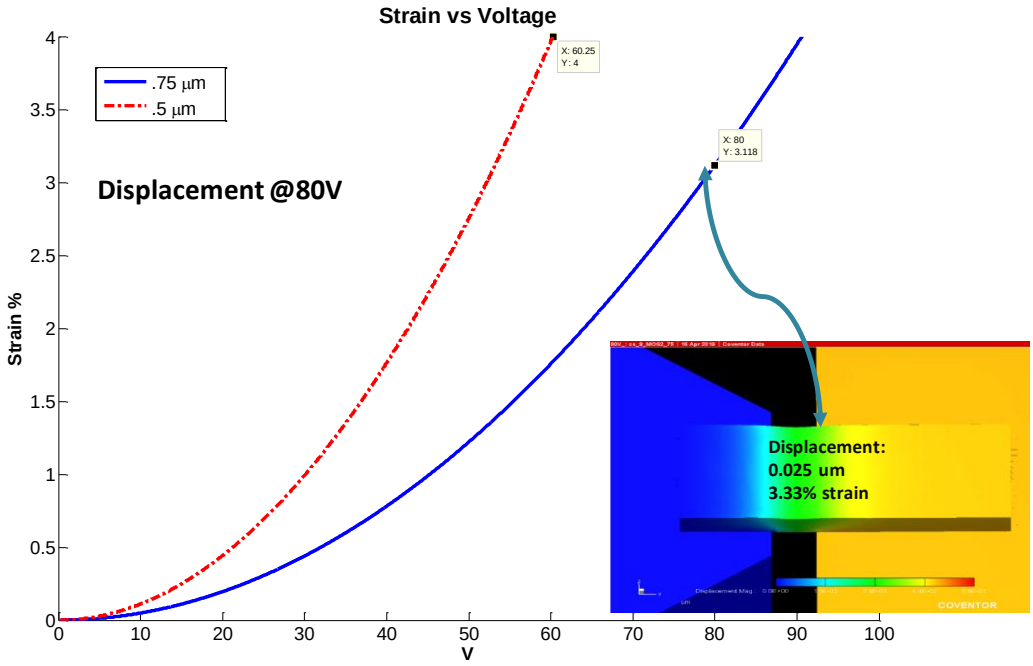

Figure 18. Voltage vs Strain relationship for a 0.5 um and 0.75 um gap and inset of a 0.75 um gap simulation correlating to analytical result.

2.3 Selection of Substrate

Once it was demonstrated that the mathematical model and simulation closely matched, further discussion and analysis was done to determine how the new device would be fabricated. The selection of the substrate was a very important part for the development of this work, since it will determine the necessary technology accordingly to the available equipment and the proper steps to fulfill the desirable device. As discussed in Chapter 1, SOI wafers were selected to fabricate the double-anchor MEMS. The selection of SOI facilitates the fabrication by utilizing

already known techniques for silicon processing and the readily available equipment located at the University of Texas at El Paso nanofabrication lab.

The selection of SOI as a substrate provides numerous advantages for the double-anchor fabrication. Amongst these, residual stresses can be said to be negligible during fabrication due to the device layer being silicon, as it is known that silicon can withstand several processes avoiding stress, therefore, accomplishing one of the goals to be met. Another important factor is the sandwich like structure of Silicon-Insulator-Silicon substrate, which creates an advantage to work on the device layer and creating a possibility for a single mask process. Furthermore, the resistivity of the device layer can be selected to a desired value, and if not, doping procedures can be performed to achieve ohmic contact for the metal electrodes. Another advantage for using SOI is the buried oxide layer (BOX). The BOX can be used as an insulator to prevent any leakage currents from the device layer to the substrate itself and as a sacrificial layer to release the MEMS structure.

A 3-inch p-type SOI wafer was selected considering that the nanofabrication lab has the capability to process 3-inch wafers. Three configurations of SOI wafers were purchased from Ultrasil Corporation. Table 2 shows the parameters of a desirable substrate for an optimum performance and fulfillment of the 3rd generation double-anchor design. The lowest resistivity available was from 0.01 to 0.05 Ω-cm being p-type boron doped. The resistivity is expected to correspond to a doping concentration of 9.719 x 10^{18} cm^{-3} to 9.392 x 10^{17} cm^{-3}, providing a good doping range for the metal-semiconductor interface. The BOX layer thickness is 1 μm to avoid any undesired out of plane actuation of the device and any leakage currents. For the 3rd generation double-anchor, the handle layer will not contribute much to the structure or performance of the device. Considering that, the handle layer thickness and resistivity were selected to be ~400 μm and 1-10 Ω-cm respectively. A schematic of the SOI wafer is shown in Figure 19.

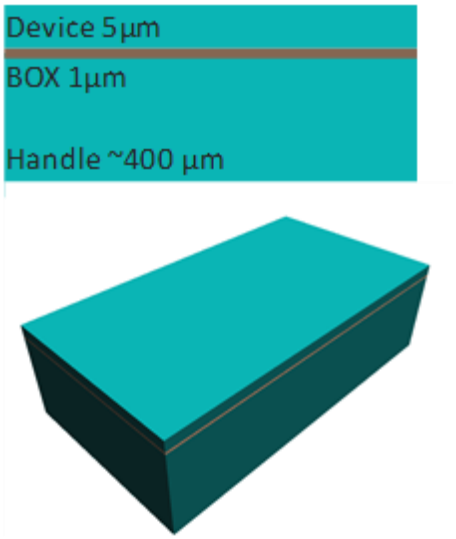

Figure 19. SOI Sample showing basic dimensions in cross-sectional view and 3D view

Table 2: SOI Substrate Parameters

Parameter	Value
Device Layer Thickness	5 μm
BOX	1 μm
Handle Layer Thickness	380 μm
Device Layer Resistivity	.01-.05 Ω-cm
Handle Layer Resistivity	1-10 Ω-cm
Wafer Size	3 Ω-cm

2.4 Fabrication Flow

The fabrication flow is another important part for the development of this work. It will determine the steps required to fabricate the double anchor. By creating a fabrication flow, it helps to understand each individual step and the importance that each step entails in the process. Moreover, it can create a model of the end product prior to any real fabrication, helping to conceptualize the design.

The issues shown in Table 1 were an important factor to determine the physical dimensions and substrate parameters for the double-anchor design. Moreover, these factors will also influence the fabrication process involved for the double-anchor design. By fabricating the devices at UTEP's Nanofabrication Facility, several of the issues in Table 1 are expected to be addressed. Higher throughput can be achieved by minimizing the required time for fabrication and testing. Taking advantage of the capability to process silicon at UTEP's Nanofabrication Facility, a fabrication flow was developed considering all the previously mentioned factors.

Figure 20 depicts how the process would flow starting from the SOI wafer to the release of the device structure. The process starts by having a clean SOI substrate, followed by a lithography step as seen in Figure 20 B). This lithography step is a negative tone lithography. Negative tone was chosen because it was observed that a metal layer could be deposited and patterned using lift-off to serve three purposes. The metal layer could be used as a hard mask for silicon etching, as a conductor to improve switching performance, and as a material to clamp the TMDC. Moreover, the need to use of a chemical to etch and pattern the metal hard mask was eliminated by using a lift off process. In this manner, the process flow depicted in Figures 20 B), C) and D) are crucially important to maintain the process simple. The following step after etching the silicon is the TMDC clamping process, where a second lithography is needed. Lastly, once the TMDC is clamped to the MEMS, the device should be released by using some SiO_2 etching procedure, which could be a vapor HF, or a critical dry process using buffered oxide etch (BOE).

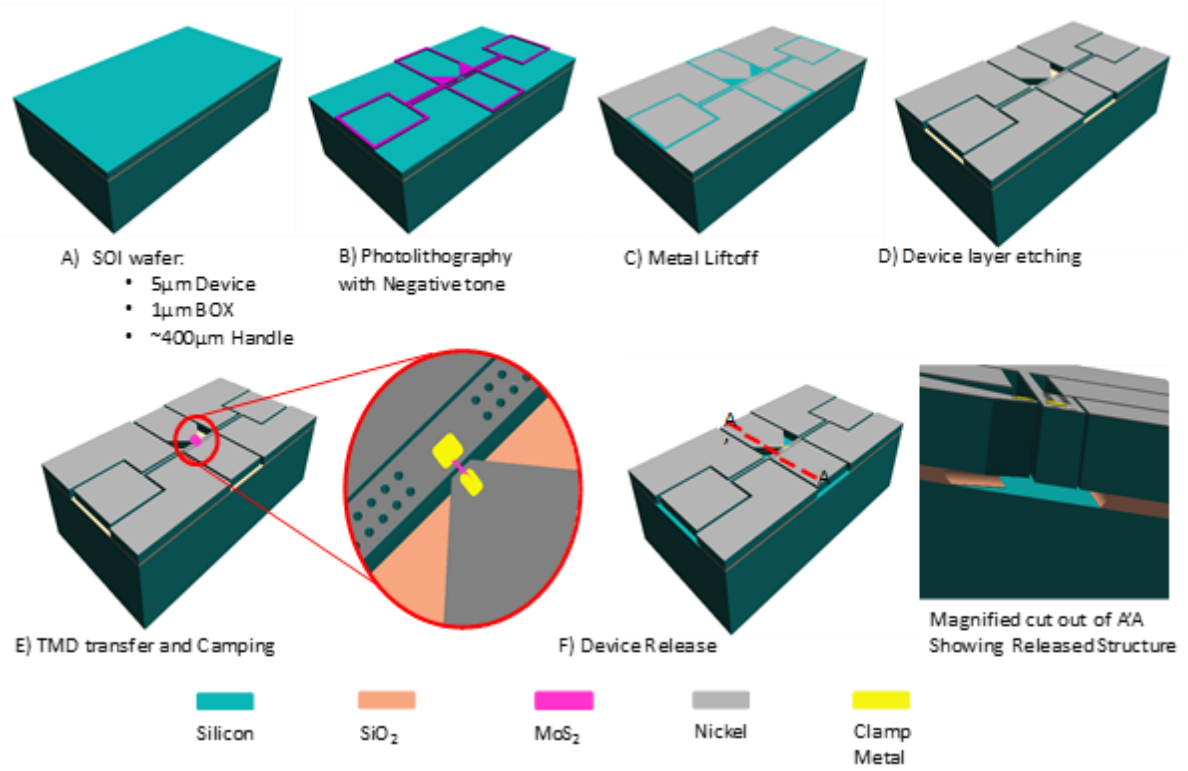

Figure 20. Fabrication Flow showing a) SOI substrate, b) the Lithography, c) Metal lift-off, d) dry etching,

2.5 Mask Design

During CMOS fabrication, it is known that several lithography steps are required, hence the need of several masks and designs. This can lead to misalignments which can lower the yield. Taking in consideration that a simple process is desired and that SOI wafers are used, a single mask was designed. However, to fabricate the double anchor MEMS with the integration of 2-D materials, two photolithography steps are required. To avoid a second physical mask, the device and anchoring designs can be integrated into the same mask creating a single die to serve as clamping mask during the second lithography step.

The mask was designed using the Layout Editor software that is included in the Coventor software package. It is important to note that the total beam length is given by,

$$L_{TOT} = 2L_{BEAM} + L_C \tag{8}$$

where L_{BEAM} is the length of the beam prior the key structure of the beam, and L_C is the length of the actuation area. L_C was set to a constant 85 μm. These dimensions are shown in Figure 21. The mask contained devices with three different beam lengths (L_{BEAM}) and three different gap sizes (x_o) to study the effect of each parameter on the device performance. These parameters are shown in Table 3. The combinations are 75 μm, 85 μm, 95 μm for the beam lengths, and 0.5 μm, 0.75 μm, and 1.0 μm for the gaps. This creates a total combination of nine variations (3x3 combinations). Different zones were created to separate each combination, where each individual zone consists of four rows and 7 columns. All nine zones conform a single 1cmx1cm die, where all possible combinations are included in each die providing a total of 252 devices per die.

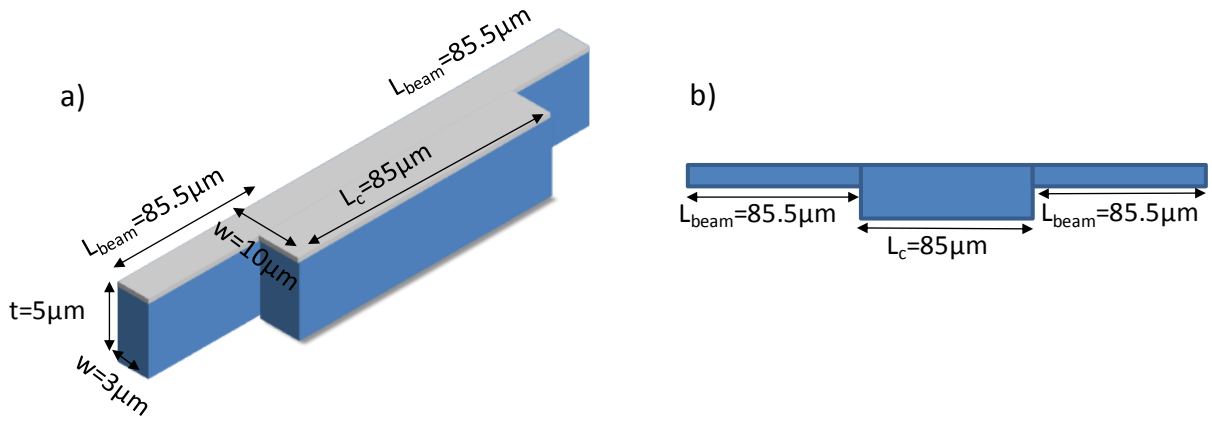

Figure 21. a) 3D model of beam and b) top view used for resistance calculations showing important dimensions of the beam.

Table 3: Different Zones showing length and gap combination

Zone	L_{BEAM} (µm)	x_o (µm)
1	95	0.75
2	95	0.50
3	95	1.00
4	85	0.75
5	85	0.50
6	85	1.00
7	75	0.75
8	75	0.50
9	75	1.00

Another important factor in the design for the mask is the lift-off process step involved in the fabrication. With this purpose, the mask needs to be a dark field mask. Therefore, the desired areas to be etched should be clear in order for the photoresist to cover the exposed areas, facilitating the liftoff process. Figure 22 shows the design of the mask. The complete 4-inch mask is shown in Figure 22 (a), a single die containing all the 9 different zone is shown in Figure 22 (b), and a zoom into how the device looks is shown in Figure 22 (c). From Figure 22 (c) it is observed that the device has a contour. The inside of this contour defines the clear field of the mask that will be covered by the photoresist, which will later be removed, leaving an exposed area to etch the silicon.

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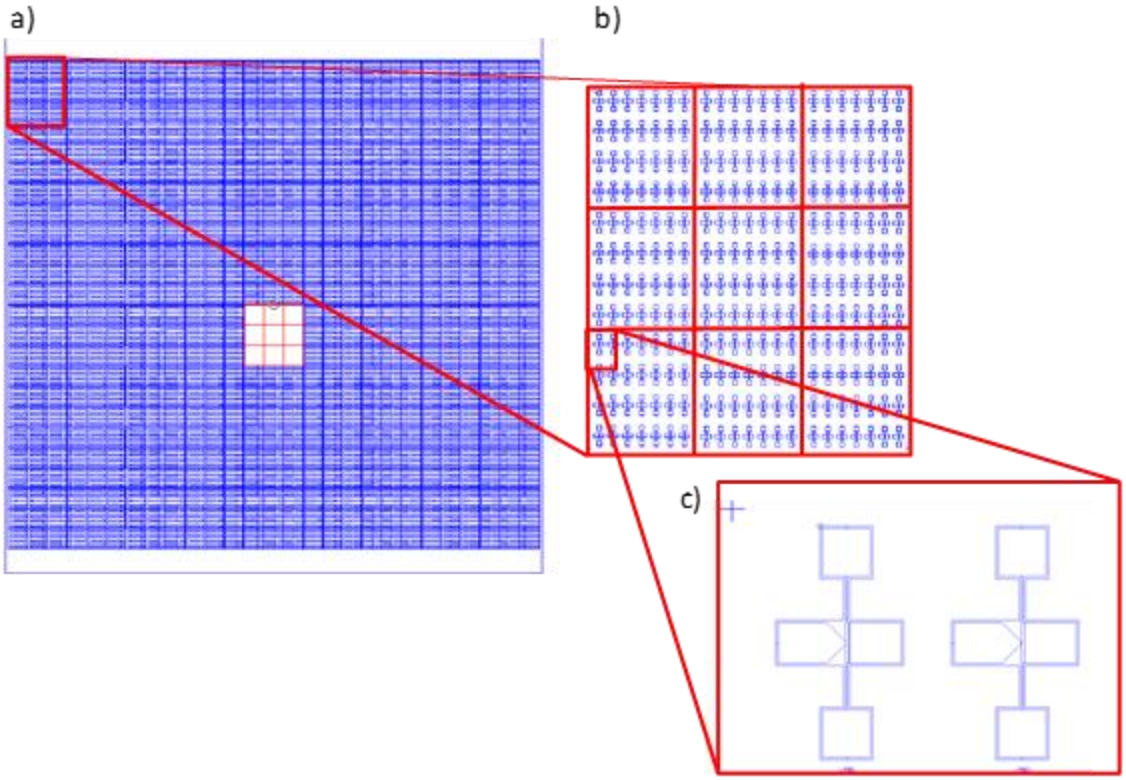

Figure 22. a) Complete 4" mask layout, b) a single die section with the 9 different zone, and c) a single device with an alignment mark for clamping purposes.

2.6 The Selection of Nickel

The selection of the metal layer is very important for multiple reasons. The metal has to form a good ohmic contact with the silicon device layer. Additionally, the metal needs to create a

very good mechanical anchor with the TMDC to prevent any slipping. Another important factor to consider is the ability for the metal to adhere to silicon without the need for a wetting layer. In addition, the metal has to be deposited in a non-conformal fashion to enable the lift-off process. Lastly, the metal should serve as a hard-mask and withstand the silicon etching process. Nickel was selected due to its low resistivity $\rho = 6.99x10^{-8}$ Ω·m, and its good contact with both p-type and n-type silicon [35, 16]. In addition, it has the ability to be thermally evaporated, and the advantage of silicide formation via annealing for the reduction of the metal-semiconductor barrier height [35, 16]. This makes nickel a good metal for interconnections of ICs [35]. Furthermore, nickel can withstand the dry etching process of silicon, making it even more attractive for fabrication. Additionally, nickel is a very commonly used metal to interface with MoS_2. It can be used in conjunction with a graphene layer to improve the electrical behavior of Ni-MoS_2 contacts [36]. MoS_2 is also known to be a lubricant material, hence the need of a metal that will hold the MoS_2 flake, which nickel fulfills. In this manner, nickel provides good electrical and mechanical characteristics that will contribute to the double-anchor performance.

2.6.1 Electrical Response Calculations

An estimate of the electrical response of the beam can be obtained by calculating the RC time constant. Of course, the beam is also governed by its mechanical resonant frequency. The lower of the electrical and mechanical frequencies will determine the ultimate switching speed. In this section, the RC time constant is calculated to estimate the electrical response. The double-anchor actuator is modeled as a capacitor with series resistance. The resistance is first calculated by analyzing the direction of current flow through the beam as it charges and discharges. The ability to distribute the electric field evenly across the entire beam is a key factor to achieve a strong electrostatic force. A low resistance will assist the electrostatic forces by distributing the electric charges through the device. The capacitance is then calculated by modeling the actuation area of the MEMS as two plates in parallel. Finally, the RC time constant is calculated.

Since the nickel metal layer serves as a hard mask covering the entire beam, the resistance calculation involves the resistance calculations of both the silicon and the nickel and their interaction. The drift resistance formula is given by,

$$R = \rho \frac{\mathrm{L}}{A} \tag{9}$$

where ρ stands for the resistivity, L for the length of the resistor, and A for the cross-section area. For a simple resistor L and A are straightforward to calculate. For the MEMS actuator, the calculation of L and A is more involved and the structure of the actuator must be taken into account in conjunction with the direction of current flow. To simplify the analysis, the beam is divided into two different perspectives, a lateral and vertical view to model the general direction of current flow through the device. This can be observed in Figure 23 (a) where two arrows indicate the lateral and vertical directions. To simplify the calculation further, the beam was considered as one whole rectangle, ignoring the three rectangular sections that form beam as shown in Figure 23.

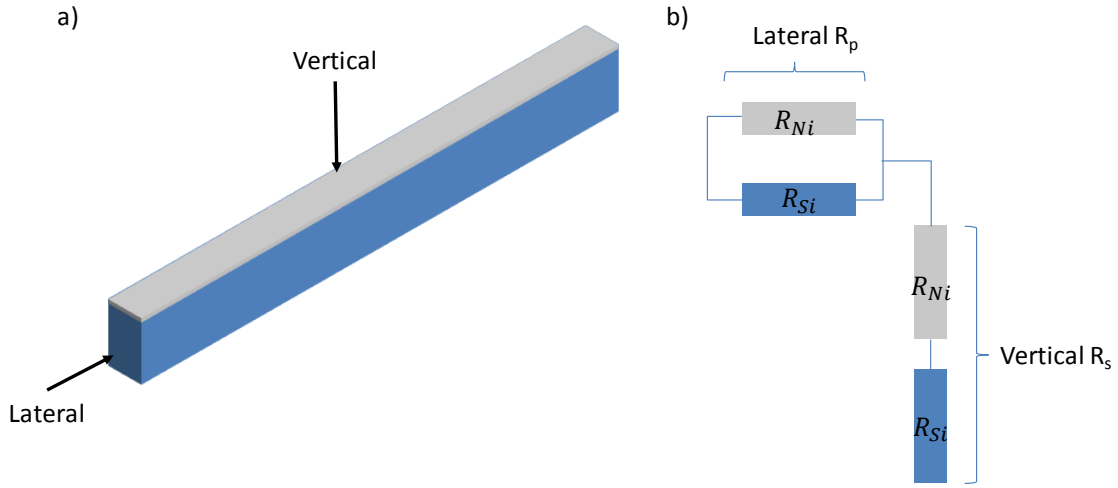

Figure 23. a) 3D model showing the direction of the cross-sectional area and b) the resistor configuration.

From the lateral perspective where the current will flow along the length of the beam, the resistance can be analyzed as the combination of the resistances of the nickel and silicon in parallel. From this configuration, it resembles two resistors connected in a parallel configuration as seen in Figure 23 b). These resistance calculations are performed using L_{TOTAL}= 255 μm. The resistivity

used for silicon was 0.01 Ω·m, which was obtained from the specifications of the SOI wafers. For the silicon layer, the cross-sectional area is the width multiplied by the thickness ($W \times t$), where $W = 3\ \mu m$ and $t = 5\ \mu m$. Looking at the nickel, the width is the same, but the thickness changes to that of the nickel which is $t_{Ni} = 0.1\ \mu m$. By using these parameters in Equation 9, the resistance calculated for silicon is,

$$R_{Si} = 0.1\Omega\text{m}\frac{255\text{x}10^{-6}\text{m}}{15\text{x}10^{-12}\text{m}^2} = 170\ \text{k}\Omega \tag{10}$$

in addition, the resistance of nickel is,

$$R_{Ni} = 6.99 \times 10^{-8}\Omega\text{m}\frac{255\text{x}10^{-6}\text{m}}{0.3\text{x}10^{-12}\text{m}^2} = 59.4\ \Omega \tag{11}$$

Since the configuration is in parallel, the total resistance from this cross-sectional view equals to

$$R_p = \frac{R_{Si}R_{Ni}}{R_{Si}+R_{Ni}} = 59.39\ \Omega \tag{12}$$

This suggests that the majority of the current will flow through the nickel as expected since the conductivity of nickel is much higher than silicon.

It is also necessary to take into the account the flow of current in the vertical direction when analyzing the charging and discharging of the silicon actuation area. In addition to the drift resistance of the individual nickel and silicon layers, the contact resistance between the two must also be taken into account. However, the contact resistance is assumed to be negligible since for a silicon resistivity of 0.01 Ω·m the barrier height with nickel is very small.

From the vertical perspective, the cross-section area needed for the drift resistance calculation becomes the surface area seen from the vertical view. This area is obtained by multiplying the total length of the beam by the width of the beam ($L_{TOTAL} \times W$). In a similar manner to the lateral view, both silicon and nickel resistances have to be calculated but in this case, the resistances are combined in series. For the resistance of silicon, the length in Equation 9 is the thickness of the silicon layer. This gives a resistance of,

$$R_{Si} = 0.1\Omega\text{m}\frac{5\text{x}10^{-6}\text{m}}{765\text{x}10^{-12}\text{m}^2} = 65.35\ \Omega. \tag{13}$$

Similarly, the nickel resistance is calculated as follows,

$$R_{Ni} = 6.99 \times 10^{-8}\Omega\text{m}\frac{0.1\text{x}10^{-6}\text{m}}{765\text{x}10^{-12}\text{m}^2} = 9.13\ \mu\Omega \tag{14}$$

In the vertical direction, the resistance of the silicon and nickel combine in a series configuration as shown in Figure 23 b) and is given by,

$$R_S = R_{Ni} + R_{Si} = 65.35000913\ \Omega \tag{15}$$

The total resistance including both directions is given by the summation of R_s and R_p as given by,

$$R_T = R_p + R_S = 124.7\ \Omega \tag{16}$$

Once the total resistance was obtained, then the capacitance for the parallel faces can be calculated using,

$$C_o = \frac{\epsilon_o A}{x_o} \tag{17}$$

where ϵ_o is the permittivity of free space, A is the actuation area ($L_C \times t$), and x_o is the gap between the plates when it is strain free. Using L_C = 85 μm, t = 5 μm and x_o = 0.75 μm, the strain-free capacitance is $C_o = 5.0174\ f$F. Lastly, the RC constant then equals to,

$$\tau = (124.7\ \Omega)(5.0174 \times 10^{-15}\text{F}) = 6.2567 \times 10^{-13} s \tag{18}$$

which in frequency equals to f = 1.5983 THz.

Chapter 3: Development of Lithography Process

The photolithography process has become one of the most important and crucial steps in any device fabrication nowadays. Lithography allows printing on the wafer and defining the desired geometry or geometries that will be used. This sets the first building block for the fabrication process. This chapter will discuss the development process of an image reversal lithography. It will detail the procedures and the importance of certain factors for the reversal process.

3.1 Development of Image Reversal Process

As stated in section 2.5, lithography is a very important process. Lithography can be seen as a blueprint to fabricate a vast majority of semiconductor devices. There exists two different kinds of lithography, positive and negative. To fabricate the double-anchored MEMS, a lift-off process was chosen to maintain the process simple. For this purpose, a negative photoresist is usually more suitable than a positive tone, since negative tones can achieve high aspect ratios and provide a slope profile in the photoresist facilitating the lift off process. Due to the simplicity of depositing the metal layer and simply using some solvent to remove the photoresist with metal on top, this method was preferred. In addition, developing a proper recipe is very important, since each step involved will affect the transferring of the mask into the wafer.

The photoresist that is utilized is the AZ5214-E, which is an image reversal photoresist that normally behaves as a positive tone but can act as a negative tone by altering some of the lithography steps. The general approach that was taken to develop a negative tone process was to first start with an already developed positive-tone recipe and alter several steps as recommended by the photoresist manufacturer to achieve negative tone. This gave a non-optimized negative-tone image. Then several parameters are adjusted to obtain good image quality.

The basic steps needed to achieve a non-optimized negative-tone image with the AZ5215-E are shown in Table 4. After a piranha clean and oxide removal on bare silicon wafers,

hexamethyldisilazane (HMDS) is spun coated at 7000 rpms. The wafer is then baked at 110ºC for 2 minutes. Normally, the HMDS application is to promote the adhesion of the photoresist to the substrate if there is any SiO_2 layer on the surface. After letting the wafer cool down for few seconds, the photoresist was applied by spin coating at 4000 rpms. According to the spin curve data from the photoresist datasheet, 4000 rpms would provide a thickness of ~1.4 μm. The following step is a soft bake at 110ºC for 2 min in a hot plate. The wafer is exposed using a Karl Suss MJB3 mask aligner for 35 seconds at 2.25 mW/cm^2 giving an exposure dose of ~78.75 mJ/cm^2. If Table 4 is followed until step 6, it corresponds to a positive tone lithography, in order to accomplish an image reversal; a post exposure bake is needed. According to the AZ5214-E datasheet, the post exposure bake is the most important step. By following the provided guidelines, the post exposure bake was done at 120ºC for 2 minutes. Next, a flood exposure without a mask is carried out, where the exposure dose can be anywhere from 150 mJ/cm^2 to 500 mJ/cm^2. For the flood exposure, the dose was selected to be ~213 mJ/cm^2. Lastly, the wafer is developed using the AZ 300 MIF developer.

Table 4: Non-Optimized Negative-Tone Lithography Steps

Step	Procedure	Parameter	Time
1	Piranha Clean	H_2SO_4 (mL): H_2O_2 (mL) (2:1)	10 minutes
2	HMDS Application	7000 RPMS	35 seconds
3	HMDS Bake	110ºC	2 minutes
4	PR Spin Coat	4000 RPMS	45 seconds
5	PR Soft Bake	110ºC	2 minutes
6	UV Light Exposure	2.25 mW/cm^2	35 seconds
7	Post Exposure Bake	120ºC	2 minutes
8	Flood Exposure	2.25 mW/cm^2	95 seconds
9	Develop	500 mL	1 minute

The lithography steps in Table 4 were experimentally tested on a bare silicon wafer and the result is shown in Figure 24 (a). The lighter areas in Figure 24 are the silicon and the darker areas are the patterned photoresist. Further study of Figure 24 (a) show that in general negative

tone was achieved but the structures had low resolution. For example, the thin part of the beam was very thin and missing in some areas. Moreover, etch holes in the central part of the beam (which were incorporated in the mask to facilitate release of the MEMS) looked distorted and not well imaged. Two parameters that are very important for the image reversal process to be successful are the first exposure and the post exposure bake. If these parameters are not optimized, the photoresist creates a "widening" effect due to the ability to create a sloped profile. This explains why the narrow part of the beam was very thin and missing in some areas (see Figure 24 (a)).

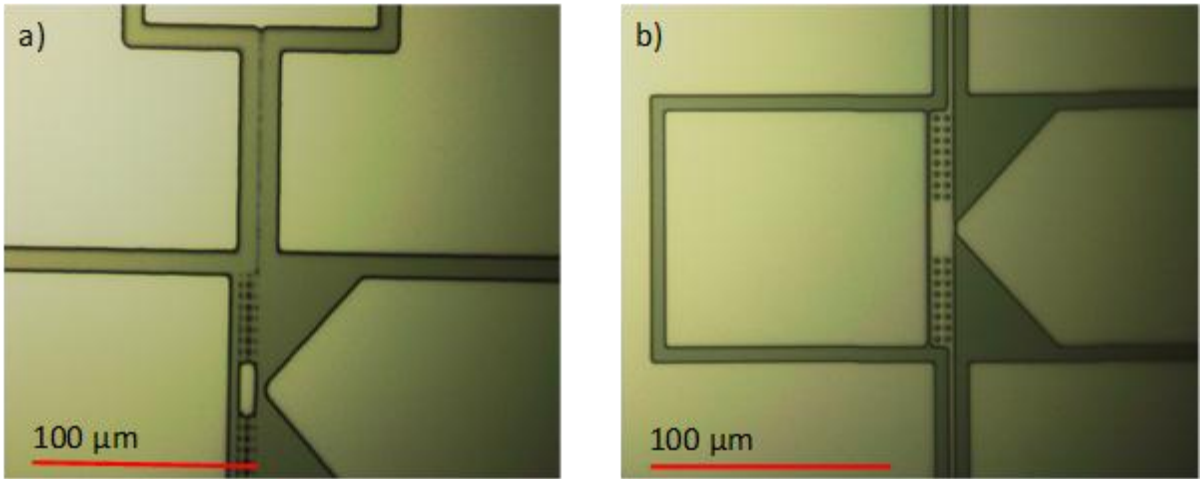

Figure 24. Plan view optical images of a patterned photoresist on a bare silicon wafer using the (a) non-optimized and (b) optimized negative-tone lithography processes.

To start optimizing the recipe, understanding how the equipment worked to deliver the adequate dosage required during the first exposure step was crucial. The Karl Suss MJB3 mask aligner is a contact lithography equipment. However, it has three operation modes; two hard contacts and a soft contact mode [37]. The first lithographies where done using the Standard Mode (ST), which only creates a mechanical pressure between the mask and the wafer However, in contact lithography, the spacing between the mask and the wafer is very important and one of the limiting factors for the resolution. This can be solved using the Vacuum Contact Mode (HP), where the system pulls vacuum between the mask and the wafer reducing this air gap between them [37]. Once this change was made, the printed image started to improve by showing more features of the desired device (see Figure 25), where the beam progressively becomes visible.

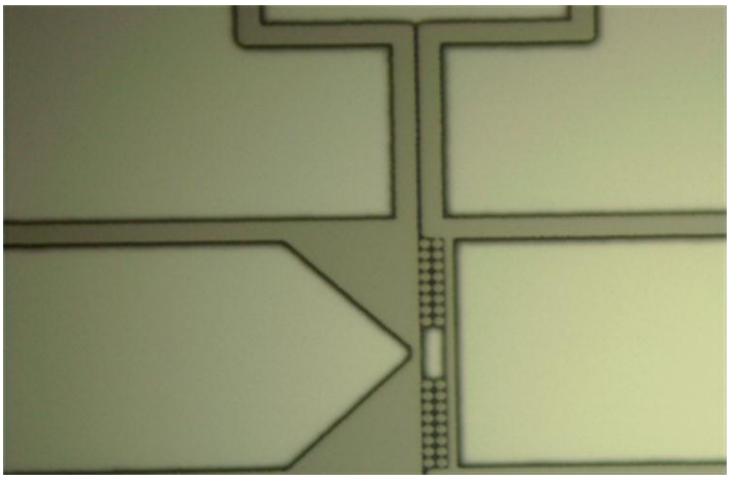

Figure 25. Lithography results after changing the contact mode of the Karl Suss equipment

After changing the operation mode of the equipment, to improve the image, a reduction of the first exposure dose was made. The product data sheet states that the dose should be lower, or at least half, of what the positive tone procedure requires [38]. Following the product data sheet, a reduction from 35 seconds to 15 seconds was made, corresponding to ~33 mJ/cm^2, still providing some opportunity to improve. Work in [39] provides an insight of different profile results for the photoresist by doing different dose and temperature combinations, for example, they set the dose at 8 mJ/cm^2 and they vary the Post Exposure Bake (PEB) to show the effect of temperature at an specific dose, and vice versa. It was observed that at 10mJ/cm^2 a sloped profile for the photoresist can be achieved, which are suitable for lift-off purposes. From 15 seconds the recipe was changed to 5 seconds to give an approximate of 11 mJ/cm^2 improving the results, however, some of the device structures still were not showing as expected. However, the beam started to become visible, even though the structure still looked somewhat dark as shown in Figure 26.

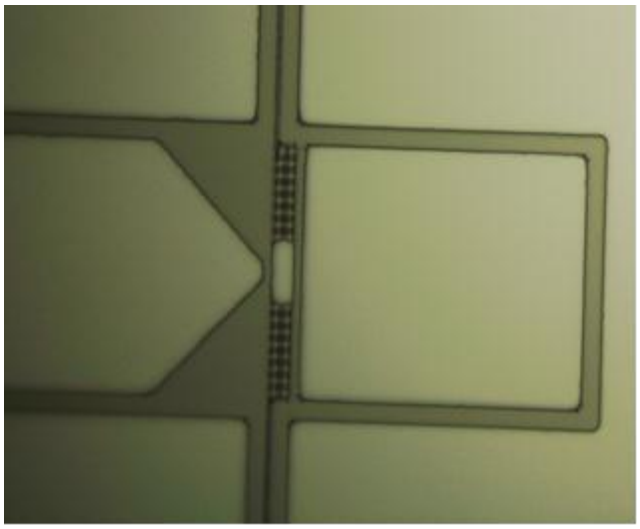

Figure 26. Results of lowering the exposure dose starting to show a beam structure.

Once an adequate exposure dose was achieved, the post exposure bake temperature and time had to be changed accordingly. The data sheet for the AZ 5214 E suggests that this temperatures should range from 115ºC-125ºC. As stated before, 120ºC for 2 min was used at first. A reduction of time was done from 2 minutes to 1:30 minutes. However, the image still appeared as the results from Figure 26. To improve the results, the temperature was reduced to 110ºC for the same time of 1:30 minutes. As seen in [39], 110ºC makes a great combination with 10 mJ/cm^2 to achieve a profile suitable for lift-off. With all these changes made, a desired lithography was fulfilled as seen in Figure 24 b) where a complete structure is clearly visible. Table 5 shows the optimized recipe that provided promising results.

Table 5: Optimized Lithography Recipe

	Values	**Time**
Spincoating	6000 RPM	~40 seconds
Prebake	110ºC	1:30 min
1st Exposure	2.25 mW/cm^2	5 seconds
PEB	110ºC	1:30 min
Flood Exposure	2.25 mW/cm^2	95 seconds
Developing	300-500 ml	30-40 seconds

A comparison between the first lithography attempts and the final lithography results is also shown in Figure 24. The changes are very significant; the entire beam structure seems completely erased in Figure 24 a). Once the exposure equipment was set to HP mode, the image

improved, however, it was not until the proper exposure dose and PEB that the entire structure fully resolved as seen in Figure 24 b). The combination of the exposure and PEB are crucial. This image reversal process creates an angle on the sidewalls of the photoresist for lift-off purposes. If the dosage and temperature are not correct, the photoresists creates a "widening" effect due to the angle formed during the cross-linking process the photoresist goes through to behave as negative tone.

SEM images were also taken to show that the desired photoresist profile for the lift-off was achieved, and the desired feature sizes were as close to the mask design. As observed in Figure 27, the thickness of the photoresist is approximately 1.6 μm with some slope desirable for the lift off process, since the thickness of the desired nickel is 100 nm. It is very common for lift-off purposes to have at least 10 times thicker photoresist than that of the metal thickness. A thickness of 1.6 μm still gives enough room to do some O_2 plasma cleaning to remove any residual photoresist prior the metal deposition, and subsequently do a native oxide etch, and still be at the 1 μm thickness range to accomplish lift-off.

The profile of the photoresist is important for several reasons. If the angle comes closer to 90^o then some fabrication problems can occur such as "bunny ears" during deposition, no success in lifting off. If the angle is excessively small one can encounter the issue of "widening" since the shadowing effect becomes larger. Figure 27 shows an adequate profile for the photoresist, where it can create a small shadow for the metal to deposit and permit the solvent to remove the photoresist with metal on top.

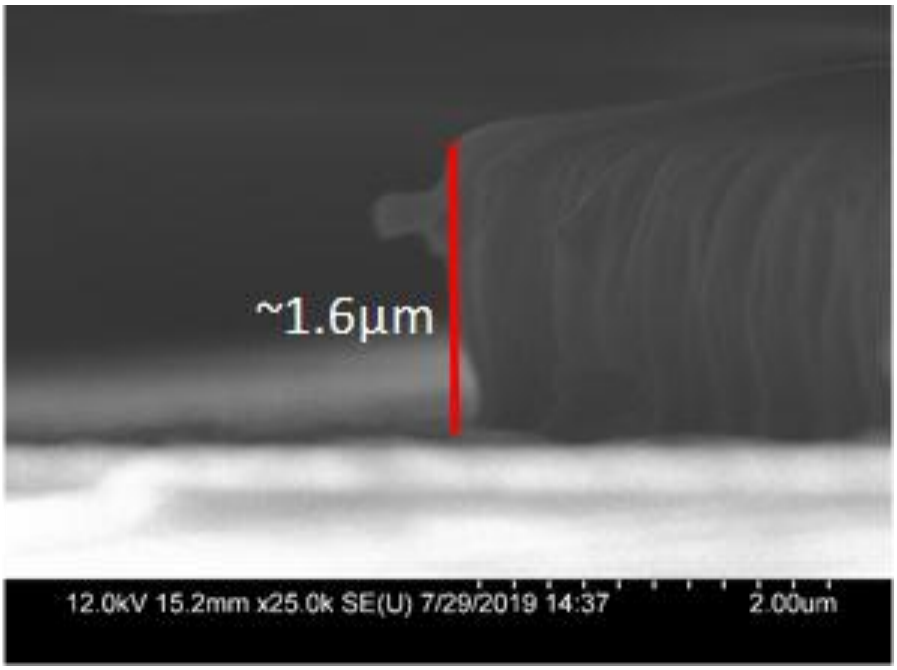

Figure 27. SEM showing thickness and desired profile for lift-off process

Chapter 4: Deposition of Nickel

This chapter will discuss the development of a process to deposit nickel via thermal evaporation, how to maintain a controllable and easy setup for future iterations, and lastly the process utilized pattern the nickel via lift-off.

4.1 Deposition of nickel via thermal evaporation

Different deposition techniques exist, amongst these, thermal evaporation is one of the most commonly used due to its capability of melting a material and allowing it to deposit onto a substrate. Thermal evaporation is readily available at the nano fabrication facility located at the University of Texas at El Paso, facilitating the access to a deposition method.

The Kurt J. Lester deposition system called "Shania" at UTEP's NanoMIL facility was used for the nickel thermal evaporation depositions in this work. Table 6 briefly describes the steps involved to successfully deposit nickel via thermal evaporation. To begin the process, the depositor is loaded with a three-quarter inch dimpled boat that is made of tungsten coated with a thin layer of Al_2O_3. The boat has a 12.7 mm diameter and 3.175 mm deep dimple being equivalent to 0.403225 cm^3 of volume. The dimple is filled with three 1/8" x 1/8" nickel pellets. Nickel has a density of 8.908 g/cc, giving an estimate of 3.6 grams for the three initial pellets of nickel used during the first deposition run.

Table 6: Required Deposition Parameters to deposit Nickel.

	Procedure	Parameter	Time
1	Rough Vacuum	50 mTorr	1 hour
2	High Vacuum	1 μTorr	2 hours
3	Melting	50%	15 seconds
4	Deposition	30-40%	3 minutes
5	Cool Down	760 Torr	1 hour

To achieve a uniform and clean deposition, the equipment used for deposition needs to reach a certain vacuum level prior to any deposition run. The equipment goes through a rough vacuum process to get rid of any turbulent flow and large particles. The rough vacuum runs for

~1hr to reach a pressure of 50 mTorr. Once the rough vacuum is done, the chamber goes through a high vacuum process using a cryogenic pump. The high vacuum process takes ~2 hours to reach a vacuum level of ~1x10^{-6} to 3 x10^{-6} Torr. This will ensure that during the deposition the chamber pressure is below the vapor pressure of nickel.

After reaching high vacuum, a power supply is used to heat the tungsten boat via I^2R heating. The power is slowly ramped up to 50% of capacity and after approximately 50 seconds, the boats starts to glow brightly and the nickel is observed to melt and assume a spherical shape. This must correlate to the melting point of nickel at 1453ºC. In addition, the system's ion gauge increases approximately 3x10^{-5} Torr indicating an increase in nickel vapor pressure. The soak time is ~15 seconds, and then the power is slowly reduced to 30% power in order to have a more stable and slow deposition rate. It was observed that by lowering the power to ~30% a 5-6 Å/s (Angstroms/second) deposition rate was achievable. This procedure is very constant and reproducible when it is the first run utilizing a new loaded boat. After this, to maintain the mentioned deposition rate, the power must be maintained somewhat higher around 35%-40%. The deposition run lasts ~3 minutes, which corresponds to ~100 nm at 5-6 Å/s. This process was optimized to obtain a nickel thickness of ~100 nm.

4.2 Lift-Off Process Development

A lift-off process was developed pattern the nickel which removes the undesired areas of the deposited nickel and exposes silicon areas. This is important since the nickel will serve as a contact metal and hard mask to etch the underlying silicon layer as stated in previous sections of this work.

Although the lift off process is a simple process in concept, attention to details is needed to achieve good results. Figure 28 shows a comparison of before and after an acetone bath was used to desolve photoresist and lift-off the nickel. It was observed that an overnight acetone bath did not remove the photoresist with nickel. During the deposition, the photoresist hardens as it is

exposed to heat since the wafer sits at an estimated distance of 30 cm from the boat. Normally, substrates are placed at a larger distance preventing the hardening effect and facilitating the lift off in acetone. As a result, a sonication bath was done in the hope to assist the process; however, the sonication provoked ripping off the nickel. This problem required that the acetone be replaced by a more aggressive solvent such as AZ400T stripper for a more effective lift-off.

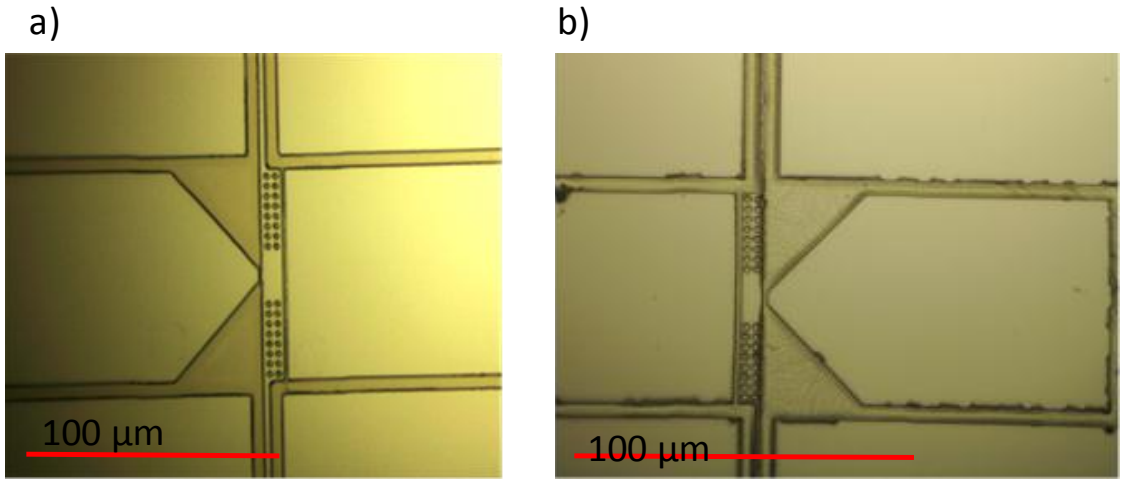

Figure 28. a) Plan view optical images showing device after nickel deposition prior acetone bath and b) after overnight acetone bath.

The process was optimized after changing the acetone for the AZ400T. This improved the lift-off result significantly as shown in Figure 29. After an overnight bath in AZ400T, the wafer was rinsed with a 10 minute DI bath and a second DI bath of 5 minutes. An acetone, IPA, DI rinse cleaning was followed to clean any residue left. Although the results were very promising, a further optimization was done to improve the timing and the overall cleanness of the wafer.

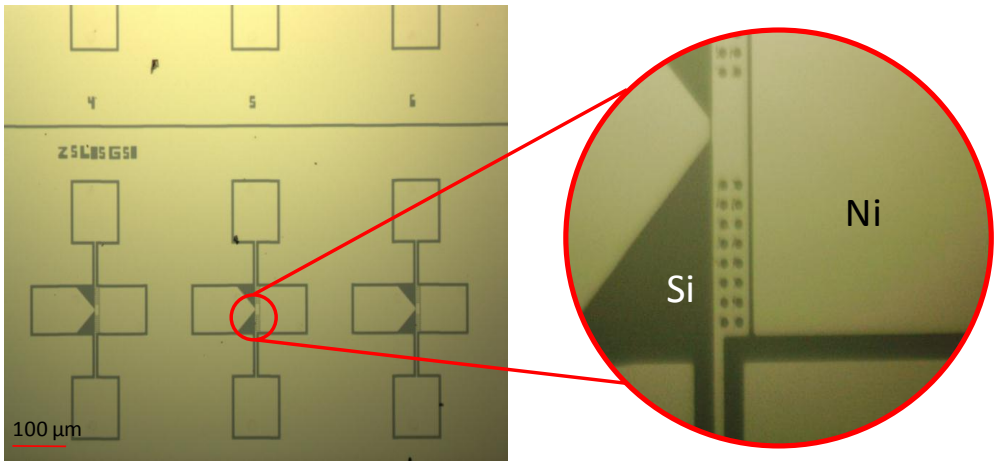

Figure 29. Lift-off results utilizing AZ400T stripper bath.

To further improve and optimize the process, the AZ400T can be heated to accelerate the removal of photoresist significantly. This was observed by reducing an overnight bath to around 35-40 minutes bath. The stripper was heated to 200°C, which is below its flashing point. Another crucial step is how the wafer is removed from the stripper band. This is very important so that no re-deposition of lifted-off nickel flakes occurs. This is done by slowly retrieving the wafer and doing a DI water rinse. This improved significantly the results, shorter times and cleaner surfaces were achieved. Nonetheless, there existed some re-deposition of the lifted material, which can be improved by suspending the wafer facing down. Since the lift off was successfully done, a sonication was done without the fear of a ripping effect. The sonication ran for 7 minutes in an acetone bath, followed by another sonication with IPA of the equal amount of time. Lastly, the wafer was rinsed and dried, ready for characterization.

4.3 Deposition and Liftoff Results

After optimizing the deposition and lift-off procedures, the wafer is then scanned using a DektakXT profilometer to measure and estimate the thickness of the nickel as observed in Figure 30. This serves as a quick preliminary result to match and calibrate the crystal monitor readings from the Inficon system.

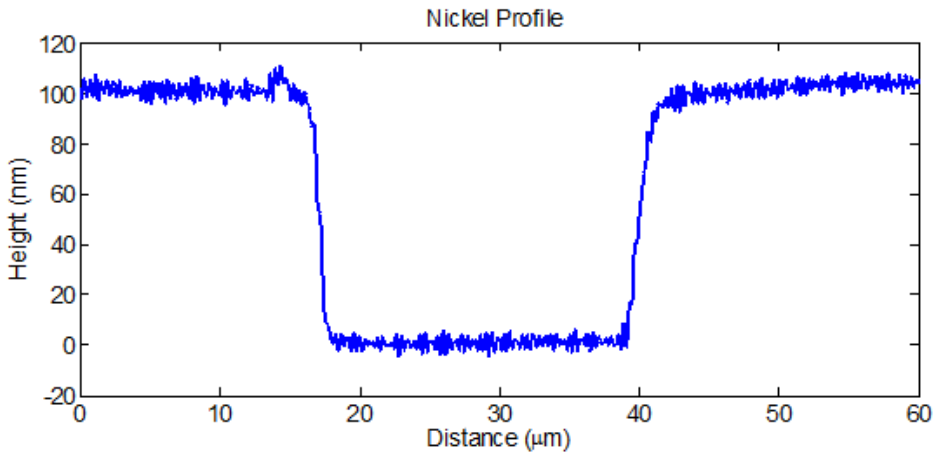

Figure 30. Nickel height profile data.

Subsequently, the wafer is measured from a cross-sectional view, to determine if the thickness correlates to the profilometer data. The cross section is viewed under an SEM as it is observed in Figure 31, demonstrating that there is a 100 nm thick layer of nickel as expected.

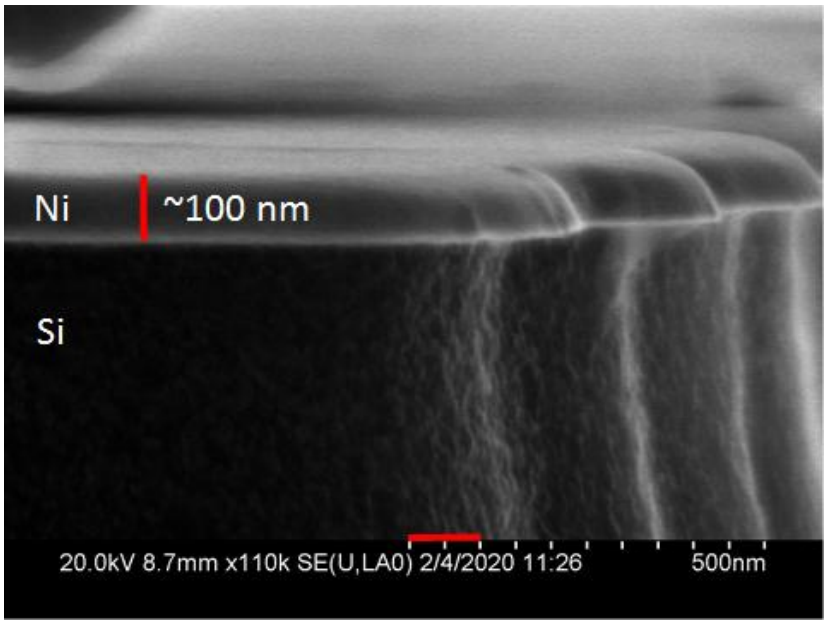

Figure 31. Cross-section showing ~100 nm of nickel

Chapter 5: Development of Silicon Etching

This chapter will talk about the Reactive Ion Etching method to etch silicon with Sulfur hexafluoride (SF6), Argon (Ar), and Oxygen (O2) and the development of an etching recipe utilizing an Oxford PlasmaLab 80 Plus.

5.1 Silicon Etching

Extensive work [40] has been done to develop different recipes and techniques to etch silicon. Amongst these techniques, the Bosch process has been widely accepted and is generically called deep-reactive-ion-etching (DRIE). This process consists in alternating C_4F_8 with SF_6. The C_4F_8 cycle creates a protective layer, and the SF_6 etches only the bottom of this protective layer and not the sidewalls. The process requires a high-density plasma and a system fast enough to change the gases quickly, since SF_6 gives an isotropic etch.

Some preliminary results were done utilizing a DRIE system located at Universidad Autonoma de Ciudad Juarez (UACJ). Several runs where attempted, where they all ran several cycles of 5 seconds C_4F_8 and 5 seconds SF_6 at different flow rates. The result was a very isotropic etch depicted in Figure 32. It is estimated that the number of cycles could have been too many for the feature sizes and the flow rates for the gases were not optimized. Even though an anisotropic etch was not achieved, these preliminary results show the high selectivity of silicon over the nickel hard mask and formed a basis to develop a reactive ion etching process at UTEP.

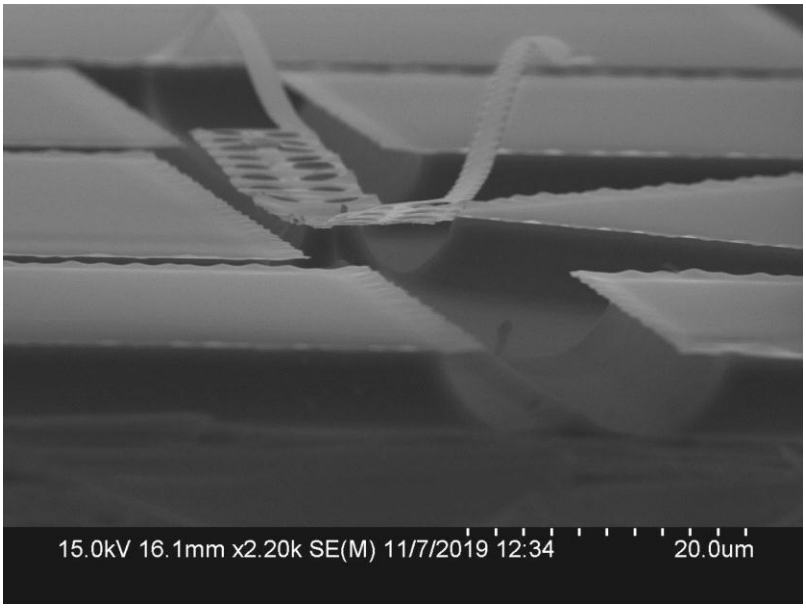

Figure 32. DRIE preliminary results showing high isotropic etch.

5.2 Development of an Anisotropic RIE Process

Work done in [41] details the physical and chemical procedures during the etching of silicon utilizing SF_6, which is one of the most common gases used to etch silicon. SF_6 has a high etching rate which depends on the pressure inside the chamber [41, 42, 43]. However, SF_6 creates an isotropic etch rather than an anisotropic etch. Fortunately it was observed in [43] that by mixing SF_6 with some other gases, like O_2 and Ar, anisotropic etching can be achieved. The use of oxygen in the mixture helps protect the sidewalls of silicon. Meanwhile, argon helps to stabilize the plasma density and to assist with ion bombardment of the silicon surface for an enhanced anisotropic etch. In order achieve a good degree of anisotropy and high etch rates, several parameters such as pressure, RF power, and gas flow rates needed to be developed.

An Oxford PlasmaLab Plus 80 etcher was used for the development of the recipe. The PlasmaLab is a reactive-ion-etch (RIE) system that has the ability to deliver the following gases: SF_6, O_2, Ar, CF_4, and CHF_3. Although RIE does not produce plasma in the same density as a DRIE, it can achieve decent anisotropic profiles with the proper settings. Several experiments were done using 3" p-type silicon wafers, ~380 μm thick, with a 100 nm nickel thick layer as a hard mask.

The etch depth goal was 5 µm since that is the thickness of the SOI device layer. Several recipes were tested to determine the best combination of gases to obtain desirable results. Prior to the silicon etching process, native oxide has to be removed, this is done using a brief run of CHF_3 and Ar plasma.

Different recipes that use a fluorine-based gas in combination with oxygen to enhance the anisotropic etch were obtained from literature and used a test recipes [44, 42, 41] as listed in Table 7. These recipes run in a single cycle, instead of cycling between gases like the Bosch process. After comparing each result, test recipe #3 showed very promising results and is show in Figure 33. However the recipe still needed to be optimized further. One problem was that the etch rate was very slow, ~0.05µm/min. At this rate, 100 minutes would be needed to etch 5µm.

Table 7: Etching test recipes.

Test Recipe	CF_4 (sccm)	SF_6 (sccm)	Ar (sccm)	O_2 (sccm)	Power (W)	Pressure (mTorr)
1	40	10	0	10	30	15
2	0	10	30	50	100	20
3	0	10	50	30	100	10
4	0	25	0	25	200	10

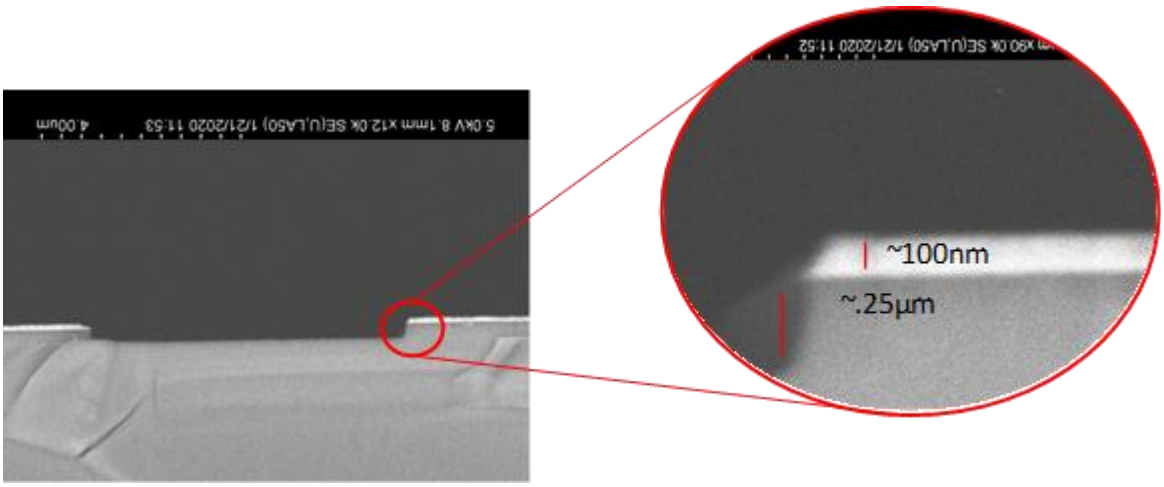

Figure 33. Results of test recipe #3 showing anisotropic profile.

To optimize recipe #3 and meet the 5 µm goal, several runs were made by changing the pressure and power to obtain a relationship between them. These combinations are observed in

Table 8. The RF and pressure were set to 3 levels; 100 W, 150 W, and 200 W for the power and 0.10 Torr, 0.02 Torr, and 0.05 Torr for pressure. All runs were 5-minute long to obtain some preliminary results. The results obtained are also shown in Table 8 where a comparison between runs can be observed. The first four runs were designed to study the effect of RF power and gas pressure on the etch profile. The results showed that there was little to no effect in increasing the RF power of the system at low pressures. However at higher pressure, the etching rate increased significantly with increasing the power and pressure. The plot in Figure 34 shows this RF/Pressure relationship from recipes 1-4.

Although higher pressure resulted in faster etch rates as shown in Figure 34, the etch result was an isotropic profile. It is important to mention that even in lower pressures some undercut bias exists; however, it was considered negligible to assume 0 undercut bias. Yet, the etch rate at low pressure was too slow. Runs 1-4 helped understand the etching relationship between pressure and power to develop further runs. The results from runs 1-4 helped to discard the use of high pressure and replace with a midrange value.

It was observed that an almost linear relationship exists between changing the working pressure from one recipe to another. For example, runs #1,3, and 8, all are set to the same RF power, however the pressure changes by a half differing from 0.1 Torr to 0.05 Torr. The etch rate also decreased almost by the same factor of half. After analyzing the data, and understanding how the etch rate was affected by the RF and pressure, the etch rate became more predictable, and the recipe was narrowed down to utilizing 0.05 Torr and 150W since it showed very promising results.

Table 8: Silicon Etch Optimization Recipes

	SF_6 (sccm)	Ar (sccm)	O_2 (sccm)	Pressure (Torr)	Power (W)	Etch Depth (μm)	Etch Rate (μm/min)	Bias (μm)	A_f
1	10	50	30	0.10	100	1.480	0.296	0.21	0.86
2	10	50	30	0.02	200	0.375	0.075	0.0	1.00
3	10	50	30	0.02	100	0.250	0.058	0.0	1.00
4	10	50	30	0.10	200	3.100	0.62	0.75	0.75
5	10	50	30	0.05	150	0.850	0.17	0.10	0.88

6	10	50	30	0.02	150	0.20	0.04	0.0	1.00
7	10	50	30	0.02	200	0.250	0.05	0.0	1.00
8	10	50	30	0.05	100	0.530	0.106	0.0	1.00

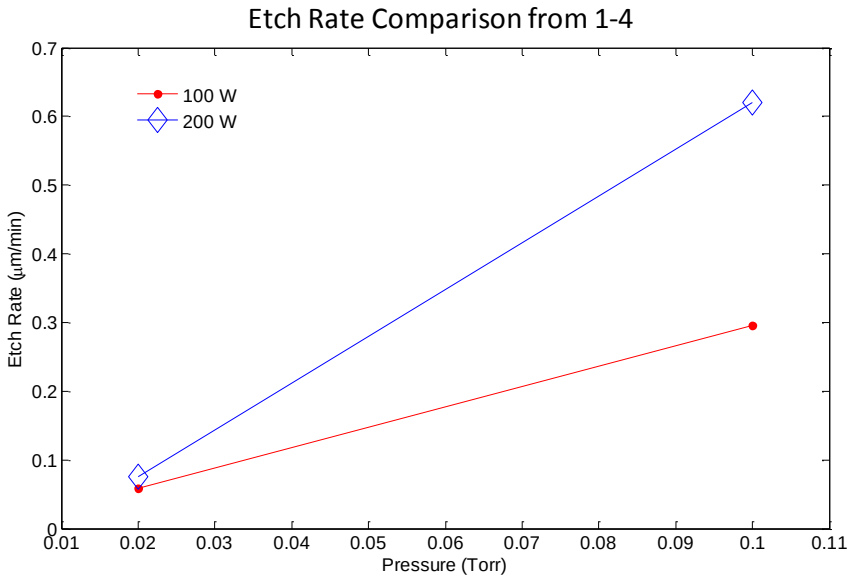

Figure 34. Comparison of recipes 1-4 showing the impact of RF power and pressure.

To further improve the recipe using 0.05 Torr and 150 W from the results obtained in Table 8, the SF_6 flow rate was increased from 10 sccm to 15 sccm to improve the etch rate. By utilizing all the obtained data, an estimated time of 25 minutes was estimated and set to achieve ~5 µm. Once these changes were made, Figure 35 shows that the 25 minute etch met the goal of etching 5 µm showing an etch rate of ~0.196µm/min. Even though a 5µm etch was achieved, some undercut was observer were the degree of anisotropy was 0.89.

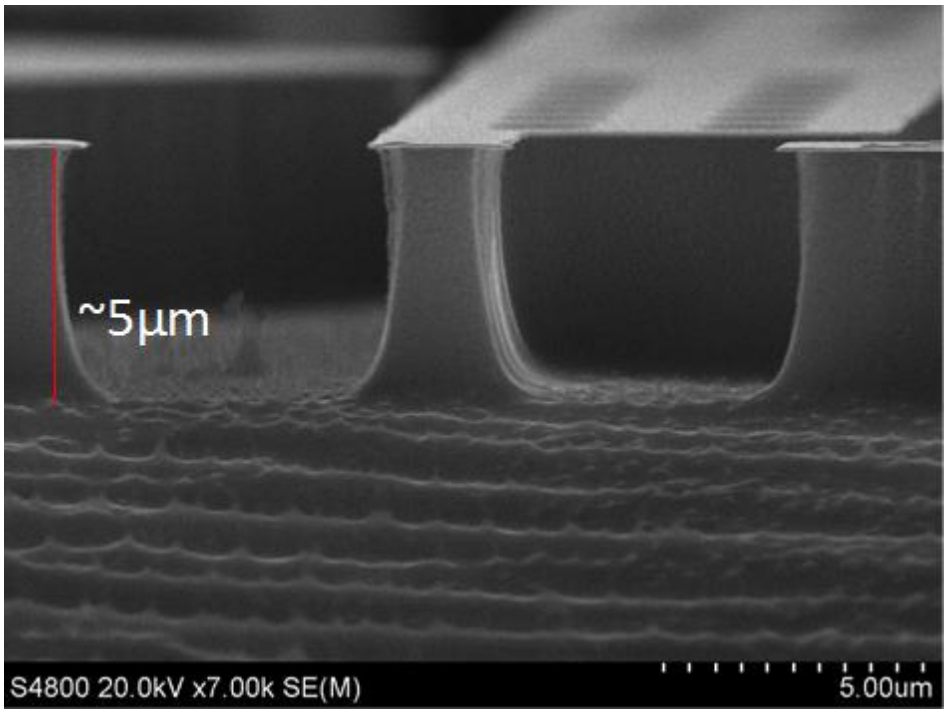

Figure 35. Etching results of increasing SF_6 flow rate to achieve 5 µm etch depth

To improve the degree of anisotropy and maintain a reasonable etch rate, the pressure was lowered and set to 0.04 Torr while the power was increased to 225W running for 30 minutes, trying to compensate the changes maintaining a reasonable etch rate. As expected the etch rate did lower, changing from ~0.196µm/min to 0.1µm/min as seen in Figure 36, where the profile is more anisotropic and the etch depth was 3 µm instead of 5 µm. Even though the etch rate lowered, this new results obtained gave a reasonable etch rate for further development and optimize the recipe. Knowing that RF power has a greater impact at this level of pressure, the power was increased to 250 Watts. As a result an average of 7.6 µm silicon etch was achieved by a 30 min run. Interestingly enough, the etch rate closely matches the predictions for such pressure and such power level. However, a lag between 1-2µm exists from the wider features to the smaller gaps, which is clearly observable in Figure 37. The larger features are 5µm wide trenches, while the smallest features are ~.6µm gaps. Moreover, this lag is tolerable for the SOI wafers, since the underlying SiO_2 will stop the etching. In addition, even if the bottom of the trench gets a notch, this is still tolerable.

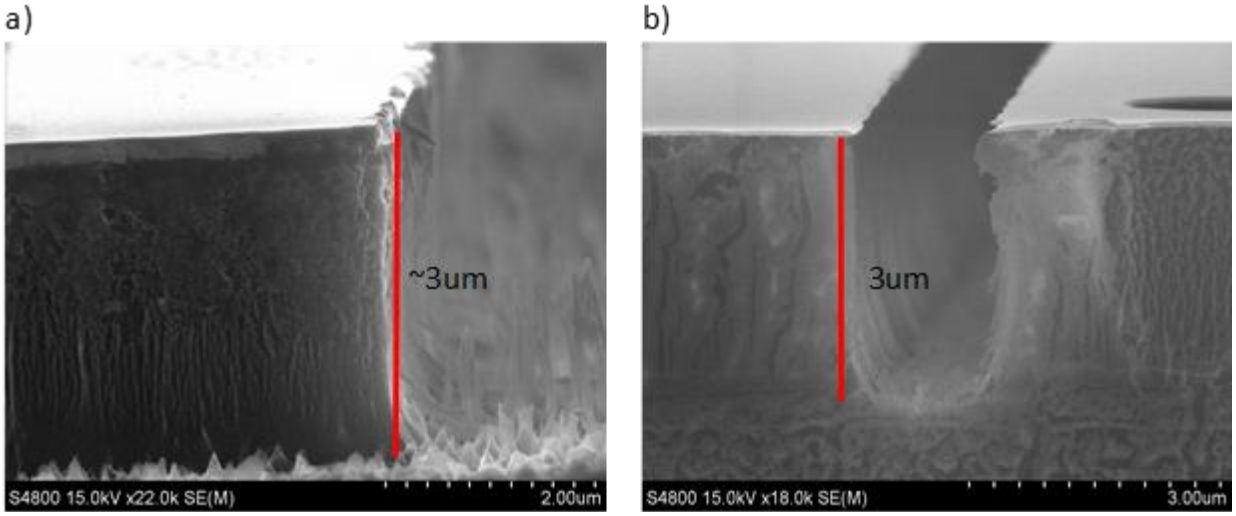

Figure 36. Si sample etching results after reducing pressure and increasing power.

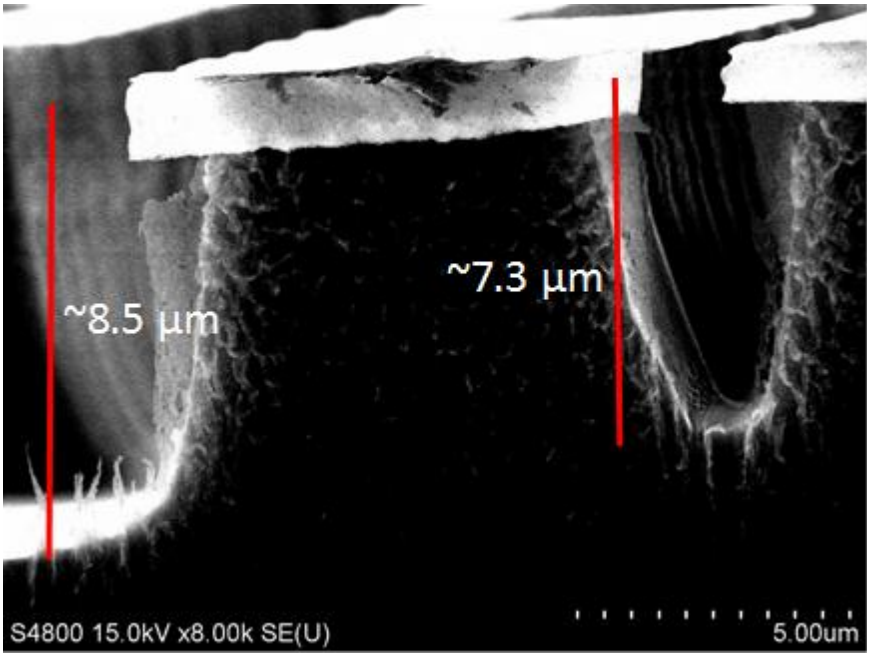

Figure 37. Si sample showing over 5 µm and lag between two different trench widths.

During the analysis of the SEM pictures and data, it was noticed that the silicon sidewalls were not as smooth as expected. This roughness can be observed as vertical undulations. Another observation was that the nickel did not present a rectangular profile at the edges. The roughness of the walls is hard to measure as observed in Figure 38, where a cross-sectional view is seen at an angle, making it difficult to observe the roughness in the out of plane direction. However, the

undulations can be observed at the in-plane direction, hence the difficulty to measure such roughness. This roughness is a product of the photoresist during the lithography process. When the nickel is deposited, it obtains such pattern from the photoresist. Regarding the roundness of the nickel at the edge of the etched trenches, its explanation comes from the deposition itself. Nickel can withstand the etching process utilizing SF_6 gas mixtures, becoming a suitable metal for a hard mask. However, when doing thermal evaporation several issues can occur. One is related to the aspect ratio between the height and width of the features. This can create a poor filling at the bottom [35]. Another, possible contribution is the fact that the metal once deposited tends to spread out, hence the formation of the rounded corners, as depicted in several examples for PVD in [35].

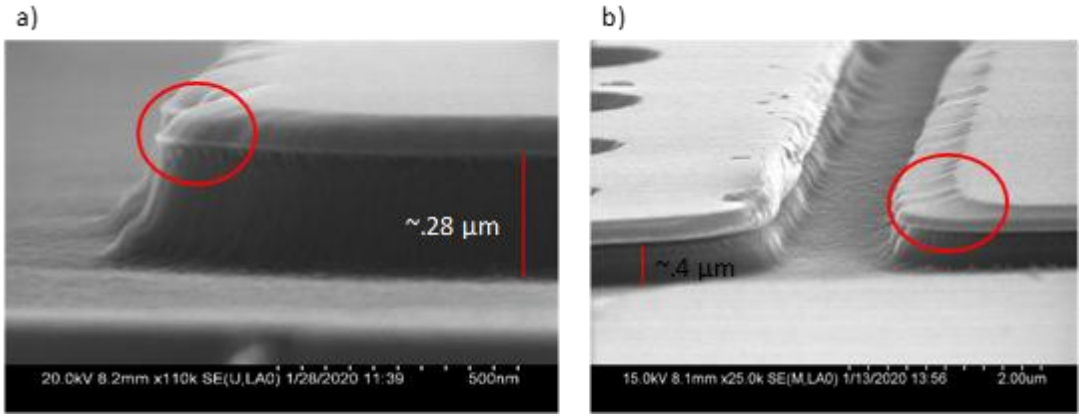

Figure 38. Observations of rounded corners in nickel in both a) and b) during etch process.

Once all the data was thoroughly analyzed and a recipe was optimized, an SOI wafer became ready to be etched, however, prior to the etching process, a dicing procedure is done. The etching is done at a die level and not at wafer level. This is to maintain consistent etching results and avoid larger lags. The dicing procedure was done at UACJ using a saw machine. During the dicing step, the wafer is covered in photoresist to protect it from silicon dust and any other damages. The sample die should be thoroughly cleaned before etching the sample. If a proper cleaning is not done, then undesirable results may be obtained.

Lastly, after dicing, cleaning and removing the native oxide, an SOI sample was etched following the recipe in Table 9. $SF_6/Ar/O_2$ with flow rates of 15/50/30 sccm respectively, 0.04 Torr, and 250W for RF power were set. The etching time was of 20 minutes calculated from the etching rate of 0.253µm/min, taking the average of 7.6 µm from the 30 minutes etch cycle, providing an estimation of 5.06 µm etch. However, the device layer was etched almost completely (as seen in Figure 39) to the SiO_2 layer. To achieve the 5 µm depth, an over etch run of 21 minutes could be done, where it will be sufficient and still prevent any undesirable undercut between the silicon and oxide layer interface.

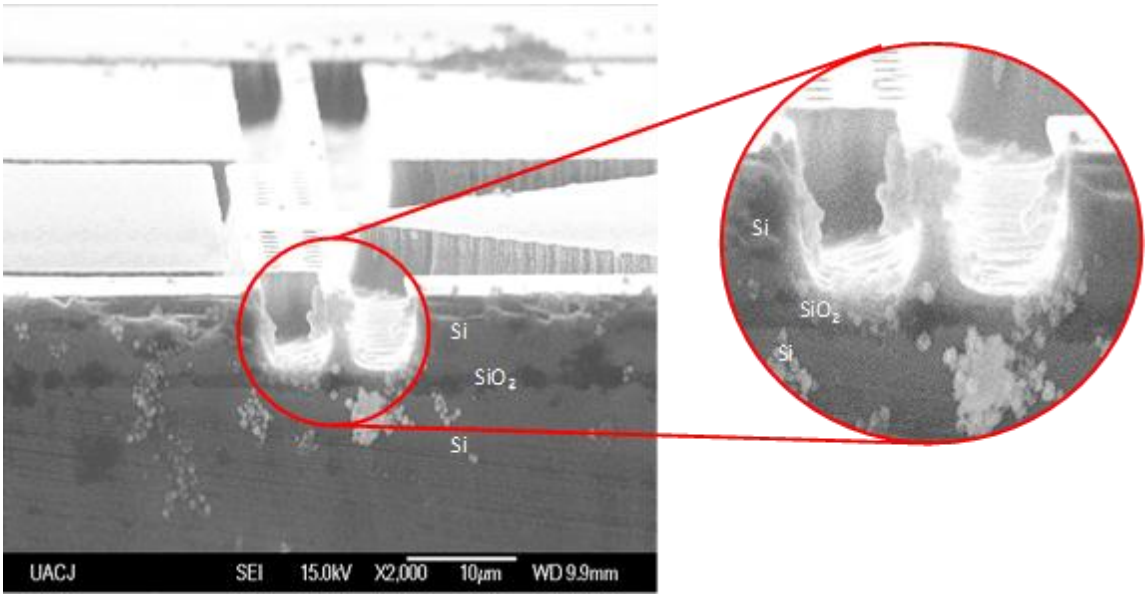

Figure 39. SOI die etched using optimized recipe reaching ~5 µm.

Table 9: Silicon etching recipe

SF_6 (sccm)	**Ar (sccm)**	**O_2 (sccm)**	**Power (Watts)**	**Pressure (Torr)**	**Etch Rate (µm/min)**
15	50	30	250	.038	0.253

Chapter 6: Conclusions and Future work

The exhaustive work done to study 2-D materials, by exploring its mechanical properties to exploit their potential for future electronics, and the promising results seen in [1, 10, 11, 34, 12] have become very attractive. The concept of a MEMS-TMDC device successfully managed to confirm theoretical and experimental data. However, due to poor yield and other fabrication problems, a motivation to redesign and develop a fabrication process has become a motivation for future iterations.

The use of SOI is a very common practice for the fabrication of MEMS. Due to the accessibility and the existence of technology to process silicon, it provided the opportunity to develop a process that could be followed by next generations. Moreover, by having an easy and reproducible process it will help improve the design as well.

A large effort was done to develop such process as a legacy for The University of Texas at El Paso. It was proven that UTEP has the fabrication capabilities to develop a process for a MEMS-TMDC device. Yet, a complete device is still in working process, where the transferring of the TMDC and a release step utilizing either a critical dry release, or, an HF vapor process are still required. However, this work demonstrates the capability to do this and create a safe working environment for future research students.

To conclude, as the process gets further optimized, and with the capabilities of new technologies, a MEMS-TMDC device can be fabricated to surpass the 3.3% strain record that has been achieved in previous work [11]. Finally, this work developed a MEMS fabrication process at UTEP's Nanofabrication Facility for the first time.

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Vita

Edgar Acosta was born in El Paso, Texas, a border city between Mexico and the United States. He grew up in both sister cities, El Paso and Ciudad Juarez. Ever since elementary school Edgar has been awarded for his excellence as an outstanding student and interest in the STEM field. During his high school education, Edgar started his quest in the Electrical and Electronics Engineering field by taking an optional workshop throughout all his high school years. He then started his college education at The University in Texas, where he earned his B.S. in Electrical and Computer Engineering in December 2017 with a Cum Laude. During his undergraduate career Edgar started his research experience as an ETERN, a program from the Center for Energy Efficient Electronics (E3S). He then got a summer REU at the University of California, Berkeley learning about the ongoing research in N/MEMS for ultra-low power applications.

He then decided to pursue his Master's in Electrical Engineering under the supervision of Dr. Zubia. He is currently working as a graduate research assistant in the NanoMIL laboratory at UTEP working on the development of a fabrication process for MEMS. As part of the center, intensive collaboration was done on a regular basis and resulted in two multi-institutional publications. As part of the project, a new device had to be designed, fabricated, and characterized using a variety of different tools in which he spent a second summer at UC Berkeley.

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