2009-01-01

Design of a Low Voltage Analog to Digital Converter

Praveen Kumar Palakurthi
University of Texas at El Paso, pkpalakurthi@miners.utep.edu

DESIGN OF A LOW VOLTAGE ANALOG TO DIGITAL CONVERTER

PRAVEEN KUMAR PALAKURTHI

Department of Electrical and Computer Engineering

APPROVED:

Eric MacDonald, Ph.D., Chair

John Moya, Ph.D.

Ryan Wicker, Ph.D.

Patricia D. Witherspoon, Ph.D.
Dean of the Graduate School

Dedication

This thesis is dedicated to my family with love.

DESIGN OF A LOW VOLTAGE ANALOG TO DIGITAL CONVERTER

by

PRAVEEN KUMAR PALAKURTHI, B. Tech.

THESIS

Presented to the Faculty of the Graduate School of

The University of Texas at El Paso

in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE

Department of Electrical and Computer Engineering

THE UNIVERSITY OF TEXAS AT EL PASO

December 2009

Acknowledgements

I would like to thank my supervising professor Dr. Eric MacDonald for his encouragement, guidance and support throughout the entire course of this research. I feel that he has given me immense practical exposure to circuit design and test concepts and has taught me the basics of carrying out quality research. I consider myself very fortunate to have had a chance to work under his guidance and supervision. Thank you very much for giving me an opportunity to work in your research group. I believe that I have learnt a lot in these years as a graduate student.

I would also like to thank my other committee members – Dr. Moya and Dr. Wicker for being on my defense committee and giving me valuable suggestions and comments. Additionally, I would like to thank the faculty and staff of Electrical and Computer Engineering Department for their direct or indirect support towards my graduate studies.

Additionally, I want to thank The University of Texas at El Paso Electrical Department professors and staff for all their hard work and dedication, providing me the interest to apply for the Doctoral Degree here at University of Texas at El Paso.

Special thanks to my co-workers Sujith Chakra Chidurala, Miguel and all my friends here at El Paso for being supportive.

And finally, I must thank my parents -Mrs. Lakshmi Palakurthi and Rama Rao Palakurthi for their blessings, love and constant words of encouragement throughout my career. Thanks to my brother Raghavendra Rao Palakurthi for his advice and best wishes. They play a very important role in every aspect of my life.

Abstract

For the past 40 years, the number of transistors per chip has been increasing at an exponential rate confirming Moore's Law regarding the growth of chip complexity. Increases in transistor count have led to enhancements in functionality and made possible products with features that were unimaginable ten years ago. Consequently, the resulting increase in digitization in all electronics, across a wide range of applications, requires the Analog-to-Digital Converters (ADCs) with a higher resolution and lower power consumption. The evolution of the integrated circuit technologies and scaling methodologies partially helps in providing faster circuits and allowing complex functionalities in a given silicon area.

The objective of the present work is to better understand the design of ADCs in the context of low voltage operation as a function of temperature, speed and power consumption. However, one requirement in designing faster circuits with transistor of smaller geometries is reducing the supply voltages. Additionally, the increase in the number of battery-operated applications has focused in reducing the supply voltage in current designs to improve energy efficiency. Few low voltage methodologies have been studied and implemented for analog circuits in general and more specifically for ADCs. In the present work, an ADC was designed which implemented the Successive Approximation (SAR) method – based on a binary search. The functionality of ADC was tested in simulation by applying a DC voltage and a ramp signal as the input and analyzing the resulting output digital codes. The power consumption at different temperatures and supply voltages was recorded and analyzed. The results indicate that the effect of temperature on power consumption is significant.

The SAR ADC was designed for TSMC 0.25µm CMOS technology. The design of the ADC at the schematic level was captured in Virtuoso Cadence. Cadence offers an integrated Electronic Design Automation (EDA) solution, which encompasses the entire design flow from behavioral modeling to

post-layout simulation. The Spectre simulator from Cadence was used to analyze the behavior of the ADC at different voltages and temperatures through simulation. Finally, a built-in Cadence calculator was used to calculate the power consumption and Spurious-free dynamic range (SFDR) at different voltages and temperatures to compare the design to previously reported ADCs.

The ADC was simulated at 27 ºC with the sinusoidal signal as the input. The input sinusoidal signal has 0.5 V P-P running at frequency of 500 Hz. The SFDR and the power consumption for the ADC at these conditions were calculated to be 40.56 dB and 2.5640 µW respectively – a 63% decrease in power consumption in the proposed design relative to the leading ADC reported in literature with 60 times decrease in speed.

Table of Contents

List of Tables

List of Figures

Chapter 1: Introduction

1.1 Motivation

In the last few decades the geometries of silicon have been reducing providing both higher densities of transistors on silicon and simultaneously improving the transistor drive current – both of which have permitted the clock frequency to increase in digital circuits. Consequently, for the last two decades, Digital Signal Processors (DSPs) have become increasingly more powerful in terms of computation. With evolving Integrated Circuit (IC) technology, the possibility exists now to implement new DSP functionalities in an efficient manner. Signal processing that had traditionally been implemented in analog is now implemented in the digital domain. The digital domain increases robustness, decreases power consumption and area, speeds up the design process and increases accuracy.

However, natural signals are in analog form. The input signals to be processed and the output signals after processing are analog while the intermediate processing is done in the digital domain. Hence, there exists a need to convert the signals at both ends of the signal pathway to take advantage of DSPs. The circuit used at the input is an Analog-to-Digital Converter (ADC) whereas the output is the Digital-to-Analog Converter (DAC).

Increase in digitization and the necessity for converters require analog and digital circuits to share the same silicon, which leads to new challenges. Every new technology (i.e. shrinking feature size, finer widths, denser interconnect and more routing layers) increases the digital functionality on silicon. New applications demand higher clock frequencies but with the engineering trade-off of additional power consumption. Moreover, the decrease in feature size also results in various problems such as RC effects, voltage drop, increased power dissipation and reduced signal integrity.

With the increase in the number of battery-operated applications, interest has been focused on reducing the supply voltage and developing low voltage design methodologies and a significant

challenge exists in designing an ADC is low voltage operation. To design an ADC at low voltages, several challenges must be overcome such as process scaling, power consumption, switches, noise and transistor matching. These issues manifest themselves differently for analog circuits than for digital circuits.

1.2 Organization of the Thesis

This work concentrates on the design of ADC at low voltages. The organization of the thesis is as follows:

Chapter 2 studies the effects of supply voltage and process scaling on signal to noise ratio, circuit speed and power consumption.

Chapter 3 discusses the selection of the Successive Approximation Register (SAR) algorithm as the well-suited ADC and describes the ADC operation.

Chapter 4 describes the design of an ADC for low voltage operation and also describes the operation and design conditions for sub-circuits such as the sample and hold (S/H), operational amplifiers (op-amp), comparators and digital to analog converter (DAC).

Chapter 4 discusses the analysis of the results.

Chapter 5 provides the conclusions.

Appendix shows the schematics of the circuits used for the design.

Chapter 2: Background

2.1 Low Voltage Challenges

The two motivations for technology scaling are reduced area and increased speed. However, as geometries shrink, the maximum electric field across the gate oxide eventually approaches the intrinsic breakdown of silicon oxide. Consequently, along with geometry scaling, there must be a corresponding scaling of the voltage and lower voltages are not well-suited for analog circuits. Due to the rise in the level of integration, the power dissipation of a single chip also tends to rise. The total power dissipation in a circuit [1] is expressed as:

$$P_{total} = \alpha_T . C_{load} . (V_{DD})^2 . f_{CLK} + V_{DD}(I_{SC} + I_{leakage} + I_{static}) - - - - - - - (2.1)$$

Where V_{DD} is the supply voltage, C_{load} is the load capacitance, f_{CLK} is the clock frequency. From the above expression that the total power dissipation depends on V_{DD} (supply voltage). Hence, one efficient approach to reduce the power consumption is by lowering the supply voltage – particularly for digital circuits.

2.1.1 Process Technology Scaling

The scaling of the supply voltage VDD is the most pronounced affects in sub-micron analog design. Table 2.1 shows the parameters of different process technologies. The data, including the effective channel length, supply voltage, oxide thickness, threshold voltage, and threshold voltage matching parameter, is collected from real processes and reprinted here from [2]. However, in analog circuits the reduction of power consumption through lowering supply voltages is more complicated. The limitations of power consumption in different types of analog circuits are discussed in [3]-[4], and data

converters in [5]. Several low voltage circuit techniques have been discussed previously in [6] and [7] and for ADCs [8].

Table 2.1: Technology Data for Different Processes

Sno	Lmin	Vdd	Tox	Vth	AVth
1	3.0	5.0	700	1.5	35
2	2.5	5.0	600	1.2	30
3	2.0	5.0	400	1.1	25
4	1.5	5.0	250	1.0	22
5	1.2	5.0	250	1.0	21
6	1.0	5.0	250	0.95	20
7	0.8	5.0	200	0.85	13
8	0.5	3.3	135	0.73	11
9	0.35	3.3	100	0.59	9
10	0.25	2.5	60	0.52	6.0
11	0.18	1.8	50	0.42	4.2
12	0.12	1.2	42	0.32	3.8
13	0.10	1.2	36	0.31	3.2
14	0.07	0.9	30	0.30	2.5

2.1.2 Signal to Noise Ratio

One of the important fundamental differences in the analog signal processing when compared to the digital signal processing is thermal noise [9]. Thermal noise limits the smallest distinguishable signal. On the other hand, the supply voltage limits the amplitude of the signal [10].

For a sinusoidal signal the peak signal-to-noise ratio is determined by:

$$\sqrt{SNR} = \frac{V_{signal}}{V_{Noise}} = \frac{V_{\max}}{2 * \sqrt{2} * V_{RMSNoise}} \text{----------(2.2)}$$

Where V_{max} is the maximum peak-to-peak signal amplitude and $V_{RMSNoise}$ is the noise voltage. Lowering the supply voltage results in the decreased signal-to-noise ratio unless the noise level is scaled down simultaneously. Thermal noise remains largest component of noise. Therefore, one approach to reduce noise is cooling, which reduces the ever-increasing thermal component [10].

2.1.3 Power Consumption

The important advantage in low voltage circuits is power consumption. If the supply voltage is scaled down while all other parameters are kept constant, the propagation delay will increase. The average switching power dissipation is proportional to the square of the supply voltage; hence, reduction of V_{DD} will significantly reduce the power consumption with a quadratic relationship. However, this assumes that the switching (operating) frequency remains constant. If the circuit is always operated at the maximum frequency allowed by the propagation delay – which is generally slower at lower voltages, the number of switching events per unit time (i.e., the operating frequency) will drop as the propagation delay becomes larger with reductions of the supply voltage. Therefore, the dependence of switching power dissipation on the supply voltage becomes stronger than a simple quadratic relationship [1].

2.1.4 Circuit Speed

Low voltage circuits are slower than the high voltage circuits. The speed of analog circuits is not usually dependent on the supply voltage. However, if the dynamic range is kept constant while decreasing the supply voltage then the capacitance has to increase to allow the circuit to run at less speed [10].

In switched capacitor circuits the maximum clock frequency is inversely proportional to the settling time, which is determined by slew rate and op-amp bandwidth.

For a single stage op-amp the gain bandwidth product is given by:

$$GBW = \frac{g_m}{2\pi C_L} \text{----------(2.3)}$$

Where g_m is the transconductance of the input transistor and CL is the load capacitance, which can be approximated to be proportional to the sampling capacitor C. Thus,

$$GBW = \frac{g_m V_{DD}^{\ 2}}{k_3 DR.k_1^{\ 2} KT} \text{ ---------- (2.4)}$$

When the settling time is dictated by the op-amp GBW, then the speed of a circuit can be reduced with the square of the supply voltage.

For low resolution circuits, the settling time depends on slew rate (SR),

$$SR = k_4 \frac{V_{\max}}{T_{clk}} = \frac{I_{SR}}{C_L} \text{ ---------- (2.5)}$$

Where T_{clk} is the clock period and ISR is the slewing current, T_{clk} is given by:

$$T_{clk} = \frac{k_1^{\ 2} k_3 k_4 DR^2 KT}{I_{SR} V_{DD}} \text{ ---------- (2.6)}$$

The above expression indicates when slewing current is kept constant then the clock rate decreases linearly with the increase in supply voltage [10].

2.1.5 Switches

The important fundamental block in circuits is the switch. An ideal switch has infinite impedance when is open and has zero impedance when is closed. At higher voltages, the switch behaves approximately similar to the ideal but when the supply voltage scales down then the problems arise in the functioning of a switch.

The on-resistance of a MOS switch is approximated by:

$$R = \frac{L}{\mu_n C_{ox} W (V_{GS} - V_T)} when V_{GS} \geq V_T \text{ ---------- (2.7)}$$

Where V_{GS} is the transistor gate-source voltage and V_T is the threshold voltage. When V_{GS} is less than V_T (switch is turned off), the resistance is infinite essentially with only the sub-threshold leakage. To turn on the switch, its gate-source voltage has to greater than or equal to its threshold voltage.

The transistor cannot conduct the whole rail-to-rail signal range when is ON. For example, the NMOS cannot conduct logic 1 properly. Similarly, PMOS cannot conduct logic 0 properly. However, the whole range can be covered by putting an NMOS and a PMOS in parallel to form a transmission gate.

The threshold voltage decreases linearly with the technology scaling until 0.35 µm. The threshold voltage cannot be scaled down linearly with the supply voltage because of increasing leakage current. The leakage current increases exponentially with linear decrease in VT. The threshold voltage values from 0.35 µm to 0.07 µm generations in Table 2.1 fit accurately to $0.32.\sqrt{VDD}$ [10].

The on-resistance can be reduced by lowering the threshold voltage or increasing the supply voltage.

2.2 Previous Work

Many papers have been published in the design of ADCs with an aim to operate at low voltage in order to reduce the power consumption [14-18]. This chapter discusses some of the proposed methods and analyzes their pros and cons.

In [14] the author has employed a new biasing scheme and current-mode approach to design a low-voltage S/H, DAC, and a latched comparator. The design in [14] was implemented in 1.2 µm CMOS process technology. The S/H used poly resistors in this design to achieve the highly linear gain. The proposed S/H circuit is shown in fig. 2.1 [14].

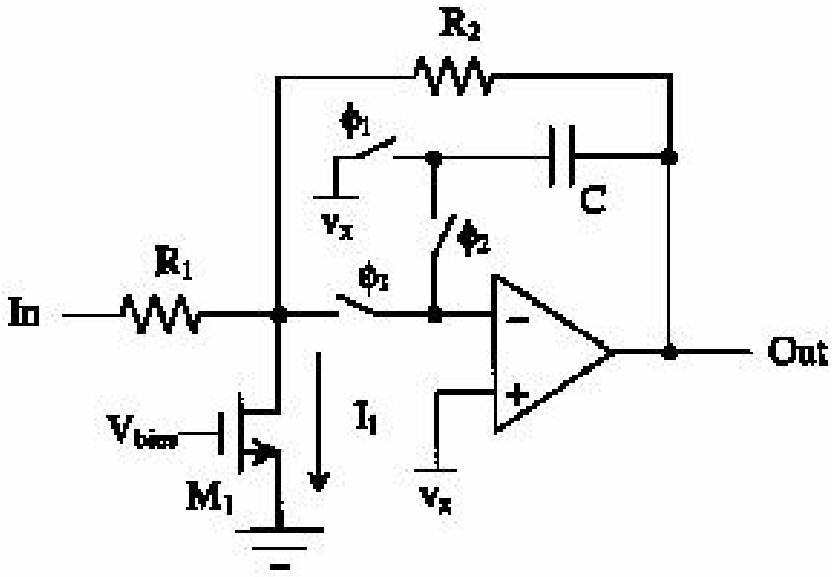


Figure 2.1: S/H with Poly Resistors at Input and Output.

R-2R architecture is used for the DAC to implement in the low-voltage. In the normal R-2R DAC, one op-amp is used at the output. However, in the proposed design, two op-amps were used so that one of the outputs can be used for measuring the performance of the DAC. The proposed DAC is shown in fig. 2.2 [14].

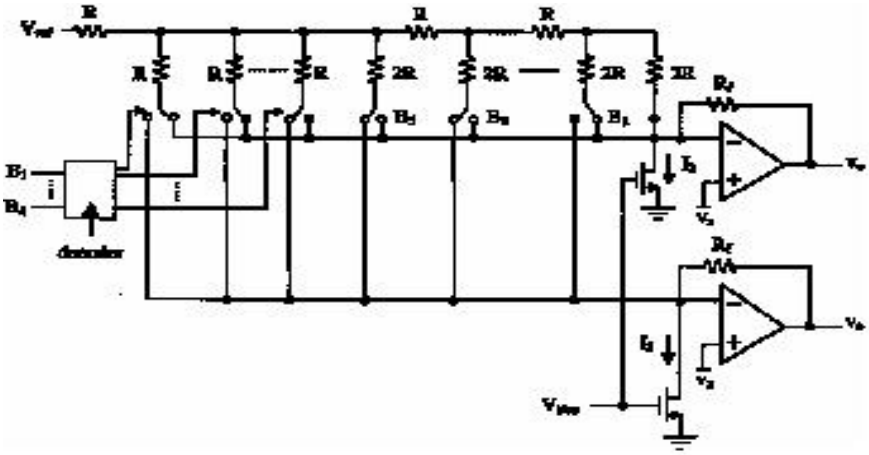


Figure 2.2: Proposed R-2R DAC.

The R-2R DAC is fast, suitable for low-voltage design. However, the R-2R architecture is not accurate. The DAC used in the present work is the Charge scaling DAC, which is fast and accurate. The DAC in the present work doesn't have an op-amp at the output, which increases the speed of the DAC. Thus, the speed of the DAC in the present work depends only on the delay of the capacitors.

In [15] the author describes time-interleaved SAR ADC with an aim to achieve the high speed at low voltages for the UWB applications – where the minimum power consumption is required. The proposed ADC block diagram is shown in fig. 2.3 [15].

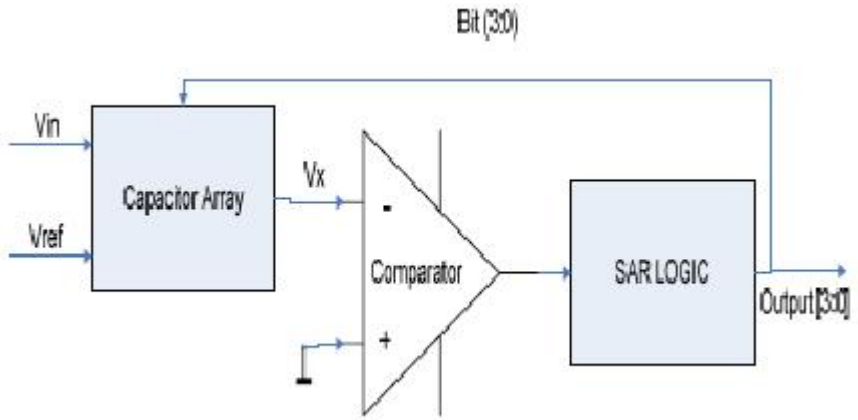


Figure 2.3: Block Diagram of Proposed ADC DAC.

As shown in fig. 2.3, the SAR ADC in this design consists of three blocks: capacitor array, comparator and a digital block. The capacitor array acts as both DAC and S/H. The output of the capacitor array is connected to the comparator, which compares the signal to the ground. The capacitor array used in this design is shown in fig. 2.4 [15].

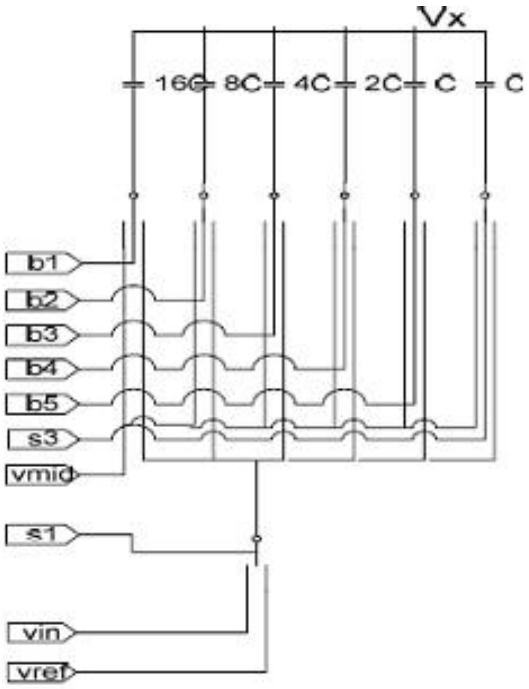


Figure 2.4: Proposed Capacitor Array.

The comparator used in this design is a basic single stage differential pair op-amp with active load. The drawback of this design is the comparator requires high gain and slew rate to maintain virtual ground in the feedback mode. The design proposed in the thesis work has the latch circuit at the output of the comparator. The latch at the output stage provides a large and fast output signal whose amplitude and waveform are independent of those of the input signals [16]. The comparator doesn't require a large gain when the latch is used at the output.

In [18] the author proposed energy-saving switching sequence technique to achieve low power consumption for Bio-Medical applications. The proposed SAR ADC architecture is shown in fig. 2.5. The drawback in this design is the comparator requires high gain. The design used in the thesis work has a latch at the output stage of the comparator.

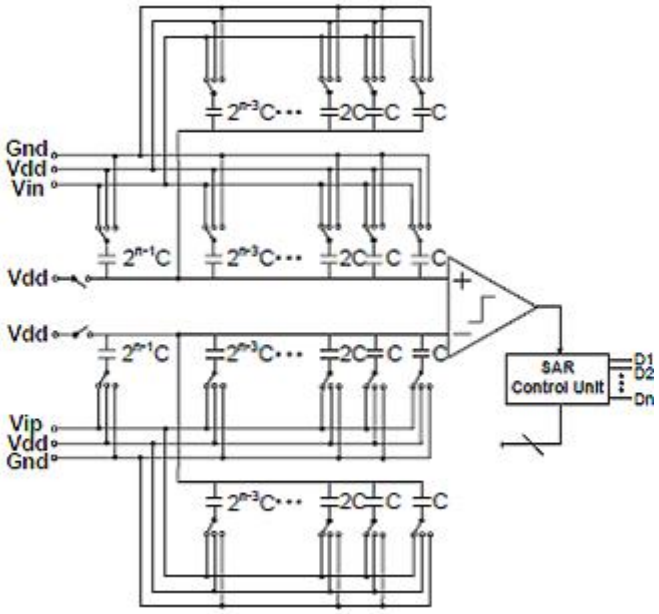


Figure 2.5: Proposed SAR ADC Architecture.

Chapter 3: Successive Approximation Analog to Digital Converter

To identify the most suitable ADCs for use in low voltage operation, this chapter explores several commonly used ADCs in industry and provides a comparison.

Types of Analog to Digital Converters used in industry include:

1. Pipelined
2. Flash
3. Sigma-Delta
4. Successive Approximation ADC

This work mainly concentrates on identifying ADCs that perform well with low voltage and provide low power, high resolution and high accuracy. After studying on the above mentioned types of ADCs, SAR ADC is the best fit, which includes 8 KS/s with 8 bits at 0.8 V. Ideally, an ADC that would work in the subthreshold regime would be preferably as the ADC would be capable of sharing a very low supply voltage subthreshold digital circuit. The first step in identifying a subthreshold ADC, however, is identifying an ADC that would perform well in the just-above-subthreshold regime, where the possibility of using a charge pump exists for generating the higher supply voltage.

3.1 Successive Approximation (SAR)

Successive approximation employs a “binary search” and is used in determining an unknown weight by a minimal sequence of weighing operations [11]. The binary search continues until every bit in the SAR has been tested. The resulting digital code is the approximation of the sampled input voltage.

Mathematically, let $V_{in} = xV_{ref}$, with x in [-1, 1] is the normalized input voltage.

The objective is to approximately digitize x to an accuracy of 1/2n. The algorithm proceeds as follows:

1. Initial approximation x0 = 0.

2. *i*th approximation xi = xi−1 − s(xi−1 − x)/2i

Where, s(x) is the signum-function (sgn(x)) (+1 for x =0, −1 for x < 0). It follows using mathematical induction that |xn − x| =1/2n [19].

1. As shown in the above algorithm, a SAR ADC requires:

2. An input voltage source V_{in}.

3. A reference voltage source V_{ref} to normalize the input.

4. A DAC to convert the ith approximation xi to a voltage.

5. A Comparator to perform the function s (xi − x) by comparing the DAC output voltage with the sampled input voltage.

6. A Register to store the output of the comparator and apply xi−1 − s (xi−1 − x)/2i.

SAR ADCs versus other Architectures

1. Versus Pipelined: A pipelined ADC uses a parallel structure in which each stage works on one to a few bits. This structure increases throughput, but at the expense of power consumption and latency. An N-bit Pipelined ADC consists of N comparators for determining the signs of the N outputs (for digital correction). On the other hand, a SAR ADC requires one comparator for the accuracy of whole system. A pipelined ADC requires more silicon area then SAR ADC [20].

2. Versus Flash: A flash ADC is made up of a large bank of comparators, each consisting of wideband, low-gain preamps followed by a latch. The comparators have to be accurate. The flash ADCs are the fastest architecture. The trade-off of these converters is with power consumption and form factor. In a flash ADC the number of comparators goes up by a factor of two for each bit and requires far more accuracy for every extra bit of resolution above eight bits increasing the complexity. On the other hand, in a SAR ADC, increasing in resolution requires more accurate components without increasing the complexity exponentially [20].

3. Versus Sigma-Delta: Sigma-delta converters are over sampling converters. This converter requires no special trimming or calibration, even to attain 16 or 18 bits of resolution. The over sampling nature of the sigma-delta converter may also tend to "average out" any system noise at the analog inputs [20]. The trade-off of these devices is its speed which is reduced logarithmically with the number of bits and these converters consume a lot of silicon area.

3.2 Functional Description of Analog to Digital Converter

In this chapter the components required to build a SAR ADC are discussed. As explained in the previous section, a SAR ADC requires a sample-hold, DAC, Comparator and a digital logic SAR are shown in fig. 3.1. Transistor level schematics for every block are presented in this chapter.

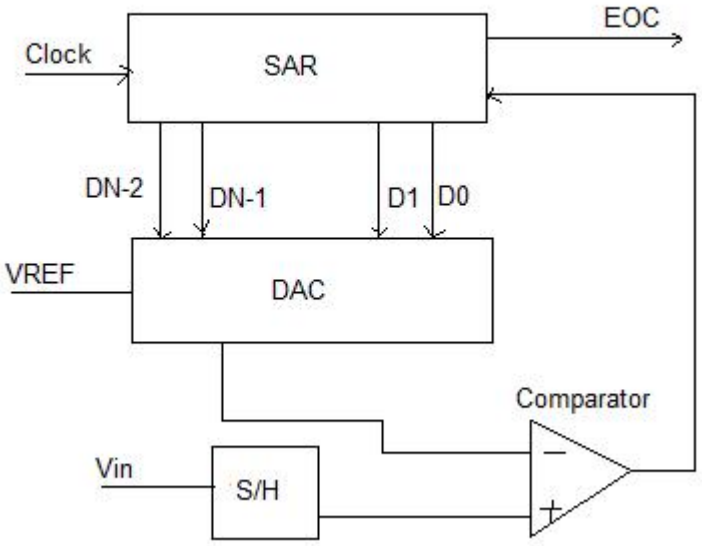


Figure 3.1: Block Diagram of SAR ADC.

3.2.1 Nonredundant Successive Approximation Register (SAR)

The digital component of the SAR ADC is a SAR. The basic SAR block composed of a shift register, memory register and a sequential finite state machine (FSM). A non-redundant SAR is simple and codes the 2^N possible conversion output values with the minimum number of flip flops (FF) ($\log 2^N$) [21]. Non-redundant SAR allows area optimization while reducing minor code probability error. The delay is reduced during the conversion because of the fewer number of flip flops in the design. The logic between the shift register and memory register is reduced which in turn results in reducing the delay. The FSM can be implemented using a counter. The usage of counters increases the speed and performance of the Successive Approximation register.

The proposed non-redundant SAR in [21] uses the minimum number of flip flops; this can be achieved using the same number of FF storing the conversion result to code the 2^N possible states of the FSM. For the total number of 2^N states N flip flops are required.

SAR Operation

As discussed in the previous sections, the operation of a SAR is based on a binary search. At the beginning of the conversion (initialization) the MSB of SAR is set to ’1’ and all other bits are set to ’0’. This digital word is applied as input to the DAC. This analog output from the DAC is compared with the sampled analog input. If this compared result is high, the SAR makes the MSB ’1’. If the compared result is low, the SAR makes the MSB ’0’. The process of applying the digital word to the DAC continues. As the MSB is obtained, the second bit is assumed to be at ’1’ and the remaining bits at ’0’. The comparison and applying to the DAC continues until the whole digital word is obtained.

The functionality of SAR can be defined as a sequential finite state machine (FSM), which generates the sequence of N steps. Each conversion step corresponds to a state of the FSM. Step 0 is the first state of conversion, which is the initialization state. From the Table 3.1, for a generic step, three actions are possible on a single bit: setting the bit to ’1’, setting the bit to comparator output, or storing the bit at the previous step. For these steps, some decoding and multiplexing logic are required and shown in fig. 3.2.

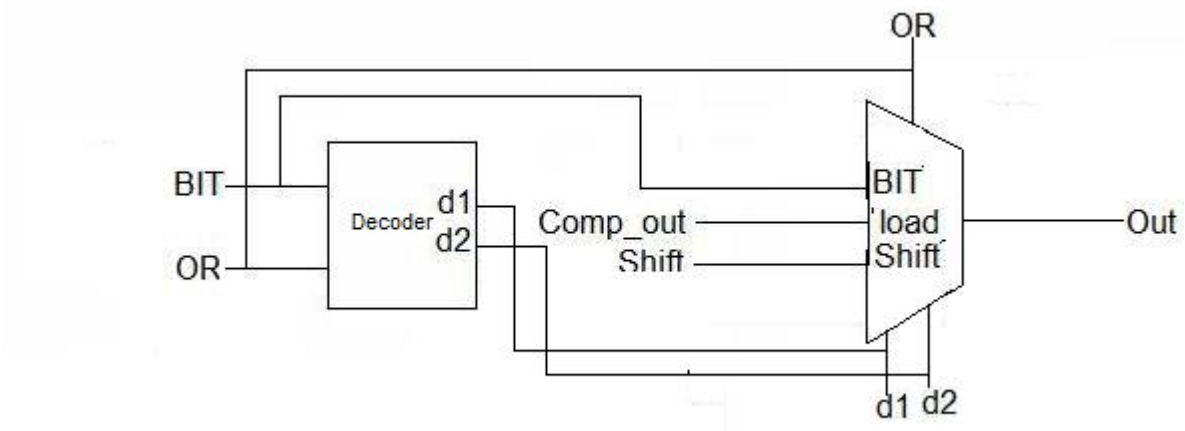


Figure 3.2: Decoder and Multiplexer.

Table 3.1: FSM Sequence

Conversion step	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	Comp Output
0	1	0	0	0	0	0	0	0	0	0	a_9
1	a_9	1	0	0	0	0	0	0	0	0	a_8
2	a_9	a_8	1	0	0	0	0	0	0	0	a_7
3	a_9	a_8	a_7	1	0	0	0	0	0	0	a_6
4	a_9	a_8	a_7	a_6	1	0	0	0	0	0	a_5
5	a_9	a_8	a_7	a_6	a_5	1	0	0	0	0	a_4
6	a_9	a_8	a_7	a_6	a_5	a_4	1	0	0	0	a_3
7	a_9	a_8	a_7	a_6	a_5	a_4	a_3	1	0	0	a_2
8	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	1	0	a_1
9	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	1	a_0
result	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	–

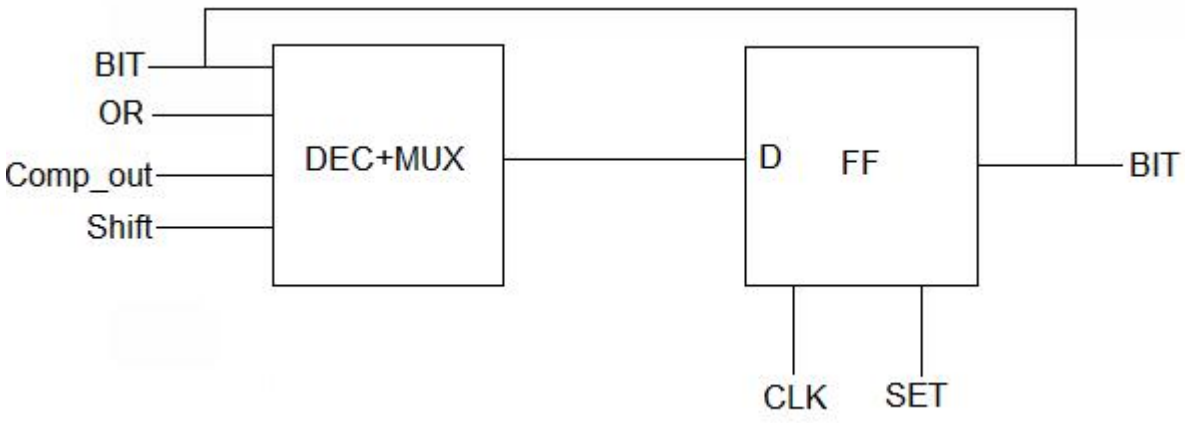


Figure 3.3: Generic Flip Flop with Shift Register.

Table 3.2: FF Outputs

	Previous Bit	Operation
1	-	Memorize Result (K)
0	1	Data Load (a)
0	0	Shift Right

The circuit in fig. 3.2 has a decoder and a multiplexer, which were used in setting the bit. The signal *Bit* is the bit from previous cycle, *OR* is output from logical OR of the previous bits. A generic flip flop, which performs all the functions, is shown in fig. 3.3.

The states that can be attained by the flip flop after decoding are shown in TABLE 3.2.

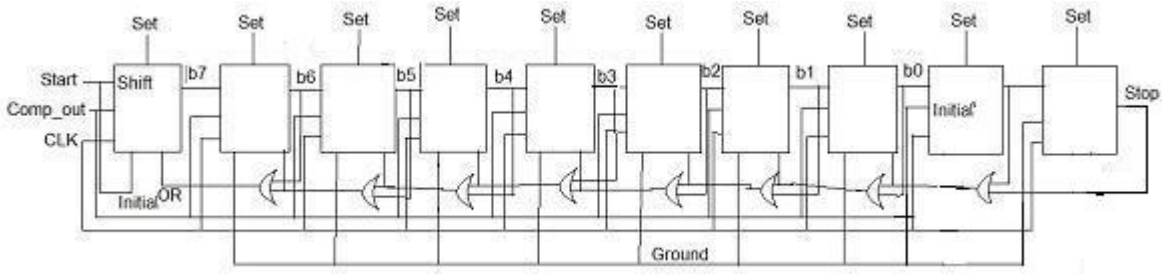


Figure 3.4: Successive Approximation Register (SAR)

SAR Circuitry

The basic structure of the SAR is a multiple input N bit shift register, which is shown in fig. 3.4. The multiplexer and decoder alone are not sufficient to select the value for the bit. The SAR circuitry requires some control logic. Referring to the algorithm for the Kth flip flop, the all zero state for the less significant bits than the Kth bit are decided by the OR chain of the outputs off the flip flop storing them.

SAR fundamentally needs to initialize the current MSB to ‘1’ and remaining bits to ‘0’. Initialization is done by “*set*” input of flip flop. Conversion starts when the “*start*” signal is enabled and the result is obtained once the conversion completes and then the “*stop*” signal is enabled.

The SAR codes the possible conversion output values with minor code error probability with a FSM using the minimum number of states. The SAR is designed using relatively simple circuitry, which helps in operating at higher speeds.

3.2.2 Charge Scaling Digital to Analog Converter (DAC)

Charge scaling DACs are the most popular Digital to Analog Converter architecture. The charge scaling DACs were used for the design due to increased accuracy and speed. Another advantage of the charge scaling DAC is that it is compatible with switched capacitor circuits.

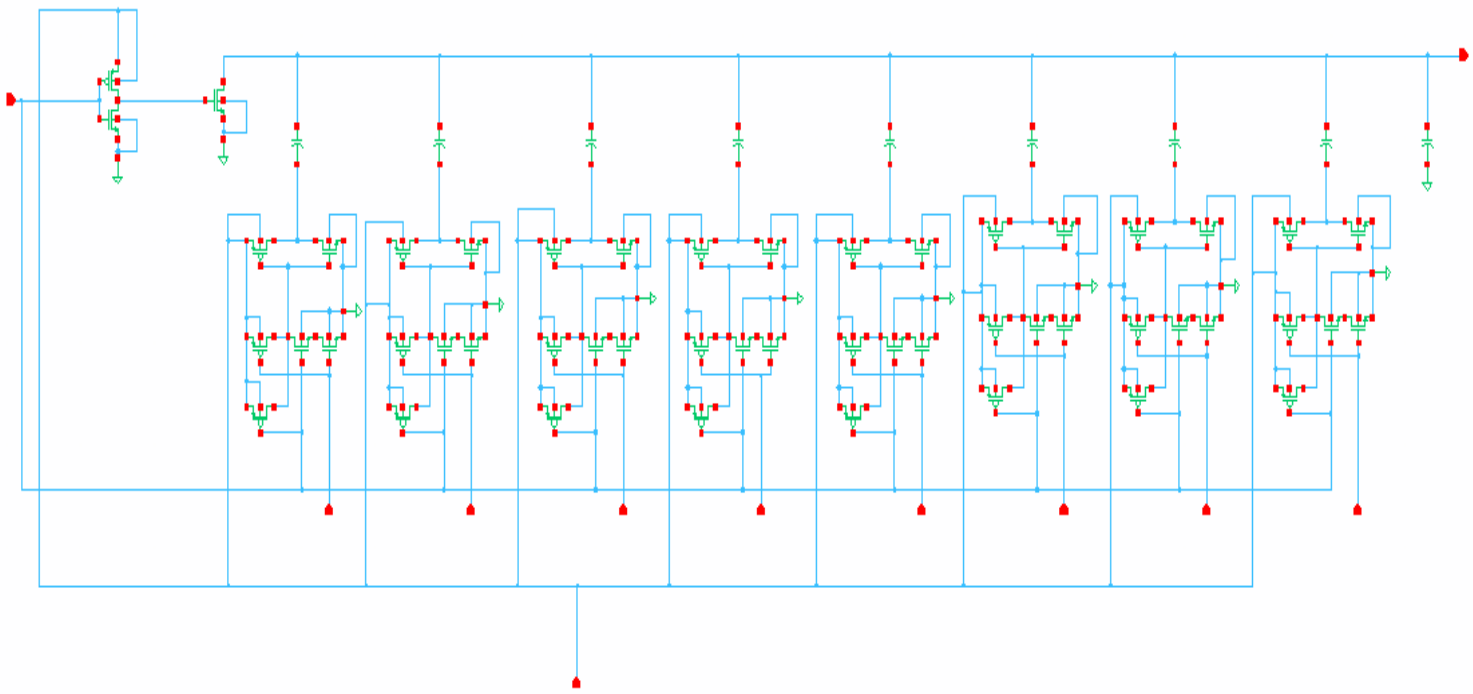


Figure 3.5: Charge Scaling Digital to Analog Converter

Fig. 3.5 shows the general implementation of a charge scaling DAC. A two-phase, non-overlapping clock is used for this converter [22]. During *CLK1* the top and bottom plates of all capacitors are grounded. During *CLK2*, capacitors are associated with the bits that are '1' are connected to V_{REF} and the bits with '0' are connected to ground (*GND*). The output from the DAC is obtained during *CLK2*. The basic charge scaling DAC has an op-amp serving as a buffer at the output. But the output of the DAC is connected to the input of a comparator, which is a high impedance node. Therefore, the op-amp can be eliminated and then the circuit runs much faster. Thus, the speed of the DAC is only dependent on the delay in the switches of the DAC and hence it settles quickly.

The DAC conversion is explained in following steps:

1. First, during *CLK1*, the capacitor array is completely discharged to the ground. This step provides the offset cancellation.

2. Conversion process occurs during the *CLK2* phase. First, the MSB capacitor is switched to V_{REF}. Due to the binary-weighting of the array the MSB capacitor forms a 1:1 divided between the MSB capacitor and the rest of the capacitor array. Thus, the output voltage of DAC is now $V_{REF}/2$. Subsequently, if V_{in} is greater than $V_{REF}/2$ then the comparator outputs a digital '1' as the MSB, otherwise comparator output is a digital '0' as the MSB. Each capacitor is tested in the same manner until the comparator input voltage converges to the offset voltage, or at least as close as possible given the resolution of the DAC.

The output voltage of the DAC is given as:

$$V_{out} = V_{REF}[b_0 2^{-1} + b_1 2^{-2} + ... + b_{N-1} 2^{-N}] \text{ ---------- } (3.1)$$

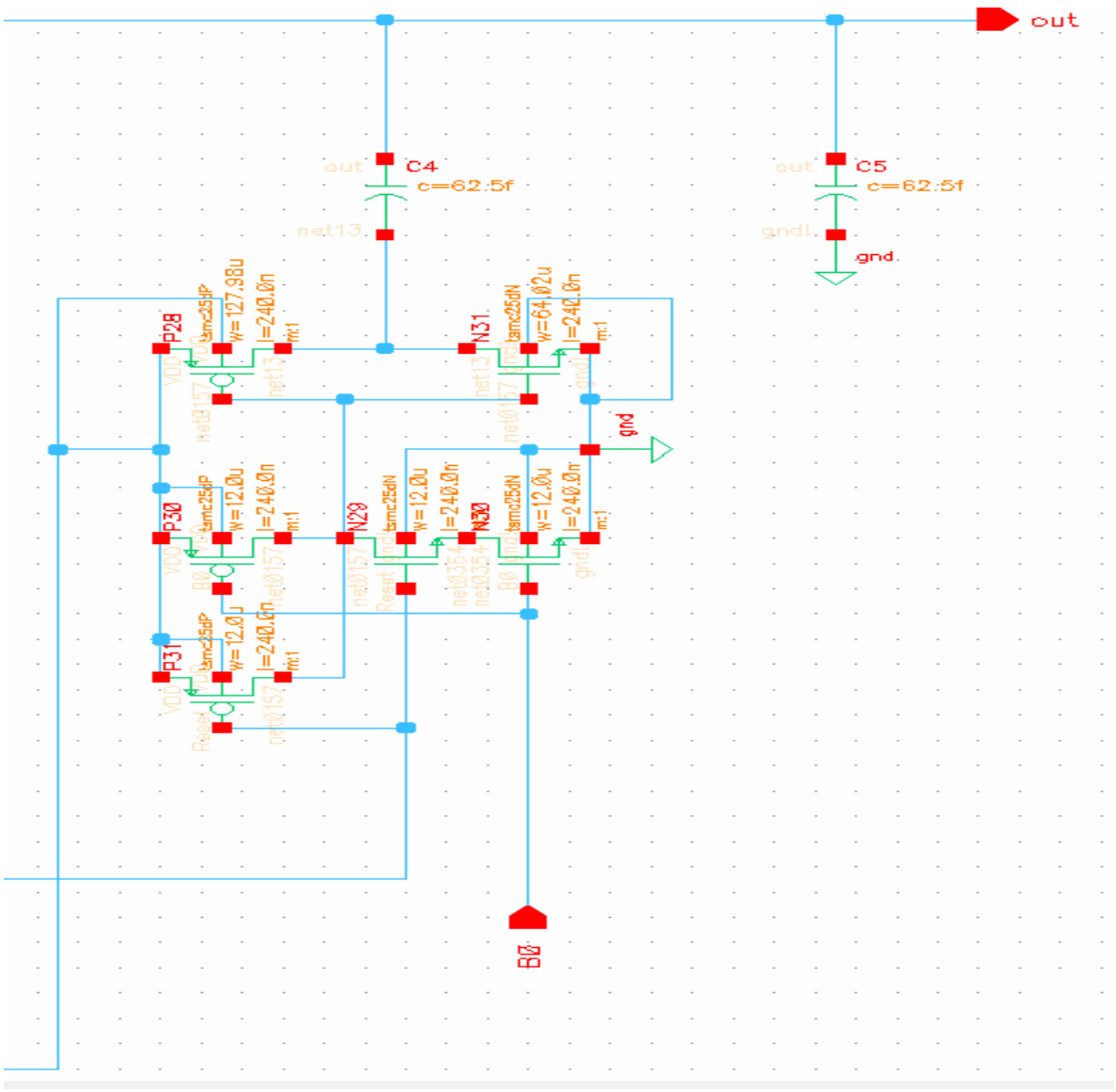


Figure 3.6: DAC LSB Switch.

The charge scaling DAC comprises of capacitors and switches. Fig. 3.6 shows the single unit of charge scaling DAC. This single unit is for the LSB. As it is mentioned earlier, the charge scaling DAC consists of an array of individually switched binary weighted capacitors. The LSB capacitor used in DAC has a value of 62.5fF and the rest capacitors are doubled from each other with MSB capacitor value of 32pF.

3.2.3 Sample and Hold Circuit

An important analog building block in designing data-converters is a Sample-Hold circuit. The main requirement in designing sample-hold circuit is the speed. The sample-hold circuit should operate reliably even at higher frequencies as the input is sampled and the same is used as the reference for the rest of conversion period. The “hold” step should be of minimum period.

When the stop signal is enabled the sample is acquired. In this step, the conversion stops and digital outputs are memorized. No conversion process takes place during this step and this period can be utilized to acquire the new sample. The sample and hold circuit is in hold mode throughout the conversion process.

The sample and hold circuit considered for the ADC design is based on the circuit proposed in [23] is shown in fig. 3.7. The other important problems faced in designing sample and hold circuits are clock feed through and charge injection. These problems are being minimized in this proposed circuit.

The sample of the input is taken during CLK1 and the input voltage is kept at hold for the conversion process during CLK2. During sampling, all switches are on except Q2. This connects C1 and C2 together and charges them to the input voltage. During this period, the op-amp is being reset and the positive terminal of the op-amp is charged to 0 V. Q4 and Q5 are turned off, and shortly thereafter Q1 and Q3 are turned off. Finally Q2 is turned on. In this period, sample and hold circuit is in hold mode. The sample and hold circuit in hold mode is shown in fig. 3.8. The unity-gain feedback holds the voltage level for the whole period (i.e. during hold mode) and also the output impedance of sample and hold circuit is low [23].

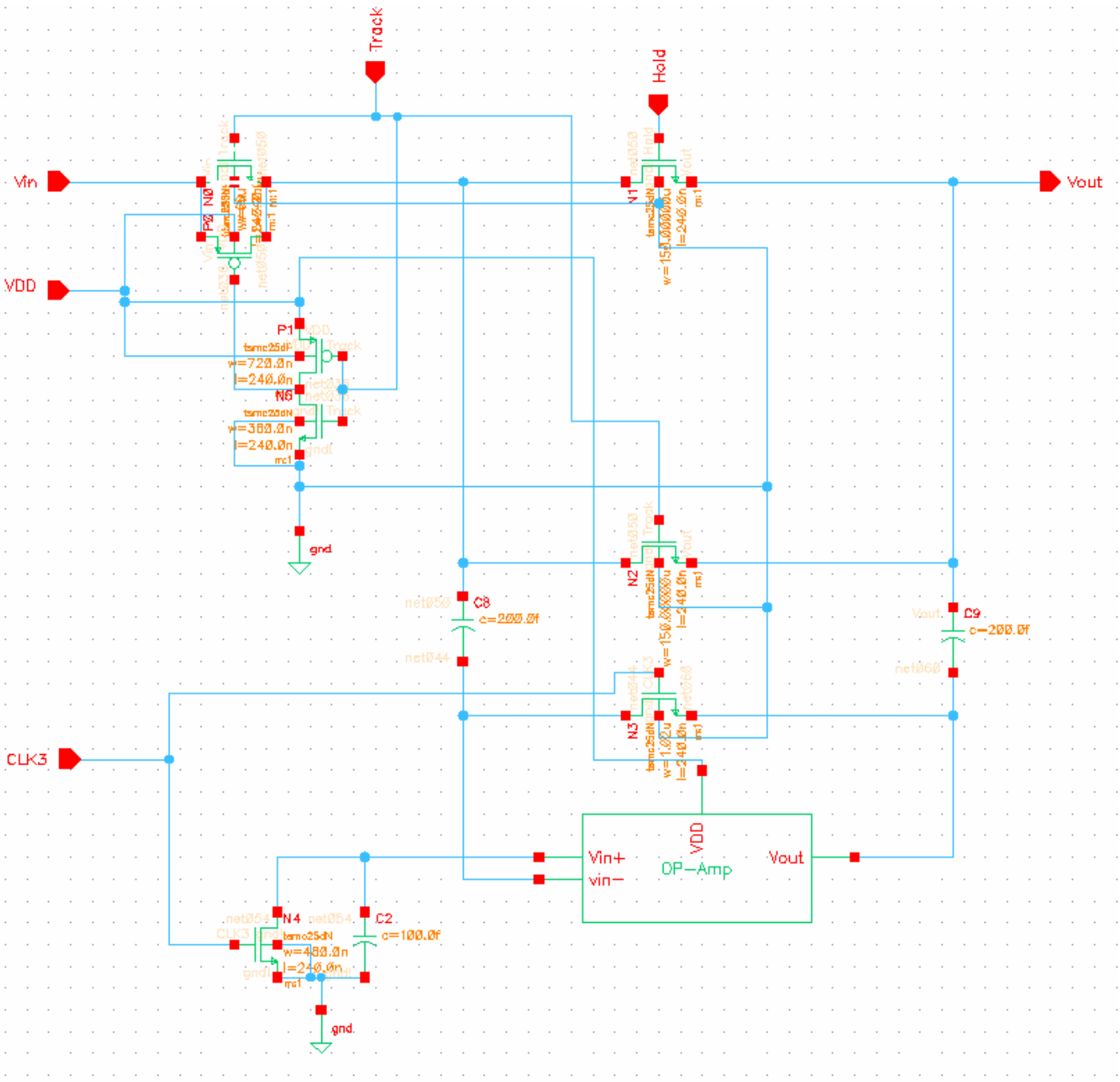


Figure 3.7: Recycling Sample and Hold

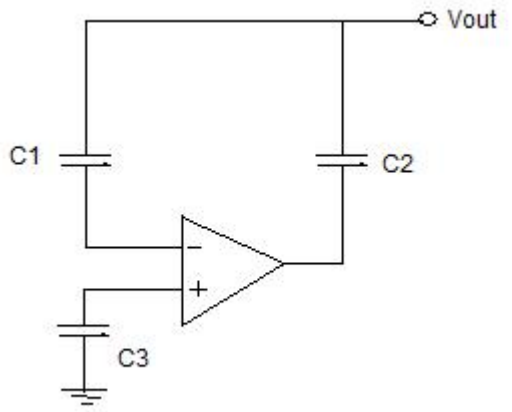


Figure 3.8: Sample and Hold Circuit in Hold Mode

In the sample and hold circuit, Q4 and Q5 are turned off slightly before Q1 and Q3, their clock feed through is not only signal independent but largely cancels due to the common-mode rejection of the input stage of the amplifier. The charge injection of Q1 and Q2 doesn't affect the output voltage. The charge injection of Q3 is signal dependent and does affect the output voltage, but its effect is minimized by the loop gain [23].

3.2.4 Comparator

In any ADC, comparators are the most critical components because their input offset voltage, delay and input range directly influence the resolution and speed of the ADC. The noise generated within a comparator plays an important role in overall performance at higher frequencies.

Fig. 5.5 shows the proposed comparator. The comparator consists of a CMOS latch circuit and an S-R latch circuit. The CMOS latch circuit includes the biasing part, differential and regeneration circuit. The PMOS differential pairs are responsible for the amplification in circuit.

Comparator Optimization

1. Transistor M1-M3: Consider the PMOS differential pair (M1 -M3). From [24] the difference of currents between differential and regeneration stage will be

$$\Delta I = I_{D2} = I_{D3} = \frac{k}{2}\frac{W}{L}\Delta V\sqrt{\frac{4I_D}{K(W/L)} - \Delta V^2} \text{ ----------(3.2)}$$

   From the equation 3.2, the size of the PMOS transistors have significant effect on the comparator performance. Increasing the W/L ratios of PMOS transistors of differential pair (M1-M3) will produce ΔI [25]. This saturates either M8 or M9 for a smaller difference between Vin and Vref. This way the offset error can be reduced. However if W/L ratios of the transistors are too large, this will create too large current of ID2 and ID3. This excess current will disable the S-R latch before the regeneration happens.

2. Transistor M4 and M5: PMOS transistors M4 and M5 are controlled by CLK. Since the design uses no pre-amplifier these transistors help to minimize the kickback effect by separating the inputs from outputs during the regeneration process.

3. Transistor M6 and M7: NMOS transistors M6 and M7 act as switching transistors. The switching time of these transistors is given by [25]

$$T_t = \frac{1}{f_t} = 2\pi\frac{V_t WLC_{js}}{I_D} \text{ ----------(3.3)}$$

   From the equation 3.3, by decreasing the widths and lengths of switching transistors, the switching time will increase with a performance improvement in the regeneration process.

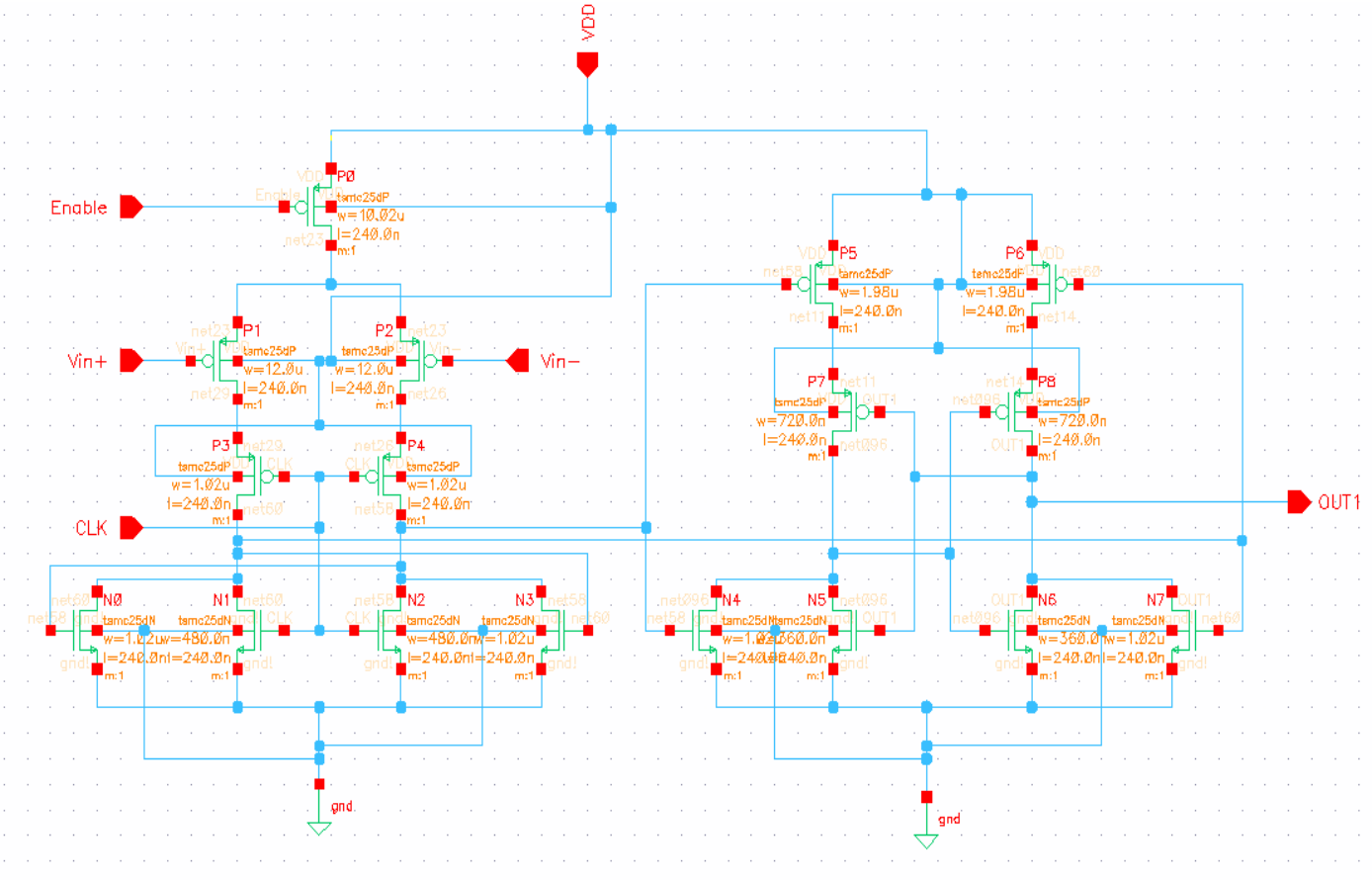


Figure 3.9: Latched Comparator

4. Transistor M6 and M7: NMOS transistors M6 and M7 act as switching transistors. The switching time of these transistors is given by [25]

$$T_t = \frac{1}{f_t} = 2\pi \frac{V_t WLC_{js}}{I_D} \text{ - - - - - - - - - - - - - - - (3.3)}$$

From the equation 3.3, by decreasing the widths and lengths of switching transistors, the switching time will increase with a performance improvement in the regeneration process.

5. Transistor M8 and M9: NMOS transistors M8 and M9 implement a regeneration circuit. Drain current of these transistors affect the regeneration process. By increasing the W/L

ratios of NMOS transistors will produce larger drain currents and thus producing the quicker regeneration process. However, too large drain current will discharge the two branches too quickly, which will cause the increase of offset voltage to maintain a proper regeneration process.

Comparator Operation

The comparator operates in two phases (clock high and low), amplification phase and regeneration phase during the comparison cycle. When the clock is low, the amplification phase occurs. During this amplification phase the PMOS cascade pair M4 and M5 turn on while the switching NMOS transistors M6 and M7 are turned off and inputs are amplified and sampled at differential nodes.

When the clock is high, the NMOS switching transistors M6 and M7 turn on and regeneration occurs. Now, the differential nodes are discharged to ground.

3.2.5 SAR ADC Operation

The components that are required to design ADC are explained in previous sections.

The description of the converter is as follows: The conversion cycle starts with enabling the "start" signal in SAR control. During this period, the initial pattern of 1000 0000 is set in SAR. This pattern is given to the DAC, which generates an analog equivalent for this pattern. This analog voltage value is compared with the sample and hold output. Based on the comparator output, either the MSB bit is set to zero or remained at same level. Here the MSB is accomplished and a similar process is continued for rest of the bits. Including the first step on in which initial pattern is generated; 8 bit converter takes 10 steps to convert. On the tenth step, the decision for all 8 bits is completed and the digital output is ready. This is accomplished by a "stop" signal, which locks the bits of the SAR on tenth

step. During the stop period or on the last step of every conversion, the analog input is sampled and used as the reference for the next conversion cycle. The operation of a 5-bit SAR ADC is shown in fig. 3.10.

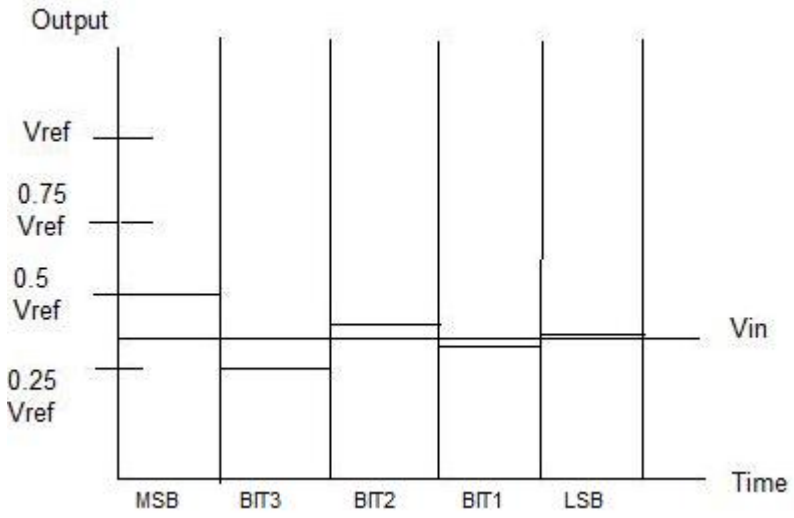


Figure 3.10: Operation of 5-bit SAR ADC

Chapter 4: Results

In this chapter, the simulation results obtained during the design of the Successive Approximation Analog to Digital Converter are presented. The overall simulation waveforms of the ADC are shown in this chapter.

4.1 Experimental Setup

Successive Approximation ADC is designed at transistor level. The transistor level implementation and simulations has been accomplished using Virtuoso Cadence ICFB design environment. Cadence offers an integrated Electronic Design Automation (EDA) solution, which encompasses the entire design flow from behavioral modeling to post-layout simulation. The simulations are done in Analog Design Environment (ADE) and are carried out using Spectre simulator provided by the tool. The transistor level schematics are implemented in schematic editor. TSMC 0.25µm technology is used for the design.

The implementation of each component is described as follows: each component is implemented at transistor level in the schematic editor and a symbol is created. The symbol is instantiated in a test bench, which provides the stimulus to the component. The component is simulated using ADE through the test bench. The results are viewed in the Waveform Editor and when required, the results are exported to a text file.

4.2 Successive Approximation ADC Functionality Verification

In the previous chapter, the components required to build ADC are discussed. In this section, the ADC has to be checked for the correctness and its performance characteristics such as power consumption and SFDR must be determined at different temperatures and different voltages. An Analog-to-Digital converter generates the digital code corresponding to the analog input provided to it.

In this implementation, the reference voltage provided is 0.8 V. The analog input voltage ranges from 0 V -0.5 V. As the implemented ADC is of 8 bits, all the analog input sample voltages are represented by 256 distinct digital codes. This implied the voltages of all the samples ranging from 0 V - 0.5 V can be represented in 256 distinct codes.

The LSB value can be calculated as:

$$1LSB = \frac{V_{REF}}{2^N} \text{---------}(4.1)$$

$$1LSB = \frac{0.8}{2^8} = \frac{0.8}{256} \text{-----}(4.2)$$

The important feature of Successive Approximation ADC is the feedback mechanism in its structure. During each step of a conversion cycle, the SAR must guess a digital code, which brings the output of DAC closer to the sampled input. This implies, during every conversion the output of DAC indicates the correctness of ADC. ADC converts convert analog signal into finite number of digital codes. This introduces a quantization error, which limits the maximum Signal-to-Noise ration that can be achieved for a given resolution. The Signal-to-Noise ratio for N-bit ADC is given by:

$$SNR_{\max} = 6.02NdB + 1.76dB \text{-----}(4.3)$$

The ADC implemented here has 8 bits. Hence, the maximum value of Signal-to-Noise ratio is:

$$SNR_{\max} = 6.02 * 8dB + 1.76dB = 49.92dB \text{-----}(4.4)$$

To verify the ADC performance, initially a DC input was applied then a ramp signal and then a sinusoidal waveform were applied as input signal. This yields to digital codes that correspond to the captured sample. The digital codes were converted back to their analog equivalent and the value is compared with the analog voltage at the beginning of conversion.

Considering all the above concepts, the following simulations are carried out on the ADC to test its performance:

Initially DC inputs of 0.25 V, 0.4 V and 0.8 V are applied separately and their simulated results are analyzed. The inputs yields digital codes “01001111”, “10000000” and “11111111” respectively. This validates the behavior of ADC.

Next, a ramp signal of 500 Hz and with 0 V -0.5 V peak-to-peak voltages is applied. The simulated results are observed.

The dynamic performance of the ADC is mainly characterized by SFDR. The method of calculating SFDR involves the application of the input analog sinusoidal signal and the digital codes are collected. These samples are converted into frequency domain using Fast Fourier Transform (FFT). SFDR is described as the difference between the fundamental signal strength and the largest spurious signal strength. The built in function “dft” in Virtuoso Cadence calculator was used to implement FFT. SFDR can be calculated by visually observing FFT.

4.2.1 ADC Performance with DC Input Signal

This is the basic method to test the ADC. Three DC voltages are applied to test the performance of the ADC. DC voltages of 0.25 V, 0.4 V and 0.8 V are applied and tested the digital output codes whether the correct corresponding digital value is attained by the ADC.

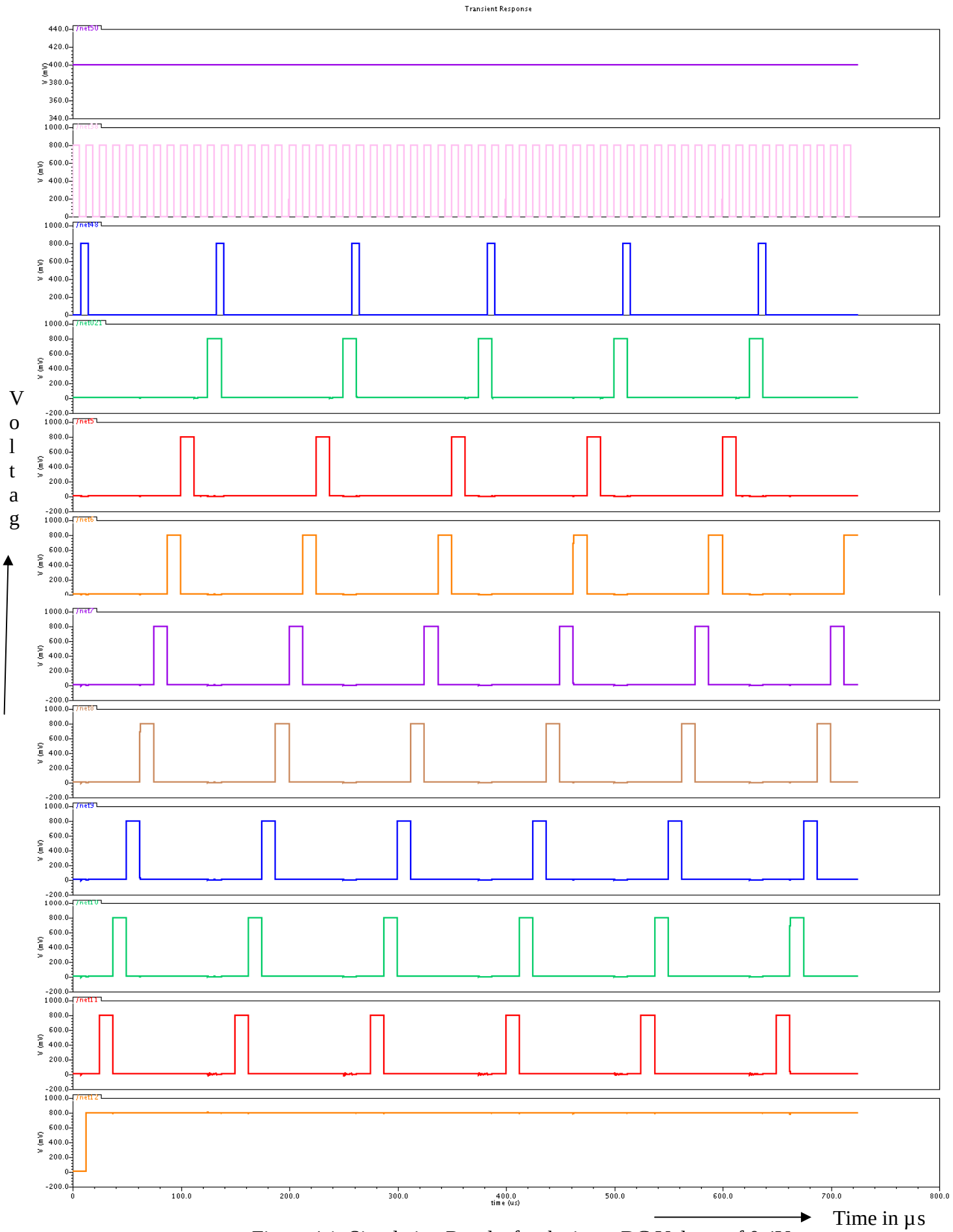


Figure 4.1: Simulation Results for the input DC Voltage of 0.4V

As seen in the FIGURE 4.1, when a DC voltage of 0.4 V is applied, the digital output codes are read as “1000 0000”. Since, the reference voltage is 0.8 V in this design, the DC voltage of 0.4 V is exactly half the reference voltage and the output digital codes are correct. Similarly, the simulations are performed for the DC voltage of 0.25 V and 0.8 V.

4.2.2 ADC Performance with Ramp Input Signal

In this section, the simulation waveforms obtained when ramp signal is applied as input signal is observed.

As seen in the FIGURE 4.2, a ramp signal of 500 Hz and 0.5V P-P is applied and the digital output codes are read and verified.

In the above two sections the functionality of ADC is being tested and verified using DC input signal and ramp input signal. Their digital output codes are read and compared with the input signal.

4.2.3 ADC performance with Sinusoidal Input Signal

In this section, the behavior of ADC is discussed when a sinusoidal signal of 500 HZ and 0.5V P-P is applied. The simulation waveforms for the applied sinusoidal signal at supply voltages 0.8V, 0.9V, 1.0V and each at 0 ◦C, 27 ◦C, 65 ◦C temperatures is observed. The power consumption and SFDR is calculated for each power supply and at each temperature. The maximum frequency that can be processed by the converter is 4 KHz due to the Nyquist Criterion as it samples at 8 KSPS but as per requirement the input analog signal frequency considered as 500 Hz.

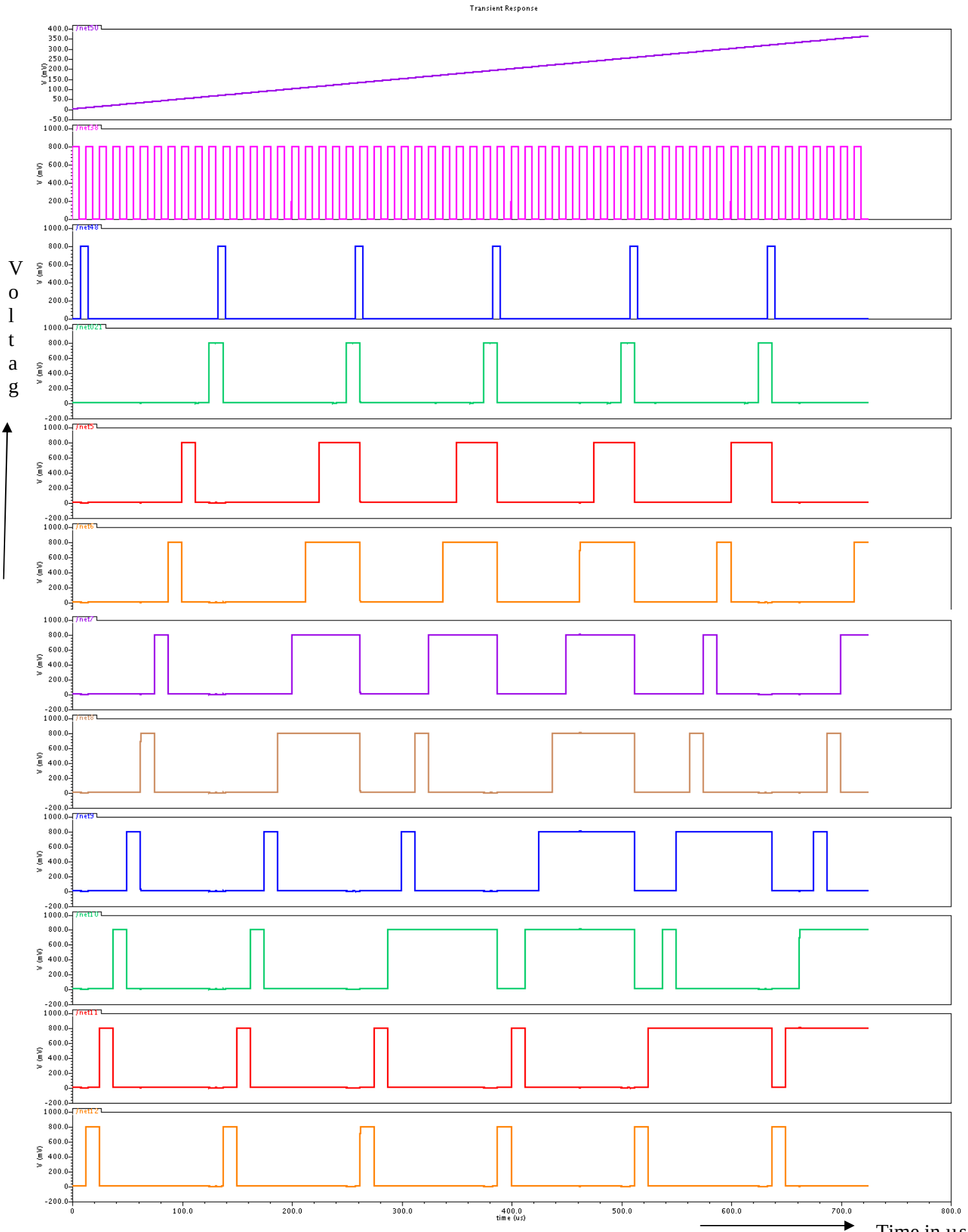


Figure 4.2: Simulation Results for the input Ramp Signal of 500 Hz of 0.5V P-P

As seen in the FIGURE 4.3, a sinusoidal signal of 500 Hz and 0.5V P-P with supply voltage of 0.8 V is applied and the respective digital output codes are observed. Stop signal is high when the analog input signal is converted and the digital bits are obtained during this period. Stop signal indicates the end of conversion. The FIGURE 4.3 shows the simulation results performed at 27 ºC.

The simulations are even done at 0 ◦C and 65 ◦C and the power consumption and SFDR.

Similarly, the simulations are done using the same input sine wave with supply voltages 0.9 V and 1.0 V. The simulation results for the supply voltages at 0.9 V and 1.0 V and at 27 ºC temperature is shown in Figure 4.4 and 4.5 respectively.

Table 4.1: Digital Bits with 0.8V as supply voltage at 27 ◦C

Time (μs)	Digital Bits
15	01010011
140	01110001
265	10001001
390	10011100
515	10011111
640	10011000
765	10000110
890	01101011
1015	01001100
1140	00110000
1265	00001111

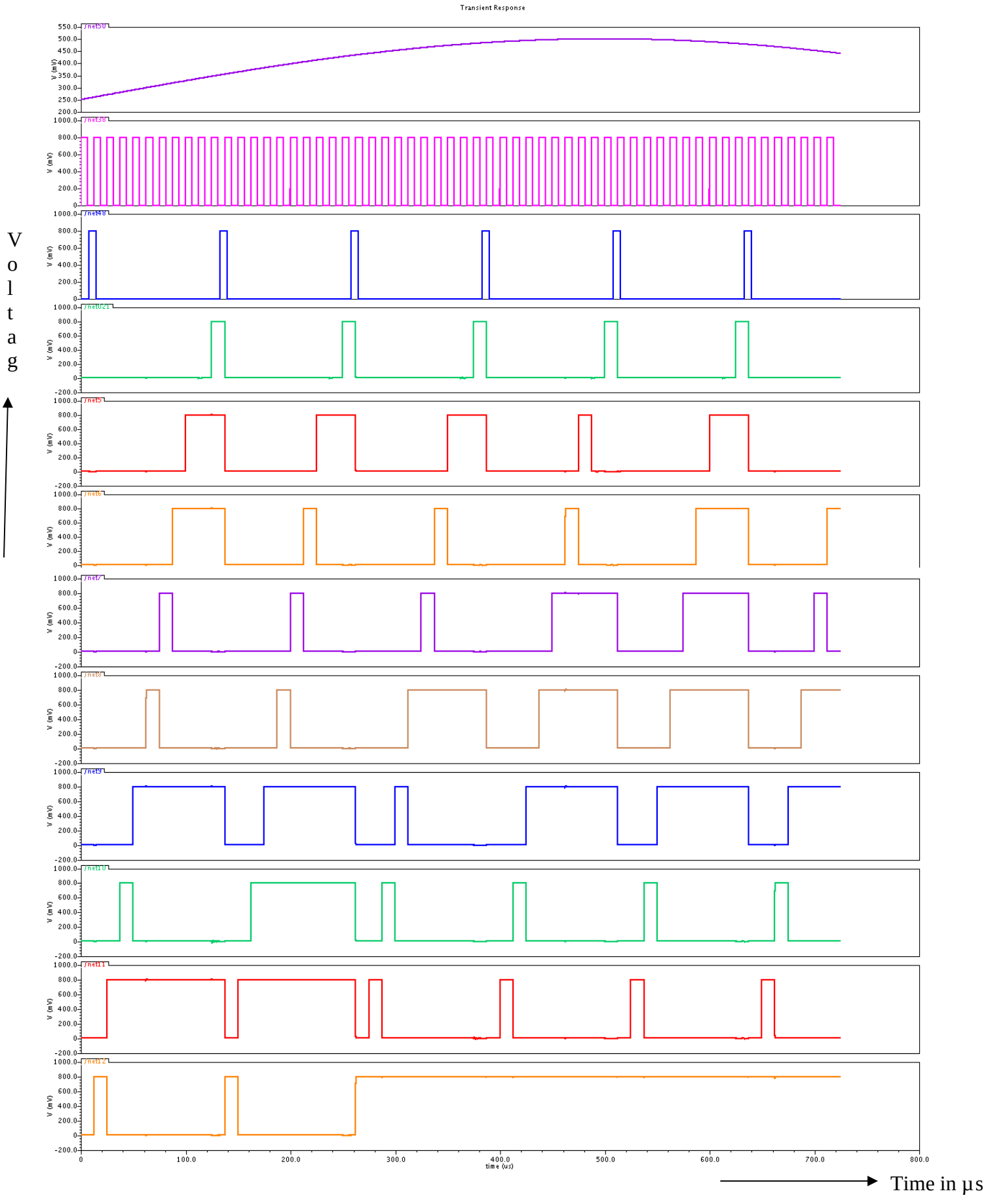


Figure 4.3: Simulation Results for Sinusoidal Signal with Supply Voltage 0.8V

4.2.4 Calculation of Power Consumption and SFDR

In this section, the calculations for power consumption and SFDR at different supply voltages and at different temperatures are shown.

The circuit has three different power supplies: first is for sample and hold circuit, second is for successive approximation register (digital block) and the final one for DAC and comparator.

The power consumption is calculated by multiplying supply voltage with the current drawn from voltage source to ground. Since, the circuit has three supplies; the total power consumption is obtained by simply adding the three power consumption components.

$$P = V * I \text{ ----------} (4.5)$$

$$P = P1 + P2 + P3 \text{ -------} (4.6)$$

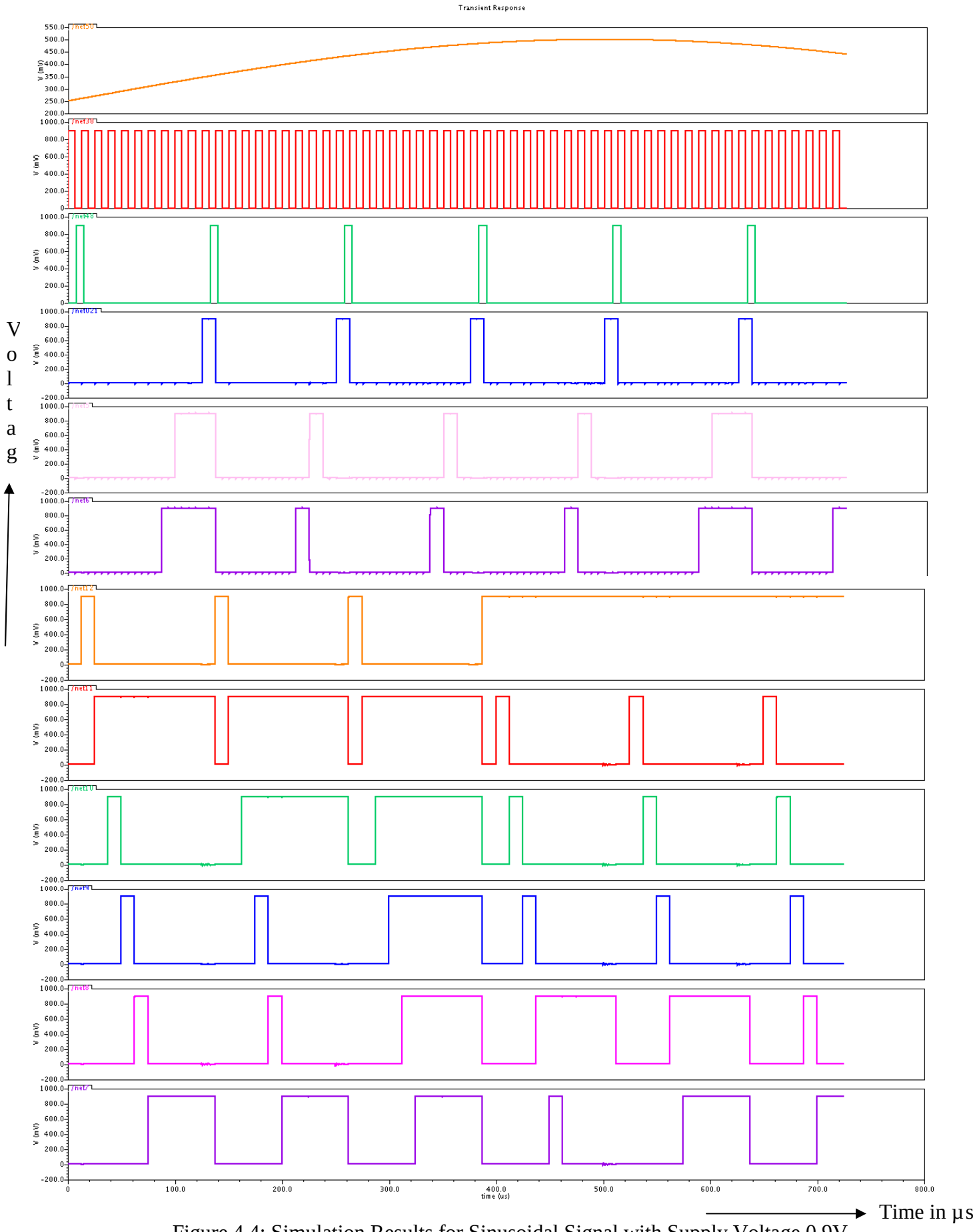


Figure 4.4: Simulation Results for Sinusoidal Signal with Supply Voltage 0.9V

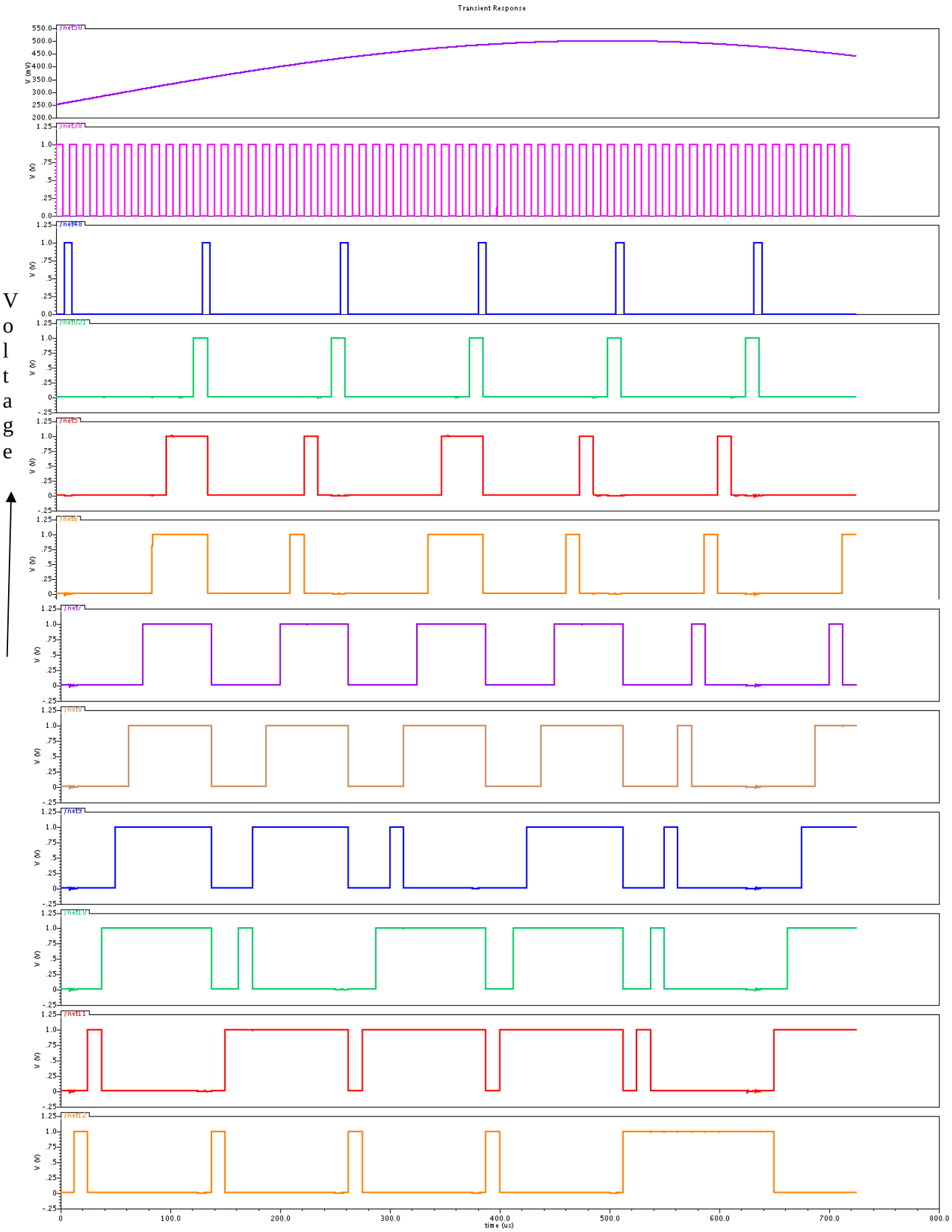


Figure 4.5: Simulation Results for Sinusoidal Signal with Supply Voltage 1.0V

Using the above equations and the calculator from Cadence ICFB, the power consumption for the ADC at three different voltages (0.8V, 0.9V, 1.0V) at 0 ◦C, 27 ◦C and 65 ◦C each are calculated.

Table 4.2: Power Consumption for Supply Voltages 0.8 V, 0.9 V and 1.0 V

P_{cons}	0.8V			0.9V			1.0V		
	0 ºC	27 ºC	65 ºC	0 ºC	27 ºC	65 ºC	0 ºC	27 ºC	65 ºC
P_{vdd} (µW)	0.442	0.610	0.807	1.307	1.666	2.206	3.492	4.165	5.065
P_{vdda} (µW)	1.948	1.870	1.796	4.763	4.469	4.165	10.329	9.485	8.537
P_{vddd} (µW)	0.079	0.083	0.095	0.103	0.107	0.120	0.127	0.133	0.151
P_{total} (µW)	2.471	2.564	2.788	6.175	6.244	6.493	13.949	13.784	13.754

Where,

P_{vdd} represents power consumed by Sample and Hold Circuit,

P_{vdda} represents power consumed by DAC and Comparator,

P_{vddd} represents power consumed by SAR (digital block) and

P_{total} represents the total power consumed by the ADC.

The above table represents power consumption of individual voltage supply and the total power consumption for supply voltage of 0.8V at 0 ˚C, 27 ˚C and 65 ˚C temperatures.

Similarly, the total power consumption is calculated for 0.9V supply voltage as 6.1751µW, 6.2435µW and 6.4927µW at 0 ˚C, 27 ˚C and 65 ˚C temperatures respectively and for 1.0V supply voltage as 13.9491µW, 13.7843µW and 13.7544µW at 0˚C, 27 ˚C and 65 ˚C temperatures respectively.

From the above table, the total power consumption increases with the temperature. Leakages in the circuit increase with the increase in temperature, which results in the increase in power consumption.

$$P_{total} = P_{dynamic} + P_{short-circuit} + P_{Leak} \text{ ---------- } (4.7)$$

From the above equation, P_{total} represents the total power consumption of a CMOS circuit. P_{total} can be expressed as the sum of three components, $P_{dynamic}$, $P_{short\text{-}circuit}$ and P_{Leak}, which represents dynamic power component, short-circuit power component and leakage power component. As the temperature increases, leakage power component becomes major component in the total power consumption [1].

Spurious Free Dynamic Range (SFDR): SFDR is defined as the difference between the value of the desired output signal and the value of the highest amplitude output frequency that is not present in the input. SFDR is expressed in dB below the fundamental.

For calculating SFDR, FFT is applied to the output digital bits. SFDR can be visually calculated from the FFT.

From the fig. 4.6 SFDR is calculated as 40.56 dB and fig. 4.7 and fig. 4.8 shows the FFT signals for ADC running at 0 ◦C and 65 ◦C respectively.

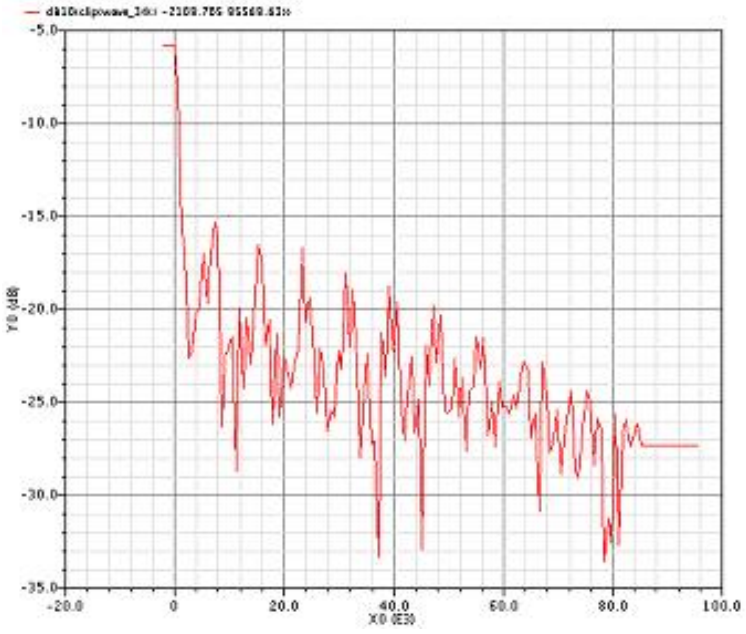


Figure 4.6: FFT for ADC operating at 27 ºC with 0.8 V Supply Voltage

SFDR is calculated at 0 ◦C and 65 ◦C for supply voltage 0.8V are obtained as 40.56 dB and 40.92 dB respectively.

4.2.5 Impact of Noise in V_{in} and V_{ref}

The noise in ADC includes quantization noise and the noise generated by the circuit. Assuming that the circuit is considered in isolation, the noise in the circuit has to be considered. The noise in the circuit consists of noise from the input V_{in} and reference voltage.

In this section the amount of noise from the V_{in} and reference voltage that can be tolerated by the circuit is analyzed. Let us assume that the sample and hold has a noisy input signal. The sample and hold tries to track this noisy signal and has the noisy signal for the conversion during hold mode. Now let us consider the *Vref* signal, an input to the Digital-to-Analog converter, also contains noise. In every step the DAC generates a fraction part of *Vref* depending on the state of switches. The noisy signals from sample and hold and DAC are the inputs to the comparator. The comparator generates a logic high or a logic low voltage depending upon whether the voltage at its V_{in}+ terminal is greater than that of the V_{in}- terminal or not. To do so, it must be able to resolve amplitudes with a difference of LSB/2 at its terminals.

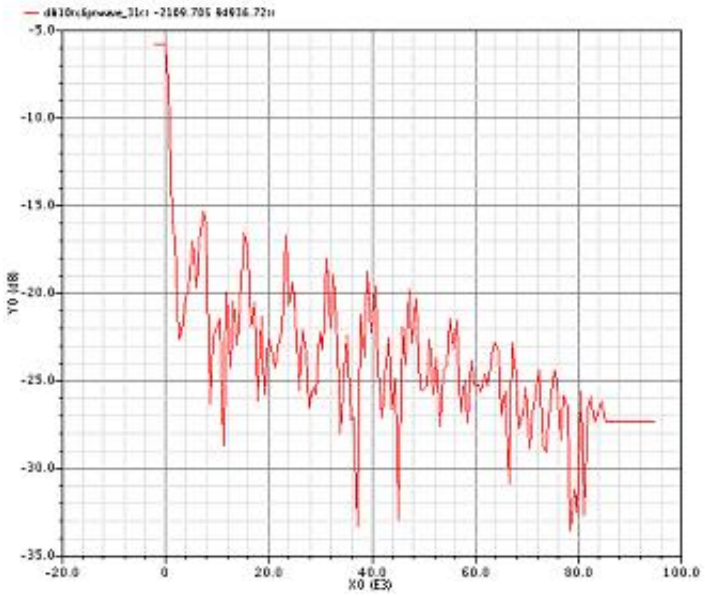


Figure 4.7: FFT for ADC operating at 0 ºC with 0.8 V Supply Voltage

From the above discussion, that as long as the noise at the inputs is of a magnitude that the comparator can still make a correct decision, it is acceptable. The noise can result in a wrong decision by the comparator but will not propagate to the output as noise again. For the same reason, this noise will also not affect the digital outputs generated by the Successive Approximation Register [27].

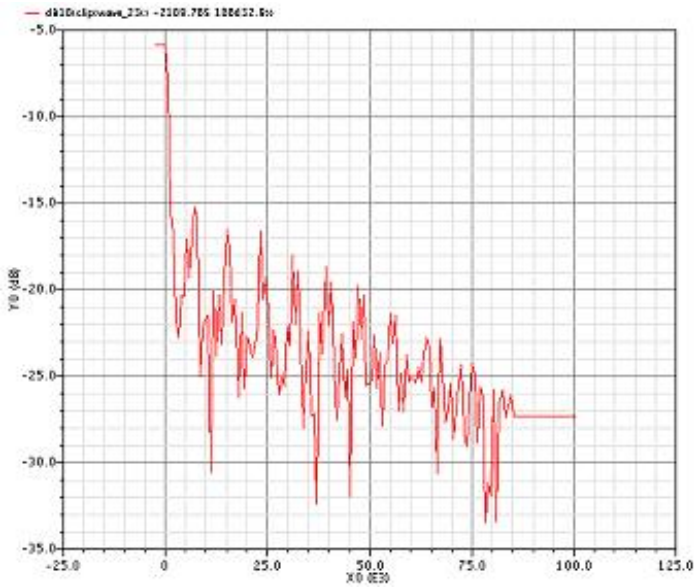


Figure 4.8: FFT for ADC operating at 65 ºC with 0.8 V Supply Voltage

Chapter 5: Conclusions and Future Work

5.1 Conclusions

The SAR ADC is implemented at the transistor level and its behavior is verified using simulations. The objective of implementing the ADC at low voltages and improving the sampling frequency of the binary search based CMOS SAR ADC is achieved.

Table 5.1: Measured ADC Performance

Supply Voltage	0.8V
Technology	TSMC 0.25 µm CMOS
Resolution	8 Bits
Conversion Rate	8 KS/s
Power Consumption	2.5640 µW
Input Swing	0 – 0.5V
SFDR	40.56 dB
Temperature	27 ºC

The comparison to the previous work is shown in the following table.

Table 5.2: Comparison to the Previous Work

	Year	Resolution	Speed	Supply Voltage	Power Consumption
Moetezapour, S.	2000	8 Bit	50 KS/s	1V	0.34mW
Sheung Yan Ng	2005	5 Bit	-	3V	30mW
You-Kuang Chang	2007	8 Bit	500 KS/s	1V	7.75μW
SAR ADC	2009	8 Bit	8 KS/s	0.8V	2.56μW

5.2 Future Work

The performance of ADC is studied in this work at 0.8 V. The future work on this includes designing the ADC at the sub-threshold voltages and analyzing the challenges and its performance. The transistor level implementation can be laid out and fabricated to test its performance. This work was developed on 250nm transistor length technology. More extensive research work can be carried out to know the performance at 90nm, 65nm or 45nm transistor length technologies.

References

[1] Sung-Mo Kang and Yusuf Leblebici, “CMOS Integrated Circuits: Analysis and Design,” McGraw-Hill Third Edition.

[2] K. Bult, “Analog Design in Deep Sub-Micron CMOS,” Proceedings of the 26th European Solid-State Circuits Conference, Broadcom, Netherlands, 19-21 September 2000, pp. 126–132.

[3] G. Groenewold, “Optical Dynamic Range Integrators,” IEEE Trans. Circuits and Systems-I, vol. 39, pp. 614-627, Aug. 1992.

[4] A-J. Annema, “Analog Circuit Performance and Process Scaling,” IEEE Trans. Circuits and Systems-II, vol. 46, pp. 711-725, Jun. 1999.

[5] F. Maloberti, F. Francesconi, P. Malcovati, O. J. A. P. Nys, “Design Considerations on Low-Voltage Low-Power Data Converters,” IEEE Trans. Circuits and Systems-I, vol. 42, pp. 653-863, Nov. 1995.

[6] R. Castello, F. Montecchi, F. Rezzi, A. Baschirotto, “Low-Voltage Analog Filters,” IEEE Trans. Circuits and Systems-I, vol. 42, pp. 827-840, Nov. 1995.

[7] S. -W. Sin, S. -P. U, R. P. Martins, “Generalized Circuit Techniques for Low-Voltage High-Speed Reset-and Switched-Op-amps,” IEEE Trans. Circuits and Systems-I, vol. 55, pp. 2188-2201, Sept. 2008.

[8] H. -H. OU, S-J. Chang, B-D. Liu “Low-Power Circuit Techniques for Low-Voltage Pipelined ADCs Based on Switched-Opamp Architecture,” IEICE Trans. Fundamentals, vol. E91-A, pp. 461-468, Feb. 2008.

[9] E. A. Vittoz, “Low-Power Design: Ways to Approach the Limits,” International Solid-State Circuits Conference, pp. 14-18, Feb. 1994.

[10] M. E. Waltari, K. A. I. Halonen, “Circuit Techniques for Low Voltage and High Speed A/D Converters,” Kluwer Academic Publishers

[11] W. Kester, “Analog Devices. MT-021 ADC Architectures II: Successive Approximation ADCs” [Online] Available: http://www.analog.com/en/other/multi−chip/ad10200/products/tutorials/CU tutorials MT−021/resources/fca.html

[12] J. Sauerbrey, D. Schmitt-Landsiedel, and R. Thewes, “A 0.5-v 1-uW successive approximation ADC,” IEEE Journal of Solid-State Circuits, vol. 38, pp. 1261-1265, 2003.

[13] E. Culurciello, A. Andreou, “An 8-bit, 1mW successive approximation ADC in SOI CMOS,” Proceedings of the 2003 International Symposium on Circuits and Systems, vol. 1, pp. I301I304, 2003.

[14] S. Mortezapour, E. K. F. Lee, “A 1-V, 8-bit successive approximation ADC in standard CMOS process,” IEEE Journal of Solid-State Circuits, vol. 35, pp. 642-646, 2000.

[15] Sheung Yan Ng, Bahar Jalali, Pengbei Zhang, James Wilson, Mohammad Ismail, “A Low-Voltage CMOS 5-bit 600MHz 30mW SAR ADC for UWB wireless Receivers,” 48th Midwest Symposium on Circuits and Systems, 7-10 August 2005, pp. 187-190.

[16] Roubik Gregorian, “Introduction to CMOS Op-Amps and Comparators,” John Wiley & Sons, Inc.

[17] Cia Jun, Ran Feng, Xu Mei-hua, “IC Design of 2MS/s 10-bit SAR ADC with Low Power,” Proceedings of the 2007 International Symposium on High Density Packaging and Microsystem Integration (HDP ‘07), Shanghai, China, 26-28 June 2007, pp. 1–3.

[18] You-Kuang Chang, Chao-Shiun Wang, Chorng-Kuang Wang, “A 8-bit 500-KS/s Low power SAR ADC for Bio-Medical Applications” IEEE Asian Solid-State Circuits Conference, pp. 228-231, November 2007.

[19] R. J. Baker, “CMOS Circuit Design, Layout, and Simulation”, Wiley-IEEE, Revised Second Edition, 2008.

[20] “Understanding SAR ADCs”. Application Note 1080, Maxim Integrated Products, May 2001.

[21] A. Rossi, G. Fucili “Nonredundant successive approximation register for A/D converters,” Electronics Letters, vol. 32, pp. 1055-1057, June 1996.

[22] P. E. Allen, D. R. Holberg, “CMOS Analog Circuit Design,” Oxford University Press, Second Edition, 2002.

[23] D. A. Johns, K. Martin, “Analog Integrated Circuit Design,” John Wiley & Sons, Inc. 1997.

[24] H. P. Le, A. Zayegh, J. Singh, “A high-speed low-power CMOS comparator with 10-bit resolution,” Proceedings of Fourth International Conference on Modeling and Simulation Melbourne, Australia, pp. 138-142.

[25] H. P. Le, A. Zayegh, J. Singh, “Performance analysis of optimized CMOS comparator,” IEEE Electronic Letters, vol. 39, pp. 833-835, May 2003.

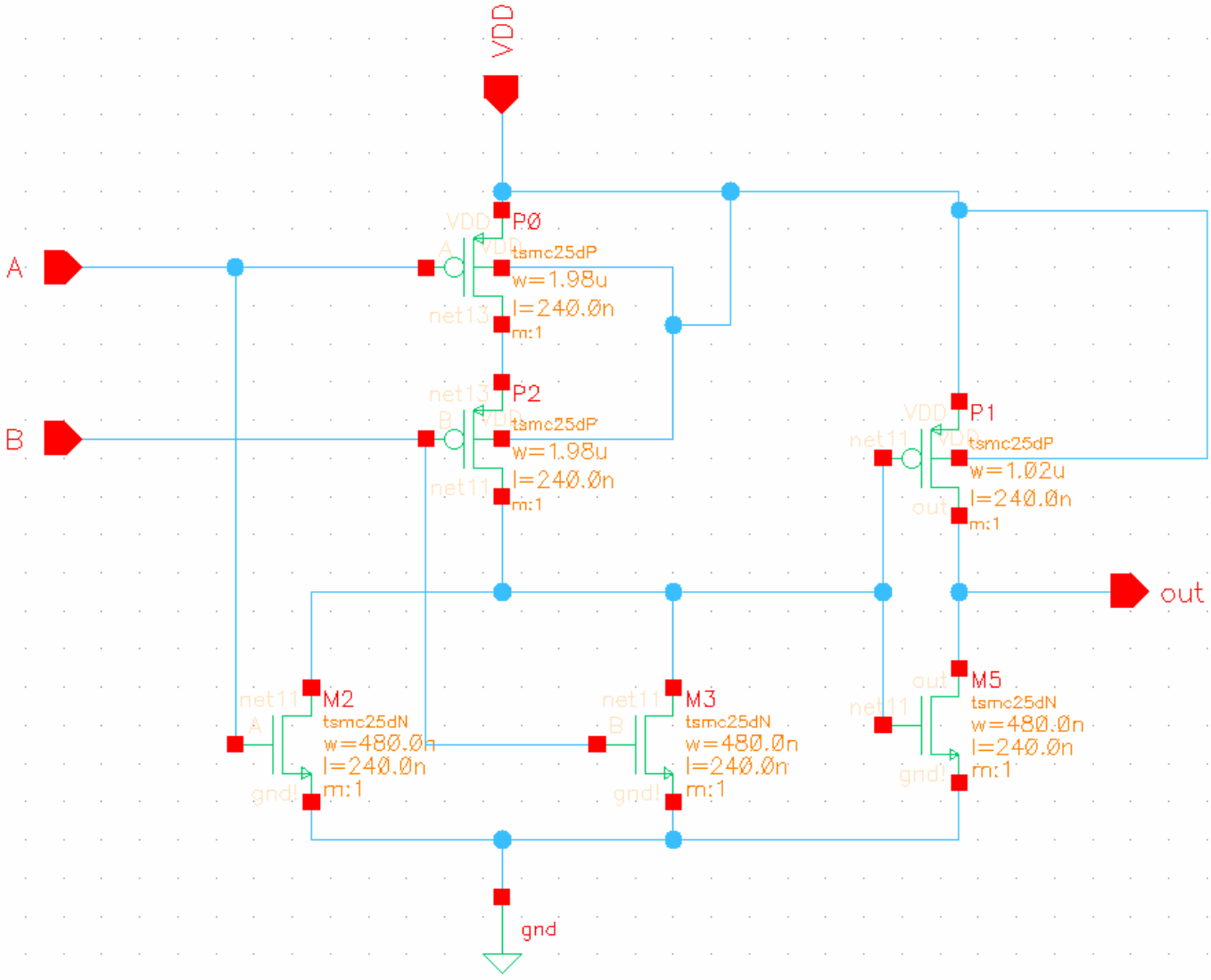
[26] P. Favrat, P. Deval, M. J. Declercq, “A High-Efficiency CMOS Voltage Doubler,” IEEE Journal of Solid-State Circuits, vol. 33, pp. 410-416, March. 1998.

[27] Vandana Desai, “Transistor-Level Simulation of a Novel CMOS Binary Search based Successive Approximation Analog-to-Digital Converter Circuit,” Thesis, University of Cincinnati, 2006

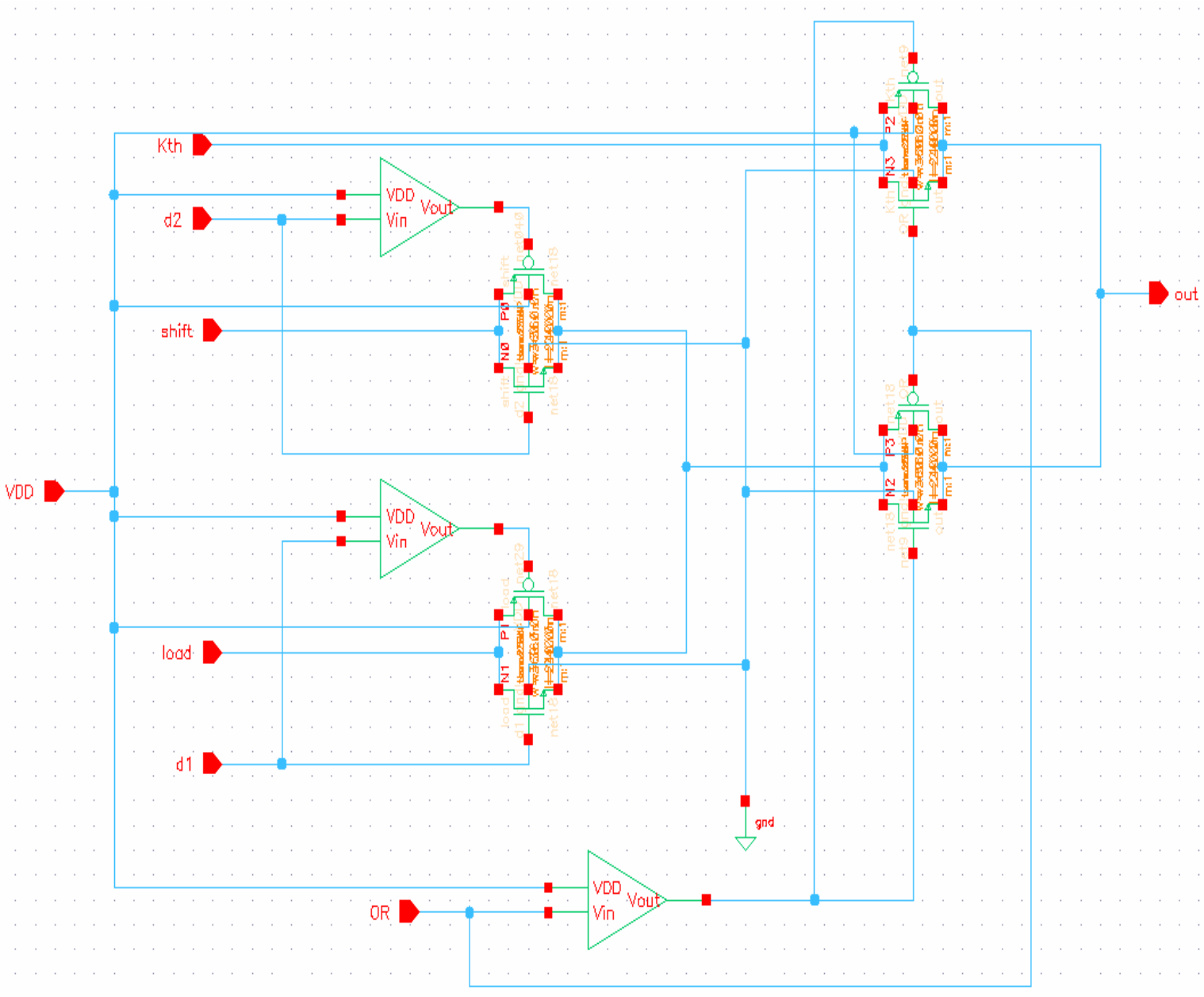
Appendix

Standard cells and gates designed in TSMC 0.25 µm CMOS technology

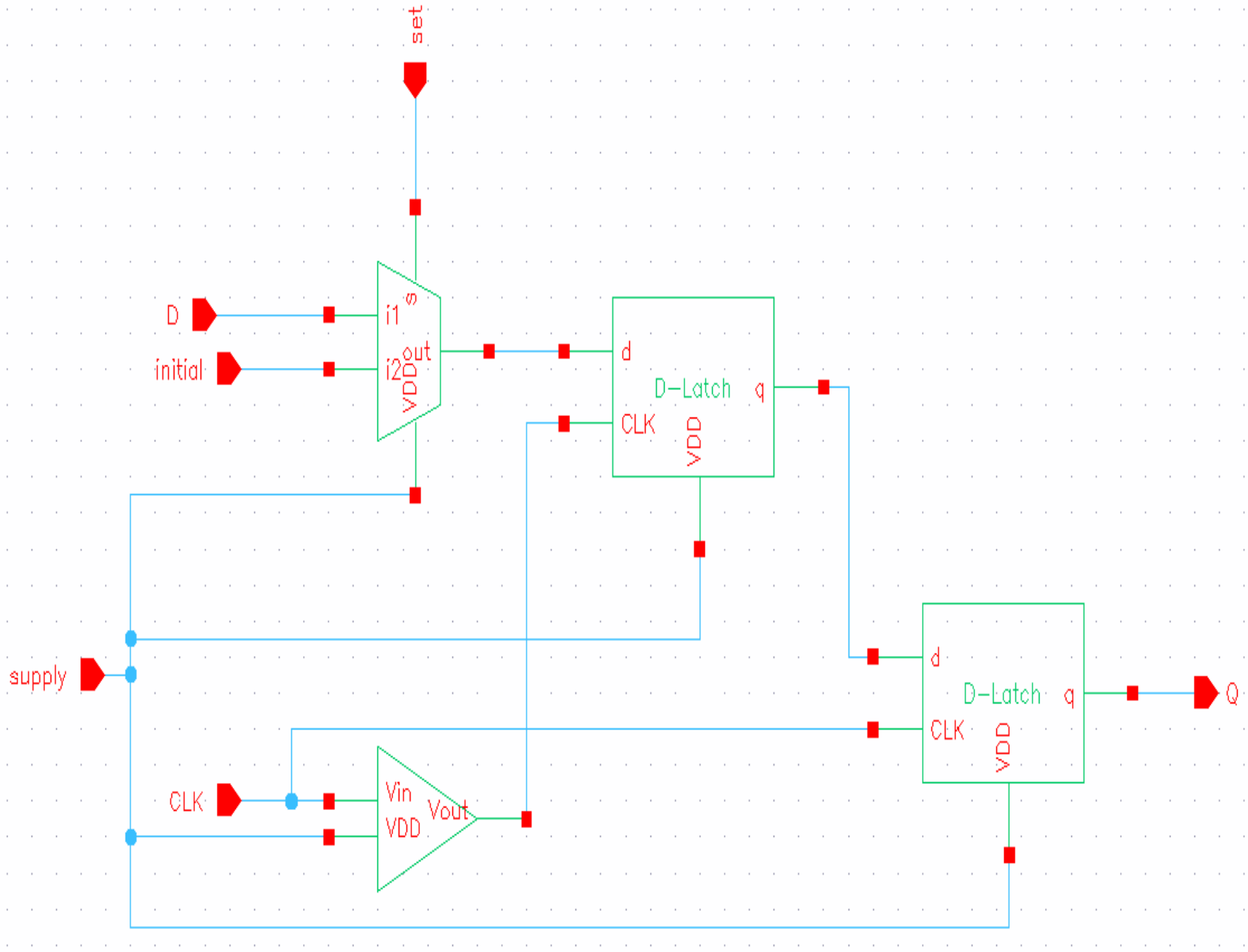
1. OR Gate



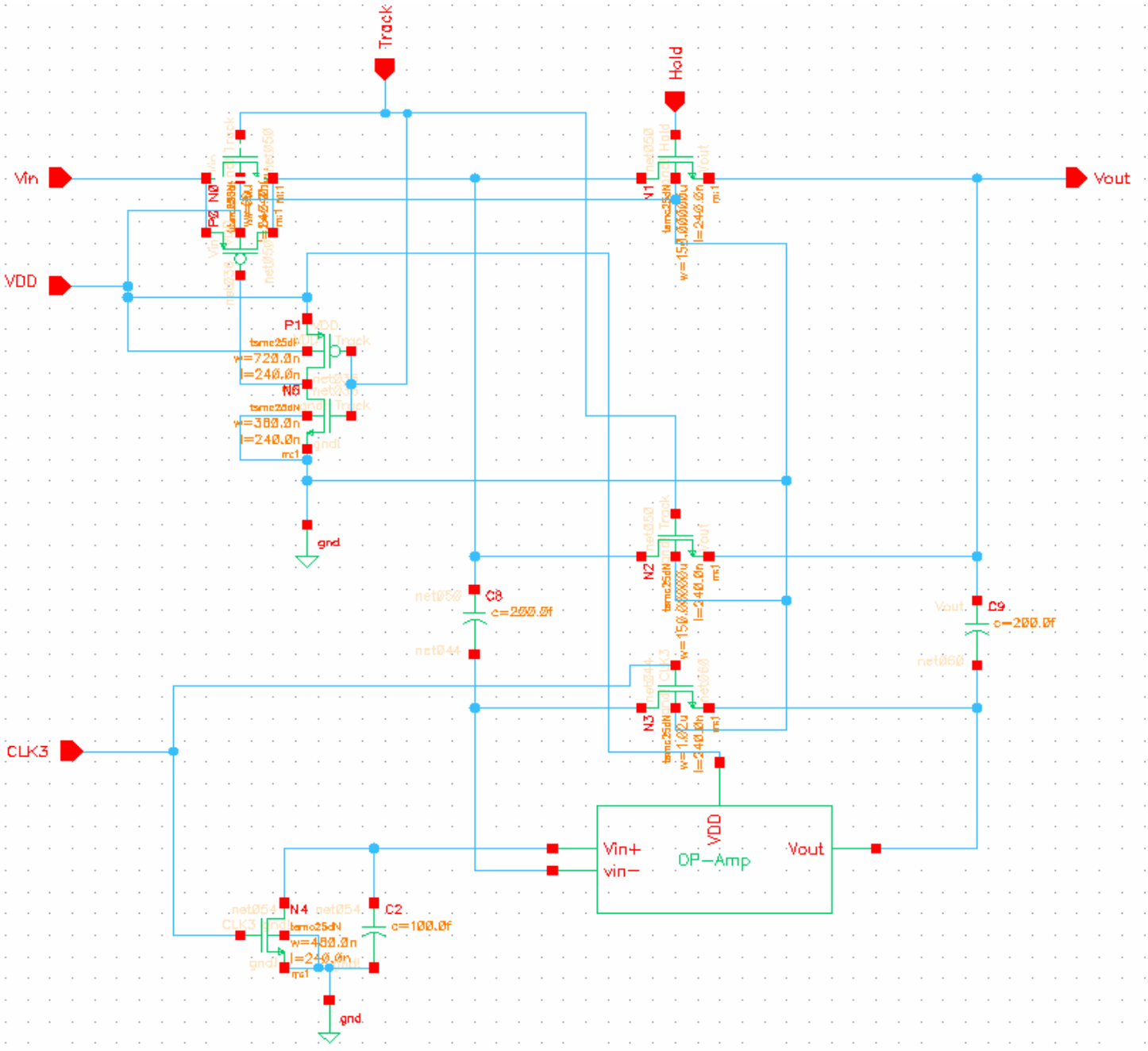
2. 3 to 1 MULTIPLEXER



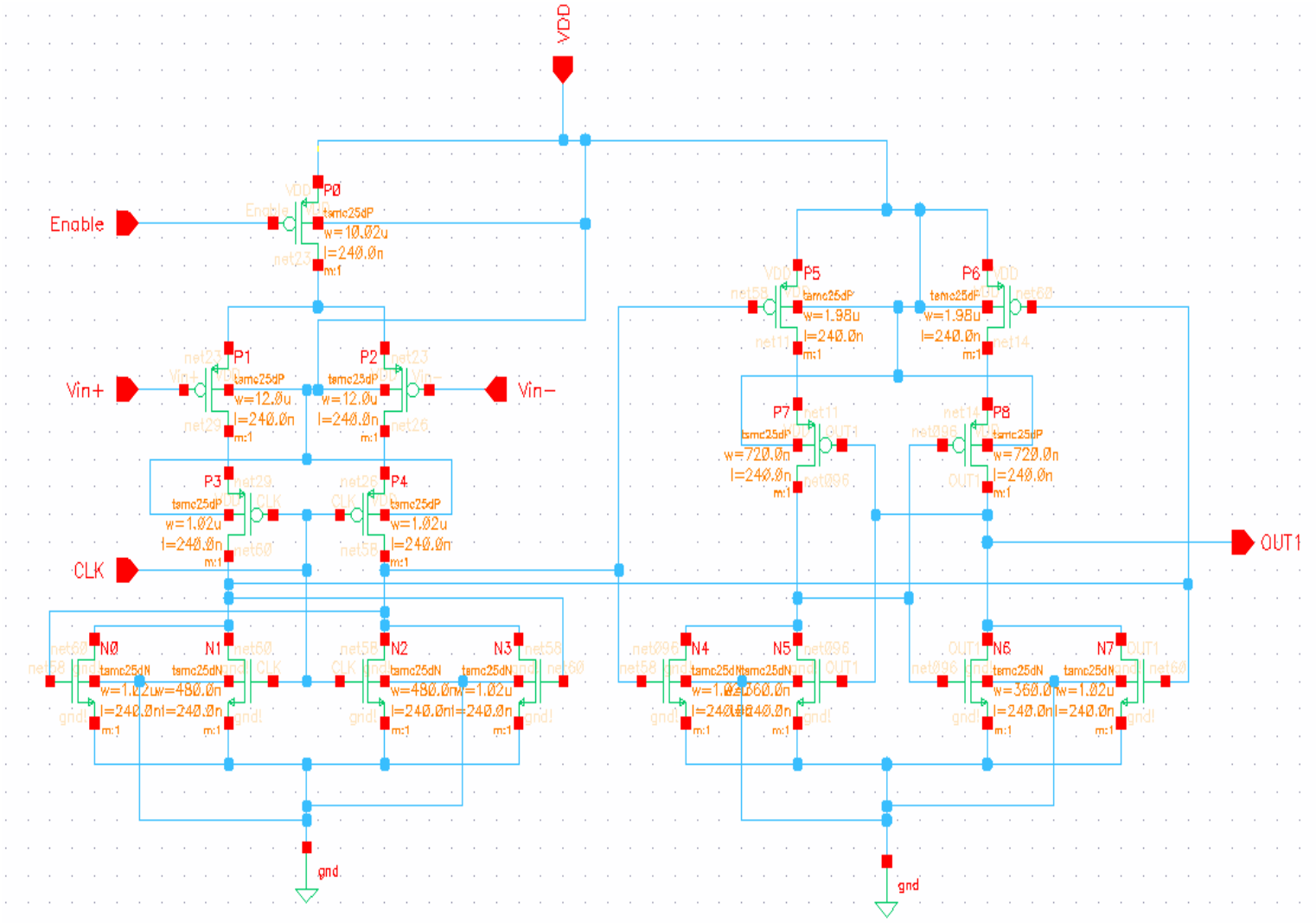
3. D-Flip Flop


set
D
initial
i1
i2
s
out
VDD
d
D-Latch
q
CLK
VDD
supply
d
D-Latch
q
Q
CLK
VDD
CLK
Vin
VDD
Vout

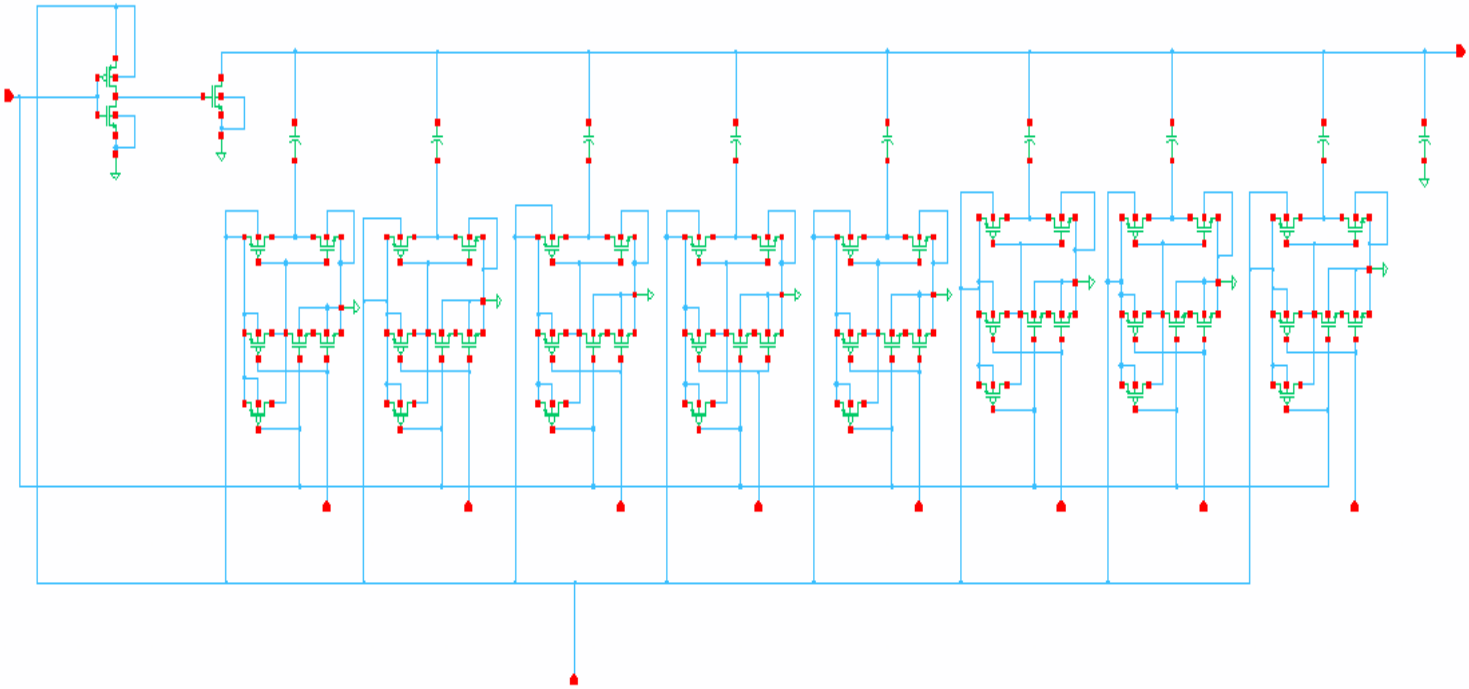
4. Sample and Hold



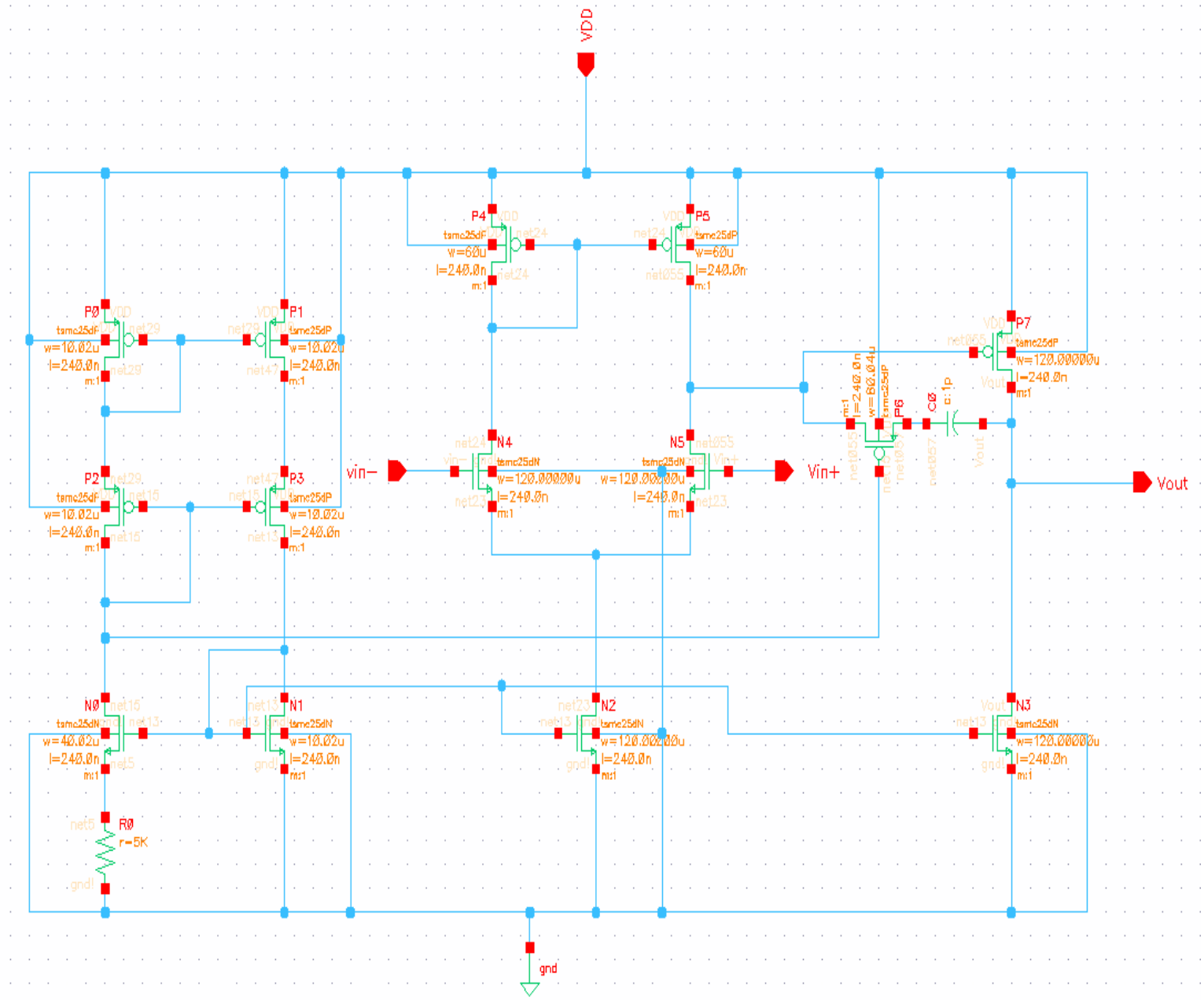
5. Comparator



6. 8 Bit Digital to Analog Converter



7. Operational Amplifier



Vita

Praveen Kumar Palakurthi was born on November 21, 1983 in Hyderabad, India. The son of Rama Rao Palakurthi and Lakshmi Palakurthi, he completed his schooling from Chaitanya High School, Hyderabad. He then entered Jawaharlal Nehru Technological University, Hyderabad, India to pursue Bachelor in Technology degree in the field of Electronics and Communication Engineering. He graduated with a Bachelor's degree in May 2005. Praveen worked in industry for a short duration before joining The University of Texas at El Paso, United States as a graduate student to pursue his Master of Science in Electrical Engineering. His area of research has been VLSI with focus on - Analog Circuit Design. Upon his graduation he will continue towards gaining Doctoral degree.

Permanent address: Praveen Kumar Palakurthi
1-4-10/6/1 Goud Colony, New Maruthinagar
Dilsukhnagar, Hyderabad - 500060
India.

Local address: 1401 N. Oregon Street, #17,
El Paso, Texas – 79902.

This thesis was typed by Praveen Kumar Palakurthi.