2010-01-01

12 Bit Charge Redistribution Digital To Analog Converter For The Residence Time Fluxgate Magnetometer

Miguel Angel Alamillo
University of Texas at El Paso, maalamillo@miners.utep.edu

12 BIT CHARGE REDISTRIBUTION DIGITAL TO ANALOG CONVERTER FOR THE RESIDENCE TIME FLUXGATE MAGNETOMETER

MIGUEL ANGEL ALAMILLO JR, BSEE

Department of Electrical and Computer Engineering

APPROVED:

Eric MacDonald, Ph.D., Chair

John Moya, Ph.D.

Ryan B. Wicker, Ph.D.

Patricia D. Witherspoon, Ph.D.
Dean of the Graduate School

Dedication

To the loving memory of my father.

To the loving memory of my best friend.

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by

MIGUEL ANGEL ALAMILLO JR, BSEE

THESIS

Presented to the Faculty of the Graduate School of

The University of Texas at El Paso

in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE

Department of Electrical and Computer Engineering

THE UNIVERSITY OF TEXAS AT EL PASO

May 2010

Acknowledgements

I would like to thank my graduate research advisor Dr. Eric MacDonald for giving me the opportunity to work in the field I am most passionate about: CMOS Circuit Design. I could have never asked for a better major advisor. Dr. MacDonald has not only expanded my skills in VLSI but has elevated my confidence to do well in my professional endeavors. Thank you Dr. MacDonald, I will always be grateful for everything you have done for me.

Also, I would like to extend my most humble gratitude to all of the SPAWAR team in San Diego, California who introduced me to the exciting field of novel magnetic sensors and funded the fabrication of the silicon designed in this thesis. Joe Neff and Eric Bozeman were an invaluable source of knowledge during all stages of design.

Additionally, I wish to give my sincere thanks to all members of UTEP's ASICs Lab for all their support and interest in this research. In particular, I would to thank Praveen Palakurthi not only for his welcomed suggestions and endless assistance, but for making me feel I was not alone in the intricate but rewarding field of CMOS Analog Circuit Design.

I am also compelled to recognize that without the assistance of the UNIX system administrators and the staff from the ECE Dept. I would have never completed my work.

To Dr. Moya I am obliged for his academic instruction, for his professional advice, and for motivating me to never quit. To Dr. Wicker I am truly grateful for taking a sincere interest in my thesis topic and for highlighting areas of improvement.

Finally, I would like to thank my family and friends who have always believed that I can accomplish anything I set my mind to. My Mother, Tommy, my sister Cynthia, and my sister Melissa are everything to me and I would never be here, if I did not had them behind me thrusting me forward. I love you all.

Abstract

The continuous advances in CMOS VLSI technology have culminated in high speed, low voltage CMOS digital circuits with gate delays below 50 ps at 1.5 V supply. At the same time, high voltage analog signal processing has fallen behind to the high flexibility and high reliability of DSP. However, the main drawback of DSP is the need for high accuracy low distortion data converters and as a consequence of the persistent efforts of reducing size, cost and power of solid-state components the field of CMOS Mixed-Signal circuit design has become of the utmost importance.

The obvious functionality of data converters is to sample a signal (e.g. analog and transform it to a digital domain) and as such converters are extensively used within sensor systems to measure sound, vibration, current, voltage, magnetic field, temperature, light, imaging, acceleration and other physical quantities. A popular magnetic sensor or "magnetometer" is the fluxgate type, which uses a ferromagnetic core wounded by an excitation and a pickup coil to detect weak magnetic vector fields driven by a periodic current. A novel readout scheme currently explored at SPAWAR is represented by the Residence Times Difference (RTD) fluxgate where the detection of the magnetic field resides in time rather than in amplitude.

This thesis will present a low power low distortion and high linearity Digital to Analog Converter (DAC) that can be integrated into a low power mixed-signal Application Specific Integrated Circuit (ASIC) that controls a microwire RTD fluxgate magnetometer to be used in naval operations and may be deployed to other defense markets. A new all digital switching strategy and a new common centroid layout are included. The DAC was designed and implemented in 0.35μm 4M2P CMOS technology. The main results are: $chip\ area = 1.2\,mm \times 1.3\,mm,\ power = 0.6\,mW, INL = \pm 2\ LSB, DNL = \pm 1\ LSB, and\ SFDR = 84\ dBc.$

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Chapter 1: Introduction

Recently, the silicon industry has been striving for integrating more number of circuits into a single core. Extensive development of CMOS technology has resulted in the extreme miniaturization for both devices and interconnects. As of late 2009, Intel has made available to the general public digital microprocessors manufactured at the near atomic feature size of 32 nm. Meanwhile, a recent trend in design has moved into integrating analog circuits together with digital circuits in the same die. Historically, analog circuits have been placed on individual substrates and were only integrated at the board level. However, with the advent of system-on-a-chip (SoC) and the continued progress of Digital Signal Processing (DSP) the need for mixed-signal designs has been rationalized [1].

In 2007 sales for mixed-signal ICs were forecast to increase at an average annual rate of 8% and manufacturing was forecast to grow up 10% each year in the following 5-10 years [2]. The future is bright for mixed-signal processing for which data converters are central. Also, data converters are the gateway to process signals in both digital and analog domains and albeit the expression "the world is going digital" resonates across countries, the real world is inevitably analog [3]. To exploit the computing benefits of DSP the desired analog signal must be translated into a format compatible with digital processors. This is the functionality of an Analog to Digital Converter (ADC). Then a Digital to Analog Converter (DAC) translates the processed digital signal back into a format consumable by analog sensors. These analog sensors may be sight, hearing or an electronic component that restarts the cycle [4-5]. The applications for sensors are innumerable and increasing. Also, a complete listing of the type of sensors can be overwhelming. Some of the most familiar types of sensors are sound, vibration, current, voltage, magnetic, temperature, light, imaging,

and acceleration. Hence, the expanding universe model of analog and mixed-signal opportunities suggests that there will always be a need for a state of the art DAC.

1.1 REVIEW OF MAGNETOMETERS

A magnetometer is an instrument to detect magnetic fields. Furthermore, a vast amount of applications are in need of high sensitivity magnetic sensors, like magnetic anomaly detection, geomagnetism, space magnetometry, magnetocardiography, biomagnetism, Nuclear Magnetic Resonance (NMR) (e.g. low magnetic field), Magnetic Resonance Imaging (MRI), metrological applications, magnetic microscopy, nondestructive testing and analysis and many more [6].

There are essentially four types of magnetometers that can be considered to fulfill a particular magnetic sensing application. Hall Effect sensors produce a voltage proportional to the applied magnetic field but the sensitivity achieved is low. On the other hand, Superconducting Quantum Interference Devices (SQUID) have the highest sensitivity. The operation of SQUIDs is based on a superconducting ring with two Josephson tunneling junctions and flux quantization; however, SQUID sensors require ultra low temperatures to operate. An improvement to the Hall Effect device is the magnetoresistive sensor that has the property of changing resistivity due to a change in the applied magnetic field. Anisotropic Magneto Resistive (AMR) and Giant Magneto Resistive (GMR) sensors have become standard components but both suffer from impedance dependency and the results observed are far from impressive.

In addition, a type of magnetic field sensor that has motivated and intrigued scientists and the research community for the last 40 years is the fluxgate magnetometer. [7-9] has historically been the foremost precursor of the fluxgate idea and [10] has been the contemporary lead investigator. Consistently, the fluxgate sensor has been built using a soft magnetic core wrapped around by an excitation coil and a pickup coil. A driving current, generally sinusoidal, modulates the permeability

of the core and creates changes in the DC flux of the pickup coil. The readout signal is a voltage on the second harmonics of the excitation frequency, as permeability reaches minimum and maximum values twice in each excitation cycle. Fluxgate magnetometers are superior to both AMR and GMR and are well suited for room temperature applications [7-10]. However, the conventional readout scheme for fluxgates has the nuisance of consuming a large amount of power to provide a high amplitude and high frequency excitation signal. A recent trend is to integrate the fluxgate sensor in a CMOS IC by doing post processing on the chip to implant the ferromagnetic core, but miniaturization has yielded low performance [11].

A novel way to operate fluxgate magnetometers at low power and high sensitivity is represented by the Residence Times Difference (RTD) fluxgate where the detection of the magnetic field resides in time rather than in amplitude [12-14].

Extensive work has been recently performed on the RTD fluxgate. The noise effects of this sensor have been characterized in the past [15]. Analysis to find the optimal materials and geometries of the core and coils has been carried out in [16-17]. Investigations on the spatial resolution have also been performed [18]. Creative applications of the RTD fluxgate like magnetic bioassay labeling and estimation of volcanic ash fallout have been presented [19-20]. Prototypes of the RTD magnetomer have been built around Printed Circuit Board (PCB) structures and microwire structures [21-22]. However, as the ongoing research on RTD fluxgates develops, the continued use of prototypes using discrete components on large boards and ideal biasing signals from bulky equipment becomes obsolete. A CMOS readout circuit was achieved in [23] and with the effects of driving mode fully characterized [24] there is a high demand for a CMOS driver circuit. A key component of this IC driver is a high resolution, high linearity, and low power consumption DAC. An inherent low power DAC architecture is charge redistribution since static power is not dissipated.

1.2 CHAPTER ORGANIZATION

The focus of this thesis is to investigate and develop an optimized low power 12 bit charge DAC to fulfill part of the driving block of a novel microwire RTD fluxgate magnetometer with the perspective of assisting the integration of components to reduce cost, size, and power of a new battery powered high sensitivity at room temperature magnetic sensor.

The remainder of this thesis is organized as follows. In Chapter 2 an exposure to the RTD fluxgate magnetometer is given followed by a discussion of designing low power mixed-signal circuits. Chapter 3 defines all the figures of merit involved in the design of data converters. A basic overview of popular Nyquist DAC architectures is presented in Chapter 4 continued by a survey of previous works. For Chapter 5 the methodology, circuit design, and technology considerations of the proposed 12 bit charge DAC is presented. Chapter 6 discusses the simulation results and describes the design environment and the algorithms used to characterize the static and dynamic behavior of the data converter. A comparison with state of the art designs is also included. Chapter 7 provides the conclusion and future work. Appendix A lists the VerilogA code for modeling an ideal 12 bit ADC and Appendix C presents OCEAN, a tool for automating SPICE level simulations. Finally, Appendix C includes a sample MATLAB algorithm for calculating DNL and INL.

Chapter 2: Background and Motivation

Magnetic field detectors have a strong demand in naval and space exploration operations and can be a great asset in the law enforcement field if integration into an energy efficient portable package can be achieved [6]. However, high performance (e.g. high sensitivity) magnetometers are either energy hungry devices or lack the accuracy to differentiate true signals from noise [10-11].

Recently, fluxgate magnetometers have received a boost of interest as a means to sense weak magnetic field vectors in the range of micro tesla with a resolution of 100 pT at room temperature. Conventional read out schemes are based on the second harmonic detection of the output voltage and cover most of the Fluxgate literature. A novel read out scheme has been presented based on the residence times difference (RTD) fluxgate. The time domain readout strategy has several unique features such as a simple sensor structure, intrinsic digital form of the output and a power consumption decrement with an increasing sensitivity demand. [12]. The aim of this work is to develop an energy efficient and high accuracy digital to analog converter design that can be integrated into a low power mixed-signal Application Specific Integrated Circuit (ASIC) that controls a magnetometer that will be used in naval operations and can be deployed to other defense markets.

2.1 RESIDENCE TIME DIFFERENCE FLUXGATE

The RTD fluxgate was developed at the DIEES laboratory in Catania, Italy, in collaboration with scientists from the SPAWAR System Center, San Diego, California. The novel sensor is based on a two coil arrangement wound around a suitable ferromagnetic core having a hysteric input-output characteristic. The working principle illustrated in Fig. 2.1 is that a periodic driving current I_e is forced in the excitation coil and generates a periodic magnetic field H_e parallel to the geometry of

the core. When a target field H_X is applied in the same direction of H_e, a voltage measured at the pickup is correlated to the target magnetic field.

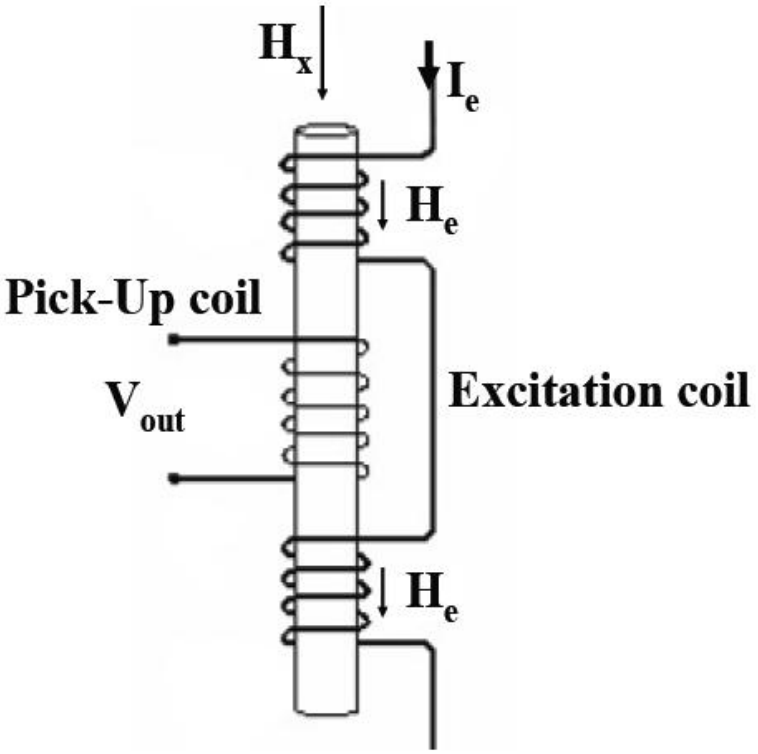


Figure 2.1: RTD fluxgate sensor [23].

The magnetic core has two switching thresholds corresponding to the coercive field levels H_C and $-H_C$, and a two state output symbolized by M_{SAT} and $-M_{SAT}$. In order to reverse the core magnetization from one steady state to the other, He must cross the switching thresholds of the magnetic core. In the absence of Hx, the time interval the core remains magnetized in the two steady states is symmetric and receives the name Residences Time. In the presence of H_X the total applied magnetic field $H_e + H_X$ is skewed and results in asymmetric Residence Times. Figure 2.2 illustrate both cases. T^+ represents the time spent crossing the upper H_C level and the following crossing of the lower H_C level. Conversely, T^- represents the time interval between the lower H_C level and the successive upper H_C level [12-14].

The output behavior of the RTD fluxgate seen in Fig. 2.3 is a voltage measured at the pickup coil with the form of a spike train. The readout circuits described in [23] modifies the spike train signal into a square wave via a Schmitt Trigger (i.e. a digital signal containing the RTD).

Successful prototypes of the RTD fluxgate magnetomer have been built around PCB structures and microwire structures [21-22]. Additionally, the recent improvements of VLSI technology and new material processing have opened the door to novel approaches realizing miniaturized magnetic sensors via either Micro Electro Mechanical Systems (MEMS) or monolithic CMOS chips. In [25] a two-chip system consisting of an integrated sensor chip and an ASIC for biasing and signal processing was developed. Later, [26] built a sensor using a single CMOS chip that required additional mask steps to electro deposit a NiFeMo film to act as the ferromagnetic core. Kawahito et al. also presented a single chip solution with a delta-sigma modulator and integrator in the feedback loop [27-29]. [30] introduced the concept of combining a flat CMOS structure and amorphous ferromagnetic material, obtained from a photolithography process, to achieve a parallel fluxgate configuration. [31] presented a low power 2-D fully integrated CMOS fluxgate sensor with a novel digital feedback principle to improve linearity and to extend the linear working range.

Albeit the miniaturization of the fluxgate sensor provides a dramatic reduction in size, the loss of performance is not trivial for many applications. Increase in magnetic noise, low resolution, and low sensitivity are common problems associated with the monolithic system solutions. Hence the market for PCB and microwire fluxgates structures is vast and expanding. Table 2.1 shows a comparison of some of the state of the arte fluxgate sensors.

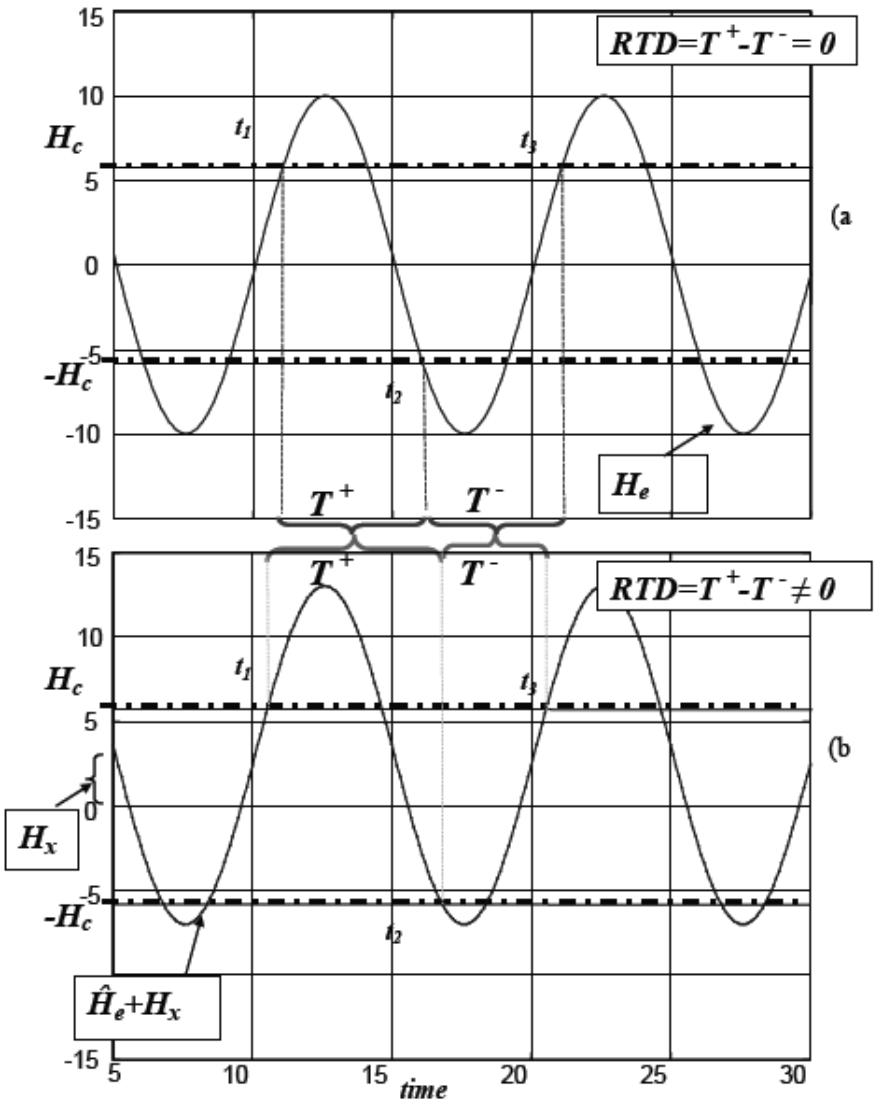


Figure 2.2: Typical RTD fluxgate magnetic field signal [23].

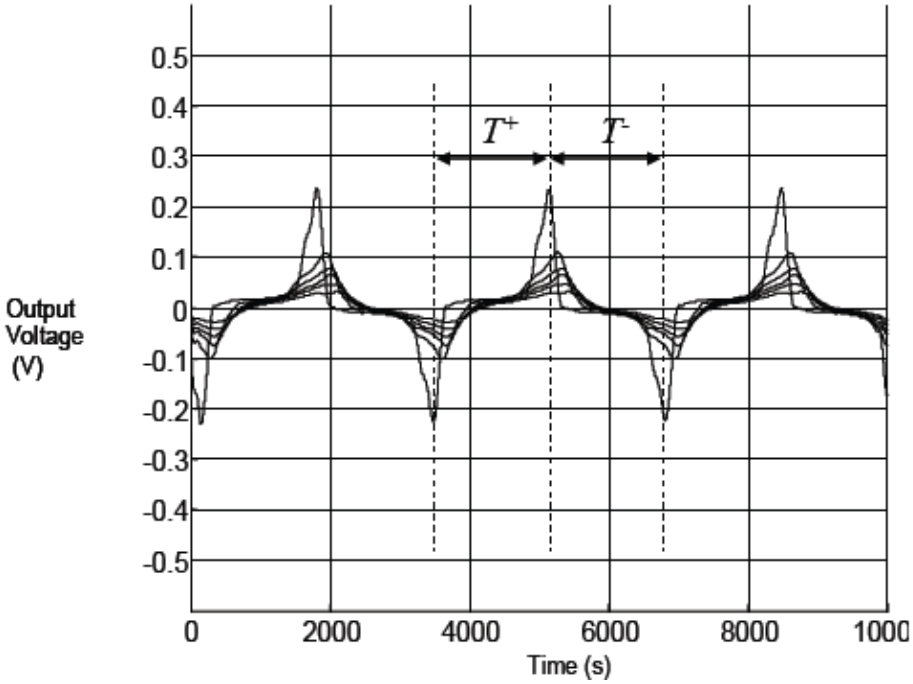


Figure 2.3: Typical RTD fluxgate pickup coil output voltage [23].

Table 2.1: Comparison of micro fluxgate magnetometers.

Source	*Sensitivity* *(V/T)*	$Noise$ $(nT/\sqrt{Hz})$	V_{DD} *(V)*	*Power* *(mW)*
[25]	70	≥60	5	160
[26]	70	≥200	5	325
[27-29]	22.5	150	≥5	≥400
[30]	170	55	5	12.5
[31]	92.5	15	2.5	10

2.2 LOW POWER MIXED-SIGNAL DESIGN

An overall reduction in cost and power consumption, enhanced system reliability, and improved debugging capability, primarily for board designers are the main advantages of seeking a low power mixed-signal design [1].

However, placing fast accurate analog circuits and high speed digital blocks on the same die often results in more challenges for the analog circuit designers than the digital designers. Parameters such as power supply noise, substrate noise, and cross talk are typically created by the digital blocks and can produce more difficulties for the analog circuits than any other block in the die. Thus, any analog designer must be aware of the possible problems and solutions in a mixed-mode environment.

The most typical problems for analog circuits built in a mixed-signal design are power supply noise, layout and floor planning, accuracy and speed requirement, substrate noise, crosstalk, and designing for process voltage temperature (PVT) variations and scalability.

High current surges can create unwanted Electro Magnetic Interferences (EMI). EMI can be destructive for analog block but no so for digital blocks. Consequently, separate power supply and ground pins for analog and digital cells are always essential in any mixed mode application. At the submicron and deep submicron feature sizes, the risk of crosstalk between two closely spaced metal traces increases. Extra grounded wires are placed in between two sensitive traces to keep them isolated. Guard rings are also used to collect the injected current from the substrate.

The layout of analog circuits is highly sensitive to gradients and random variables and as the minimum device sizes are reduced and the need for faster analog cells is increased, analog designers are facing with choosing small channel length devices to meet the speed requirement, while sacrificing matching and accuracy. Careful layout techniques along with advanced packaging technologies are essential in a mixed-signal design [32].

More than often the analog blocks built in mixed-signal chips are optimized for a particular technology. This may be a problem if the design needs to be scaled to a new technology for purposes of reducing cost and increasing yield where a certain design feature may not be available.

The recent trend in digital circuit design towards fast and energy efficient devices has lead to the reduction of power supply voltages, which consign a heavy load to high performance analog circuits. Furthermore, there is an inherent problem with analog building blocks: there are no ideal designs, just configurations, which can be optimized for a particular application. The fact that there are no standard analog cells readily available is notorious whereas reliable libraries of standard digital cells are easily available.

Chapter 3: Performance Metrics of Data Converters

Data converters are central components of communication systems like DSP and SoC. The integration of a converter into a complex system requires the knowledge of the architecture's limitations and how the particular implementation affects system performance. Since data converters used in different applications require different specifications there is a need to characterize how well is the performance. This section describes the characterization of data converters in terms of static and dynamic parameters [34-39].

3.1 THE IDEAL DIGITAL TO ANALOG CONVERTER

The purpose of a DAC is to take a digital input of n bits and transform them into a sequence of pulses whose amplitude is the analog representation of the digital code. A reconstruction process is used after the DAC to convert the sampled data into a smoothed analog signal. Figure 3.1 illustrates an example of how DACs are used in data systems.

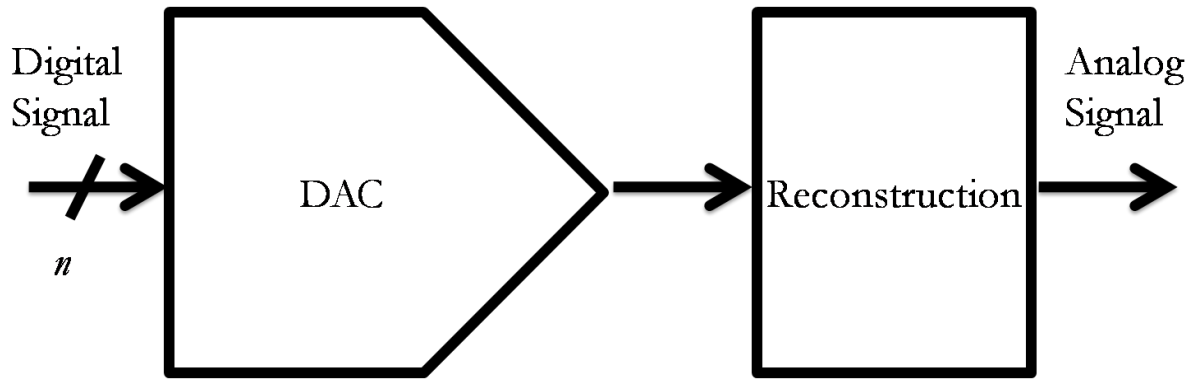


Figure 3.1: Ideal DAC in a data system.

The analog output of a DAC is typically a voltage or a current that represents a portion of a reference signal. Albeit voltage and current output DACs are equally employed in literature and

industry, voltage output DACs continue to be the preferred choice for the novice designer. In the case of a voltage output DAC, the ideal output signal can be defined as

$$\boldsymbol{v_{out} = \alpha * V_{ref}} \tag{3.1}$$

where α is the fraction of V_{ref} to be seen at the output calculated as

$$\boldsymbol{\alpha = [b_0 2^{-1} + b_1 2^{-2} + \cdots + b_{n-2} 2^{-n-1} + b_{n-1} 2^{-n}]} \tag{3.2}$$

and depends on the value of the digital input $\boldsymbol{x_d}$with n bits expressed as

$$\boldsymbol{x_d = [b_0, b_1, \ldots, b_{n-2}, b_{n-1}]} \tag{3.3}$$

In Eq. (3.3) b_0 is the MSB and b_{n-1} is the LSB and all the elements are 0 or 1.

3.2 BASICS

The first parameter of interest in a data converter is the resolution, which is specified by n the number of bits in the digital input. The resolution of a DAC indicates the number of individual and uniform quantized steps that are possible to resolve. The value of a single step is the quintessential unit of measure for data converters and is define as

$$\boldsymbol{LSB = \frac{V_{ref}}{2^n}} \tag{3.4}$$

According to Eq. (3.3) α cannot be equal to one. An infinite number of bits would be necessary to have the contrary. Therefore, a measure of how close the analog output can be to V_{ref} is needed. The relationship is called the full scale range (FSR) and is given by

$$\boldsymbol{FSR = V_{ref} - LSB} \tag{3.5}$$

Figure 3.2 is a plot of the input-output characteristic of 4-bit DAC which shows how the 16 uniform steps form a staircase waveform and that each binary word corresponds to a unique analog output value. Note that the input-output characteristic has been shifted vertically by $-1/2LSB$.

Furthermore, from the previous discussion and Eq. (3.5) comes forward the concept of quantization error or quantization noise. To better understand this term lets considered the plot of Figure 3.3. The graph is a sawtooth signal that indicates how far away is the output value of a n bit DAC from the output value of an infinite bit DAC. This separation is never greater than $1LSB$ and can be designed to be $\pm 1/2LSB$ as a result of shifting vertically the input-output behavior of the converter. Simple mathematical analysis shows that the root-mean-square value of the quantization noise can be expressed as

$$\boldsymbol{Q_{noise} = \frac{LSB}{\sqrt{12}} rms} \tag{3.6}$$

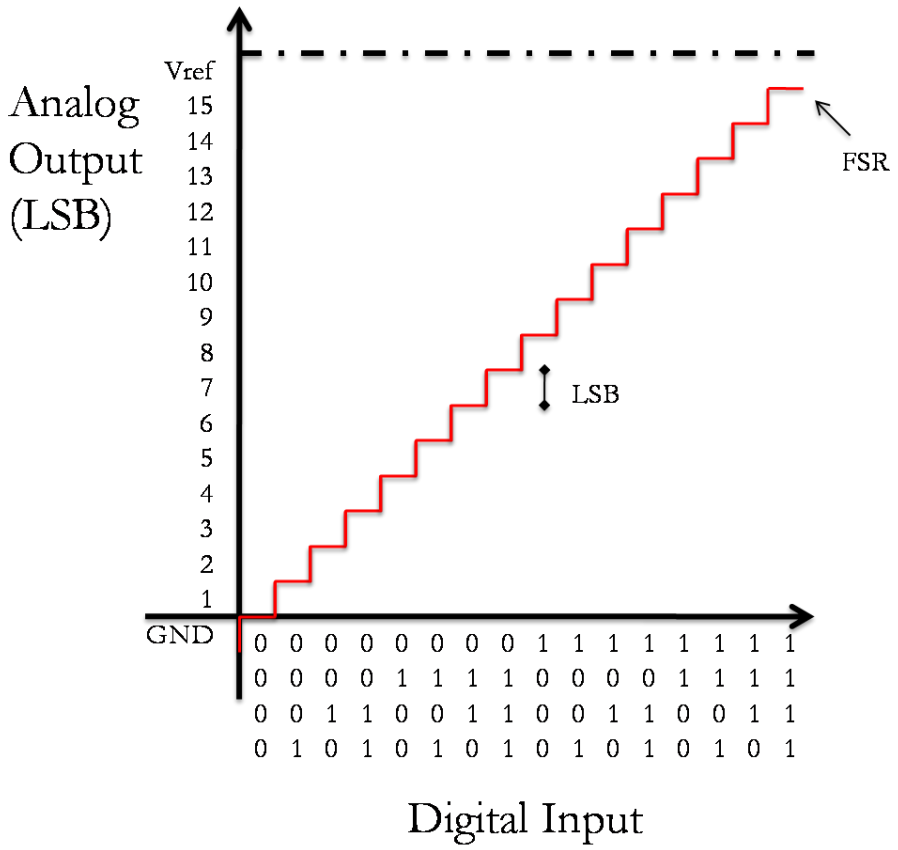


Figure 3.2: Ideal input-output behavior of a 4-bit DAC with a vertical shift of $-1/2LSB$.

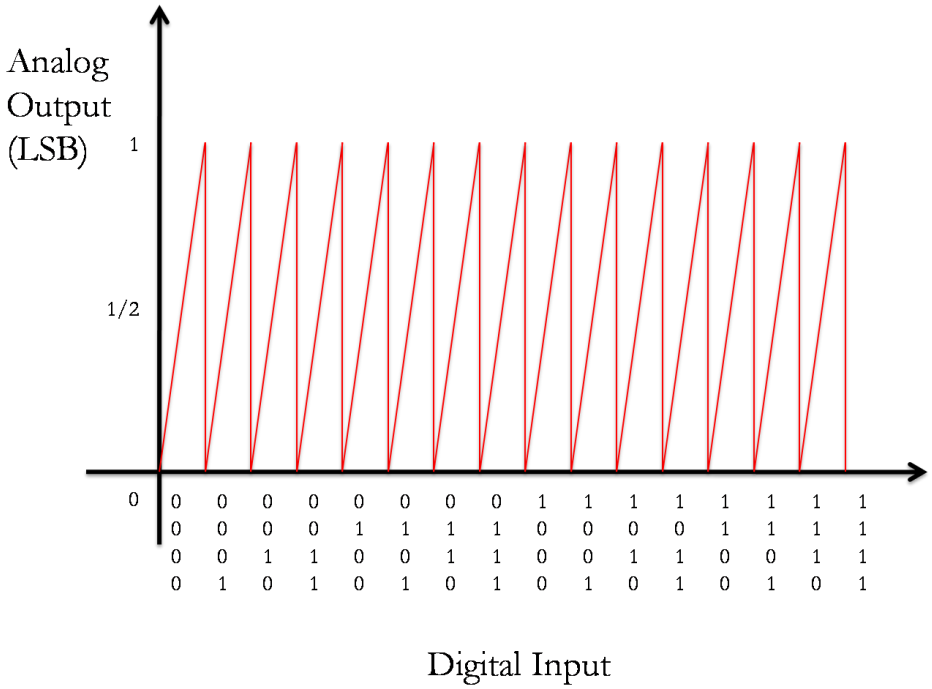


Figure 3.3: Sawtooth error signal modeling the quantization noise of the 4-bit DAC.

3.3 STATIC PARAMETERS

Practical implementations of data converters will inevitably stray from the ideal situation depicted in Fig. 3.2. The mismatch between equal components will be most common source of static errors. Therefore, Eq. (3.1) cannot be reconstructed perfectly and so a designer strives to make the actual output signal to be

$$\tilde{v}_{out} \cong \alpha * V_{ref} \tag{3.7}$$

The following are the most common static conversion errors used to describe the performance of a DAC. These parameters are normally measured in LSB.

3.3.1 Offset Error

The offset error is the difference between the ideal analog output and the actual analog output of a DAC for a given digital input and can be measured at any value of the digital input, but many authors prefer to measure the difference for zero input or

$$\boldsymbol{E_{offet} = \frac{\tilde{v}_{out}}{LSB}\Big|_{b_{n-1}}} \tag{3.8}$$

3.3.2 Full Scale Error

The full scale error or full scale gain error is similar to E_{offet} but this parameter is commonly evaluated at the MSB instead such as

$$\boldsymbol{E_{full-scale} = \frac{\tilde{v}_{out}}{LSB}\Big|_{b_0} - 2^n - 1} \tag{3.9}$$

3.3.3 Gain Error

The combination of Eq. (3.6) and (3.7) yield another valuable parameter called the gain error which measures the error on the slope of a straight line interpolating the input-output characteristic of the converter and can be defined as

$$\boldsymbol{E_{gain} = \frac{\tilde{v}_{out}}{LSB}\Big|_{b_0} - \frac{\tilde{v}_{out}}{LSB}\Big|_{b_{n-1}} - 2^n - 1} \tag{3.10}$$

Or more conveniently as

$$\boldsymbol{E_{gain} = E_{full-scale} - E_{offet}} \tag{3.11}$$

3.3.4 Differential nonlinearity error

Differential nonlinearity (DNL) is a description of how uniform is the size of the steps through the entire combination of the digital input. A DNL value of zero indicates that the step size is ideal (i.e. one LSB) and can be with computed as

$$\boldsymbol{DNL_k = \tilde{v}_{out}|_{k+1} - \tilde{v}_{out}|_k - LSB} \tag{3.12}$$

where k is the index of the digital input applied.

3.3.5 Integral nonlinearity error

Integral nonlinearity (INL) is a description of how close is the actual analog output to the ideal analog output. The calculation of INL for the k digital input is

$$\boldsymbol{INL_k = \tilde{v}_{out}|_k - v_{out}|_k} \tag{3.13}$$

The above expression yields an absolute value of INL. However, the standard practice is to compensate the offset and gain errors before calculating INL. Compensation is done with a best-fit line or an end-point line.

3.3.5 Monoticity

In order for a data converter to be monotonic, every change in the digital input ought to result in a change in the analog output in the same direction. That is, if the input increases the output increases, but if the input decreases the output decreases. Monoticity is ensured if the relative INL can be confined to

$$\boldsymbol{|INL_k| \leq \frac{1}{2} LSB \; for \; all \; k} \tag{3.14}$$

The above relationship is a sufficient, but not a necessary condition to guarantee Monoticity.

3.4 DYNAMIC PARAMETERS

The static parameters of a data converter are not enough to have a full characterization. Dynamic conversion errors are as important and are mostly dependent on the signal and frequency to be reconstructed and are more prominent as the amplitude and frequency increase.

3.4.1 Settling time

This is the amount of time the DAC takes to settle to within $\frac{1}{2}LSB$ of the final analog output value as a result of a change of the digital input value. The maximum settling time occurs at

half scale when the MSB changes. Also, to calculate the maximum sampling rate of a DAC from the settling time the following equation is used

$$\boldsymbol{sampling\ rate\ (max) = \frac{1}{settling\ time}} \tag{3.15}$$

3.4.2 Glitch Energy

During transitions of the digital input a short impulse may appear momentarily at the analog output. The impulse is caused by a time mismatch in the bit transitions. The glitch energy represents the area under the inducted pulse and is measured at half scale in units of volts-second.

3.4.3 Latency

This metric considers the settling time plus the delay from the time the digital input changes.

3.4.4 Signal-to-Noise Ratio

The ratio of the root-mean-square (rms) value of the output signal to the rms value of the quantization noise is called Signal-to-Noise Ratio (SNR). This frequency domain parameter is not absolute and is dependent of amplitude and is expressed as

$$\boldsymbol{SNR = \frac{v_{out}rms}{Q_{noise}rms}} \tag{3.16}$$

For the reconstruction of sine wave the maximum SNR is defined in decibels (dB) as

$$\boldsymbol{SNR_{max}dB = 6.02n + 1.76} \tag{3.17}$$

If the reconstructed signal is a triangle wave then

$$\boldsymbol{SNR_{max}dB = 6.02n} \tag{3.18}$$

3.4.5 Total Harmonic Distortion

The Total Harmonic Distortion (THD) is calculated by taking the ratio between the root-mean-square of the signal and the root-mean-square of the second to tenth harmonics.

3.4.6 Signal-to-Noise-and-Distortion Ratio

The Signal-to-Noise-and-Distortion Ratio ($SNDR$) accounts for both harmonics and noise and is found by taking the ratio of the root-mean-square (rms) value of the output signal to the root-sum-square value of the quantization noise including AC harmonics (i.e. zero frequency is omitted).

3.4.7 Dynamic Range

The Dynamic Range (DR) of a DAC is the value of the analog output that makes SNR and $SNDR$ equal to 0 dB. The expression to calculate DR is

$$\boldsymbol{DR\ dB = 6.02n} \tag{3.19}$$

3.4.8 Effective Number of Bits

A figure of merit that combines several of the above parameters is called the Effective Number of Bits ($ENOB$). For a full scale sinusoidal reconstruction $ENOB$ is determined by

$$\boldsymbol{ENOB = \frac{SNDR\ dB - 1.76}{6.02}} \tag{3.19}$$

The $ENOB$ value provides a valuable metric to directly compare DAC implementations.

3.4.8 Spurious Free Dynamic Range

The Spurious Free Dynamic Range ($SFDR$) is a measure of the difference in power between the output signal and the largest spur present in the frequency spectrum. $SFDR$ is measured in decibels below carrier (dBc) and excludes harmonic distortion.

Chapter 4: Nyquist Rate DAC

Digital to analog converters are grouped in different ways. First, a distinction is made serial or parallel also called flash DACs. Another classification is by the sampling frequency f_s used. If f_s is much higher than the analog signal bandwidth f_B, the converter is called an Oversampling DAC. Alternatively, a Nyquist Rate DAC guarantees the following

$$\boldsymbol{f_s = f_N = 2f_B} \tag{4.1}$$

where f_N is called the Nyquist Rate. In reality, Nyquist Rate DACs use sampling frequencies several times higher than that of Eq. (4.1). Additionally, flash DACs are further classified by the electrical quantity used in the scaling network used to generate v_{out}; voltage, current, or charge

4.1 VOLTAGE SCALING

Figure 4.1 shows a 2 bit resistive divider network connected in series between ground and the reference signal V_{ref}. The divider is composed of 2^2 resistors R of equal value. A binary tree of switches controlled by the digital input bits selects the fraction of V_{ref} to appear at v_{out}. The switches are realized with analog multiplexers (MUX). The value of the switches on-resistance and the parasitic capacitances limit the speed of conversion. The circuit shown in Fig 4.1 is also called a Kelvin Divider.

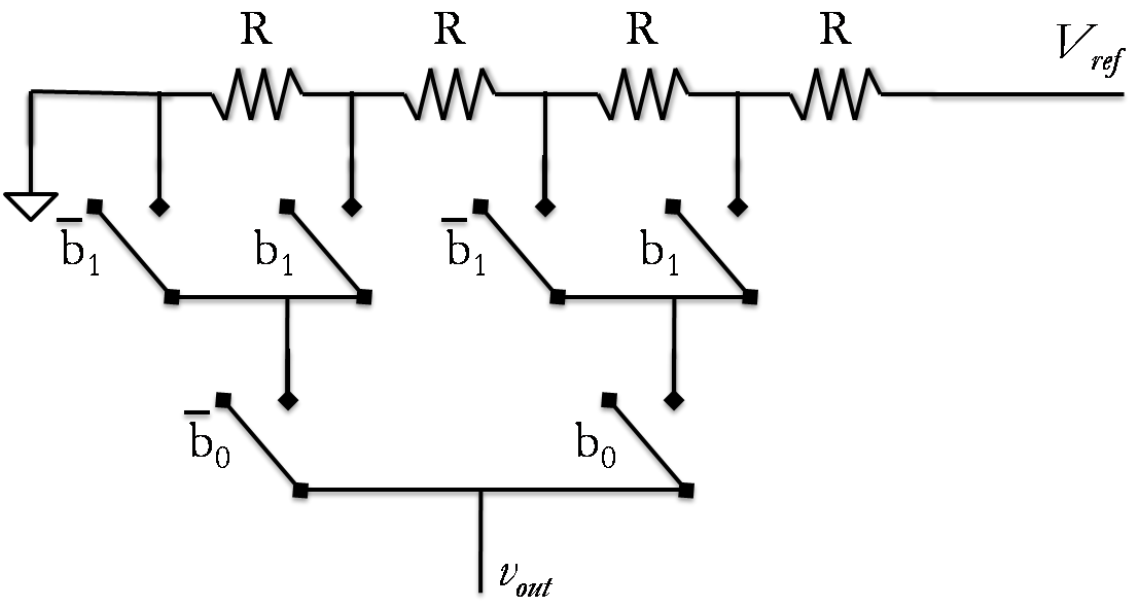


Figure 4.1: Voltage scaling DAC architecture.

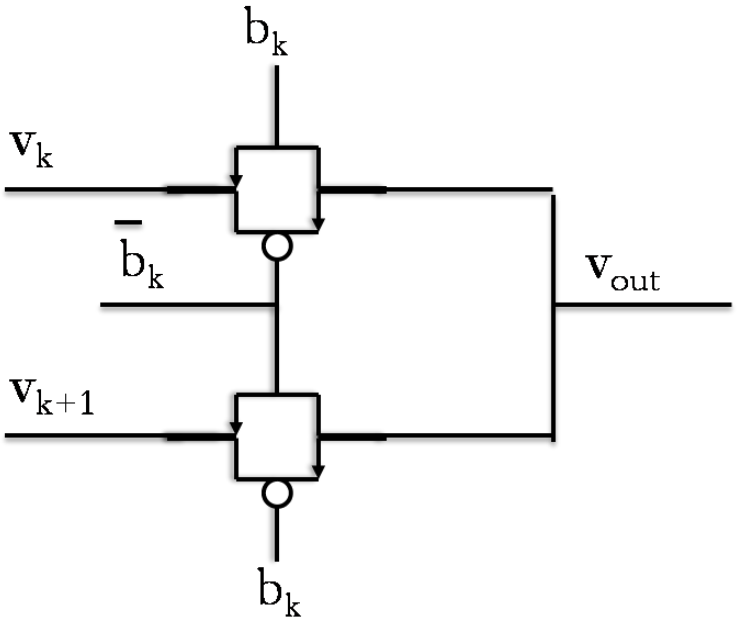


Figure 4.2: Analog voltage MUX switch.

4.2 CURRENT STEERING

Current steering architectures work by converting a reference signal into a set of n binary weighted currents or a set of 2^n uniform segment currents. Resistors as well as transistors may be used. If the sum of the contributing currents is connected to an op amp on the inverting configuration an analog voltage is obtained. In this configuration each resistor or transistor is doubled in sized compared to the nearest neighbor element. Figure 4.3 shows a 4 bit binary weighted implementation using transistors. The switching function of current steering DACs is done with a differential pair and is called a current steering cell. An example of this switch is shown in Fig. 4.4 where $M1$ and $M2$ are sized equally to reduce an offset voltage. The current cell switch composed of $M1$, $M2$, and $M3$ may be sized uniformly of binary weighted depending on the resolution and application of the converter.

Another implementation of a current steering converter is the R-2R configuration seen in Fig. 4.5. As the number of bits used is increased, a large component spread limits the effective resolution of the DAC. On the other hand, the R-2R ladder network only uses resistors of value R and 2R so matching components becomes less of a nuisance. A high degree level of matching can be obtained using common centroid geometries.

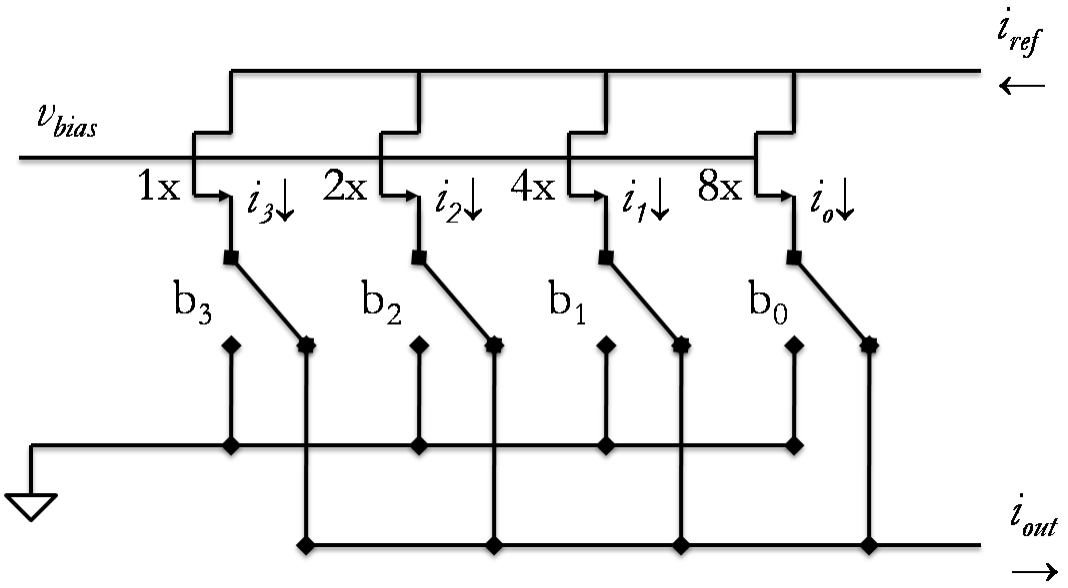


Figure 4.3: Current steering DAC architecture.

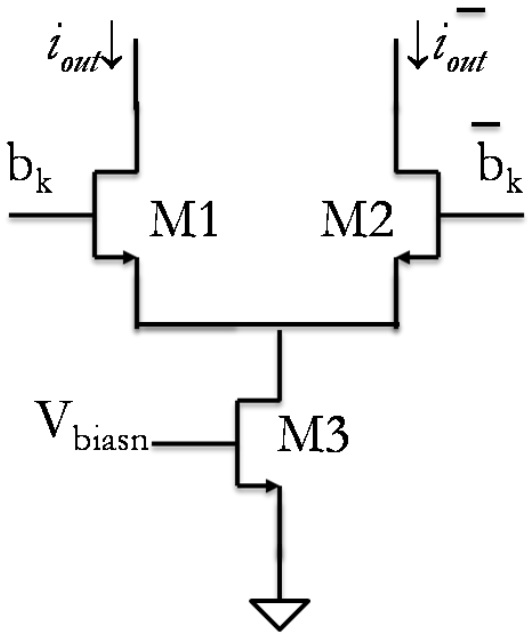


Figure 4.4: Current steering cell.

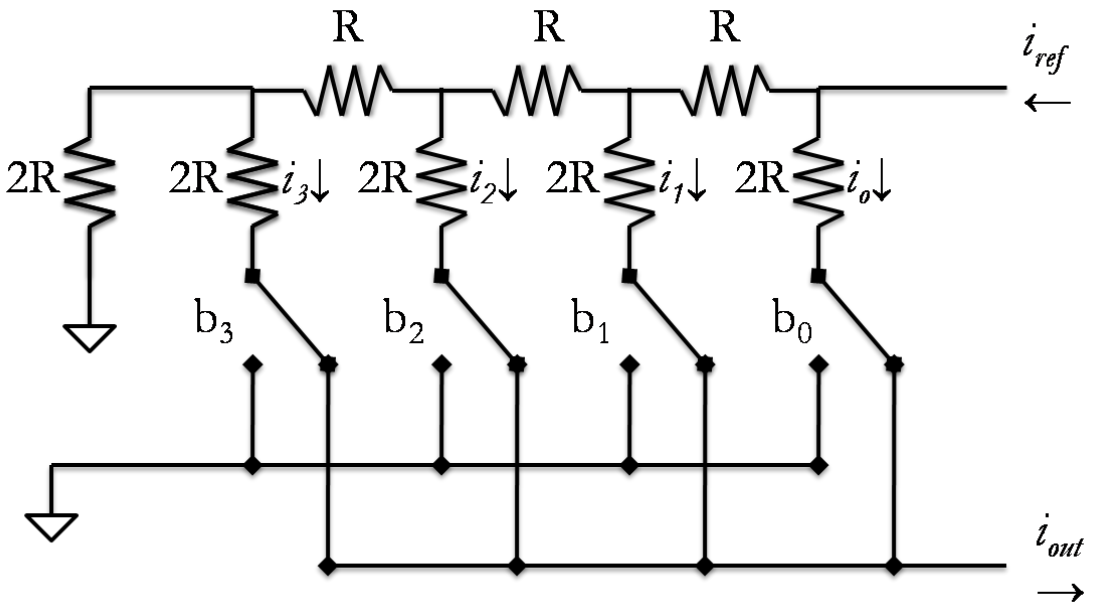


Figure 4.5: R-2R 4 bit DAC.

4.3 CHARGE REDISTRIBUTION

A charge DAC is constructed with capacitors and is a popular architecture for low power designs because the static power consumption is zero. A binary weighted array of capacitors is used to literally attenuate the output voltage by distributing the charge present at each capacitor. A 4 bit implementation is shown in Fig. 4.6. The switching logic is typically done with NMOS pass transistors with complementary input signals. Figure 4.7 illustrates how this switch is implemented. The Nonlinearity of a charge DAC is caused by three sources: capacitor mismatch, inherent capacitor nonlinearity, and parasitic junction capacitance from any MOS switch connected at the output node.

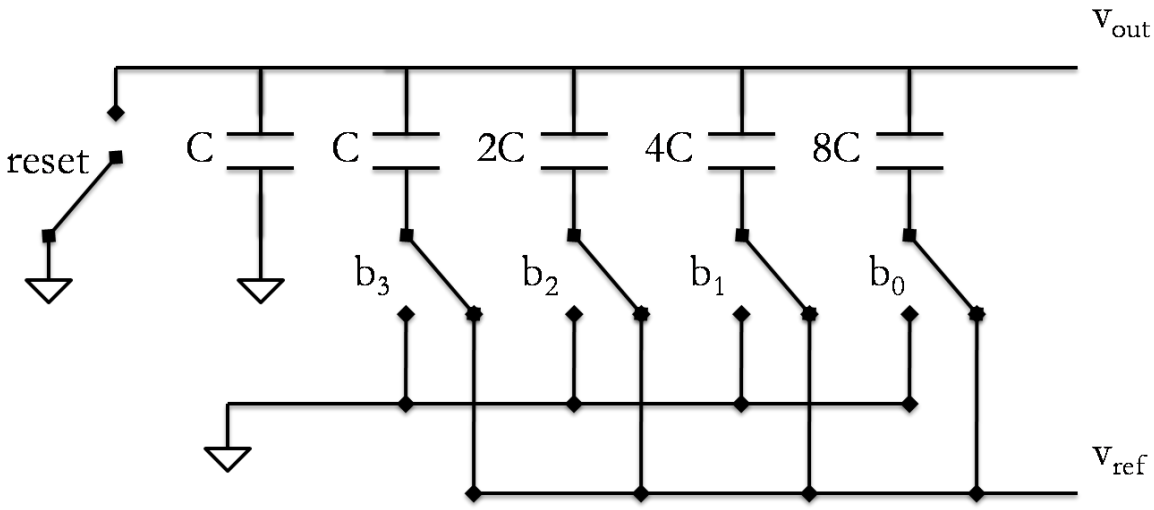


Figure 4.6: Charge redistribution architecture.

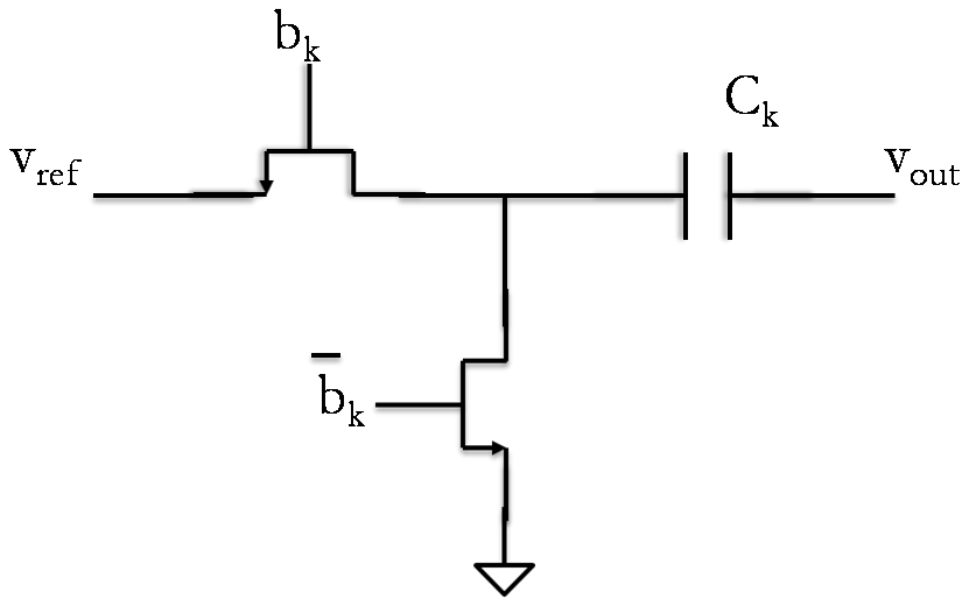


Figure 4.7: Conventional charge DAC switch

4.4 PREVIOUS WORKS

Present-day DAC designs are broken up into two classes: Nyquist-rate DACs and Oversampling DACs. In the former, the sampling frequency is at least two times the frequency of the reconstructed analog signal, (i.e. the Nyquist frequency) and in the latter the sampling frequency is at least eight times the frequency of the desired signal. Nyquist-rate DACs are also classified on the way the input code is fed into the system. If the input data is fed through in serial fashion, the converter is called a serial DAC and has the advantage of reducing hardware complexity. Now, if the input data is fed through in parallel fashion, the converter is called a flash DAC and has the advantage of performing conversions in a single clock cycle. Flash DACs are based on scaling voltage, current or charge. Each technique has benefits and detriments. Monoticity, accuracy, and sensitive to parasitic are some of the factors that can determine the architecture to be used. Among these architectures charge scaling DACs are popular in low power designs because there is no static power dissipated [5].

Conventional implementation of charge DACs use equal size capacitors connected to a common top plate and have the individual bottom plates connected to a switch controlled by the digital input that selects to connect the bottom plate to ground or a reference voltage. Depending on the value of the input word the capacitor array redistributes the charge in the network and produces a corresponding output value that is a fraction of the reference signal. However, for high resolutions the size of the scaling array requires 2^n capacitors and 2^n switches. A better approach is to use a binary weighted array that uses only n capacitors and n switches. Other approaches, attempt to reduce area by sacrificing linearity, speed, and complexity. The following is brief review of different charge redistribution DACs found in the literature.

An example of small area but low speed converter is the serial DAC from [40] but also has poor linearity due to excessive switching. A high speed architecture proposed in [41] requires small area but consumes a vast amount of power. Another charge architecture that decreases area is the C-2C seen in [42] but parasitic capacitances have a dramatic impact on linearity so this approach is only feasible in silicon on insulator (SOI) process for high resolution DACs. Recently, a multi step approach was demonstrated to have low power consumption and high linearity at the expense of speed [43].

In all of the above designs summarized in Table 4.1, there is a trade of speed or linearity for area and consequently those converters have a limited range of applications. Table 4.2 shows a comparison of different DAC architectures and other interesting DAC designs are found in [52-64]. The RTD magnetometer requires a high linearity high speed and low power DAC to generate the bias current signal and the binary weighted architecture provides this possibility.

Table 4.1: Comparison of charge DACs in literature

Type	**Bits**	***Area***	***Speed***	***Linearity***	***Matching***	***Complexity***
Serial [40]	10	2C	0.1	Low	High	Moderate
Two-stage buffer [41]	10	64C	1	High	Moderate	High
Two stage [42]	10	64C	1	Moderate	Moderate	High
C-2C [43]	10	29C	>1	Low	High	Low
PseudoC-2C [44]	10	38C	>1	Moderate	High	Low
Multi-step BW [45]	10	32C	0.5	High	High	Moderate
This work	12	4096C	1	High	Moderate	Moderate

Table 4.2: Comparison of DAC architectures in literature

	[46]	**[47]**	**[48]**	**[49]**	**[50]**	**[51]**	**This work**
architecture	current steering	current steering	R-2R ladder	Resistor ladder	Resistor String	Current steering	Charge scaling
bits	10	10	10	10	10	10	12
Technology	0.35µm	0.18µm	0.18µm	0.35µm	0.13µm	0.35µm	0.35µm
Power (mW)	≤7.8	<22	4	n/a	0.5	≤0.6	<0.6
Area (mm2)	0.23	0.35	0.01	0.022	0.18	0.18	1.5
INL (LSB)	0.2	0.1	.75	.70	2.0	0.42	0.5
DNL (LSB)	0.2	0.1	.70	.35	0.5	0.42	0.5
Speed	30Ms/s	250M/s	Low frequency	3µs/10pf	2Ms/s	2µs	2µs
output	≤2.25mA	≤10mA	<2.2mA	Voltage no buffer	Voltage high swing	Voltage high swing	Voltage high swing

Chapter 5: Proposed 12 Bit Charge DAC

The proposed system consists of two main blocks: charge DAC and output amplifier. The DAC takes a 12 bit digital input to produce an analog output voltage. The converter block is composed of 3 sub blocks: scale, buffer, and filter. The output amplifier block is a voltage to current CMOS opamp optimized for high output currents. The block diagram of the proposed system is shown in Fig. 5.1 with the off chip biasing components $R_{bias\,1}$, $R_{bias\,2}$, $R_{bias\,3}$, and V_{bias}.

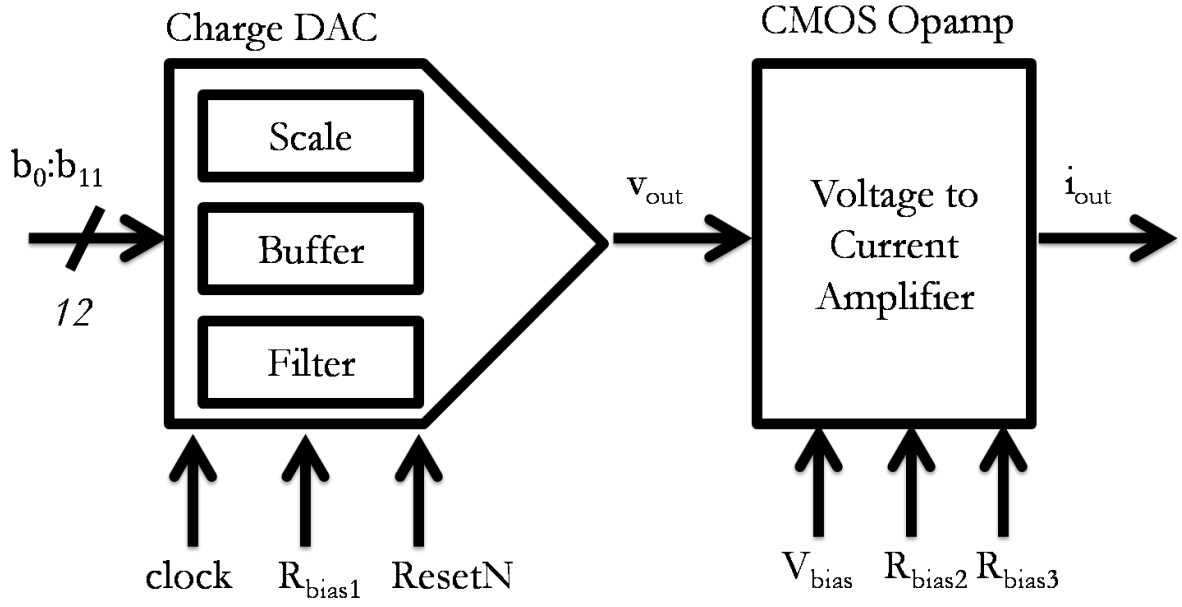


Figure 5.1: Block diagram of proposed data system.

5.1 CHARGE SCALING NETWORK

This is the core of the converter design. The capacitor array was formed with 12 binary weighted capacitors plus an additional terminating capacitor as shown in Fig. 5.2.

A conventional charge DAC uses a pass transistor as the switching element. Albeit functional, a constraint is imposed such that the value of V_{ref} cannot be set equal to V_{DD}. Hence, the circuit designer is faced with a nontrivial task of designing a stable voltage reference. In addition, the reset switch is then sized larger than necessary so that the entire capacitor array can be

completely discharged to ground, but at the same time the large reset switch introduces a higher parasitic junction capacitance.

All of the above problems can be avoided by moving away from analog circuitry and moving into digital circuitry. A Digital CMOS logic gate provides rail to rail operation and is a natural candidate to model a switch that only requires to select between V_{DD} or GND. Figure 5.3 illustrates the proposed switch for the $LSBs$. The switch is a two input CMOS NAND gate cascaded with CMOS inverter with digital input bit b_k and reset input $\bar{R}$. Table 5.1 shows the truth table of the digital switch used. Note that $\bar{R}$ is an active low signal and so the output signal Y depends only on the bit value when the reset is not active (i.e. $\bar{R} = 1$). Transistors $M5$ and $M6$ were sized such that the switch had a sharp response to reduce unwanted glitches at the output.

Table 5.1: Truth table of proposed CMOS switch

b_k	$\bar{R}$	Y
0	0	GND
0	1	GND
1	0	GND
1	1	V_{DD}

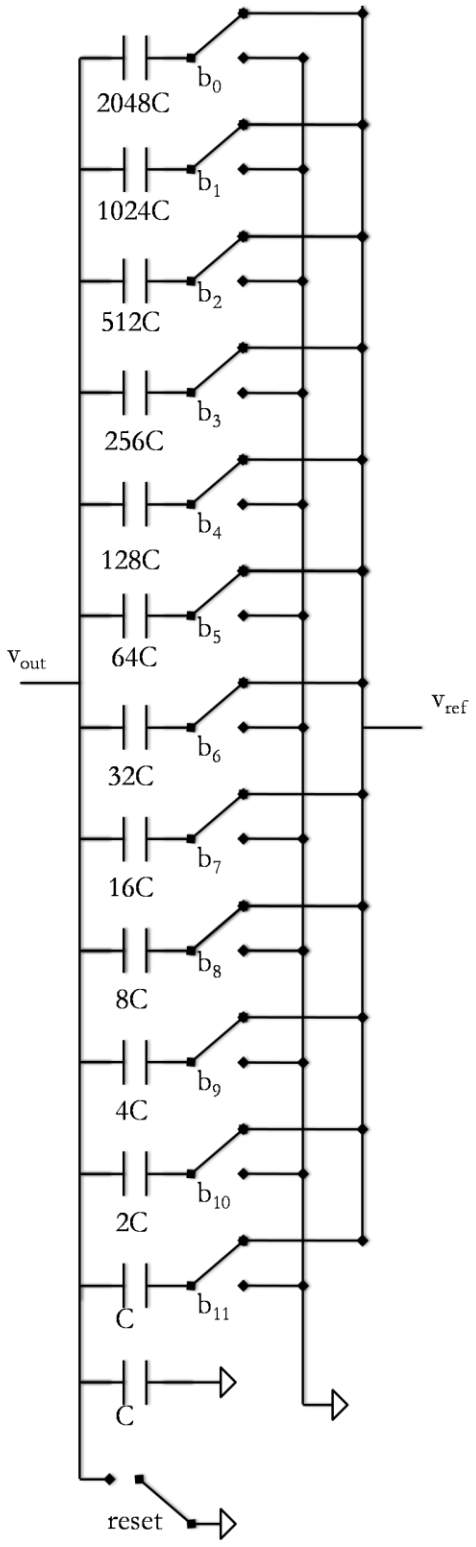


Figure 5.2: Proposed binary weighted capacitor array.

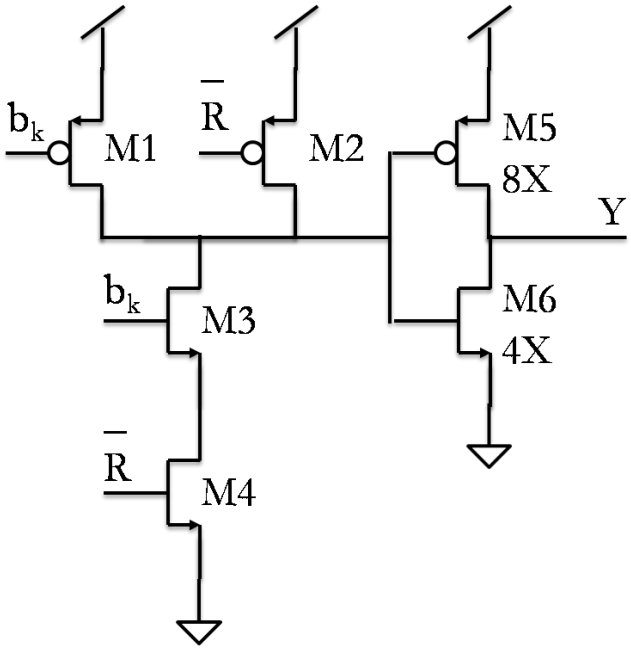


Figure 5.3: Proposed CMOS logic switch for bits $b_4 - b_{11}$.

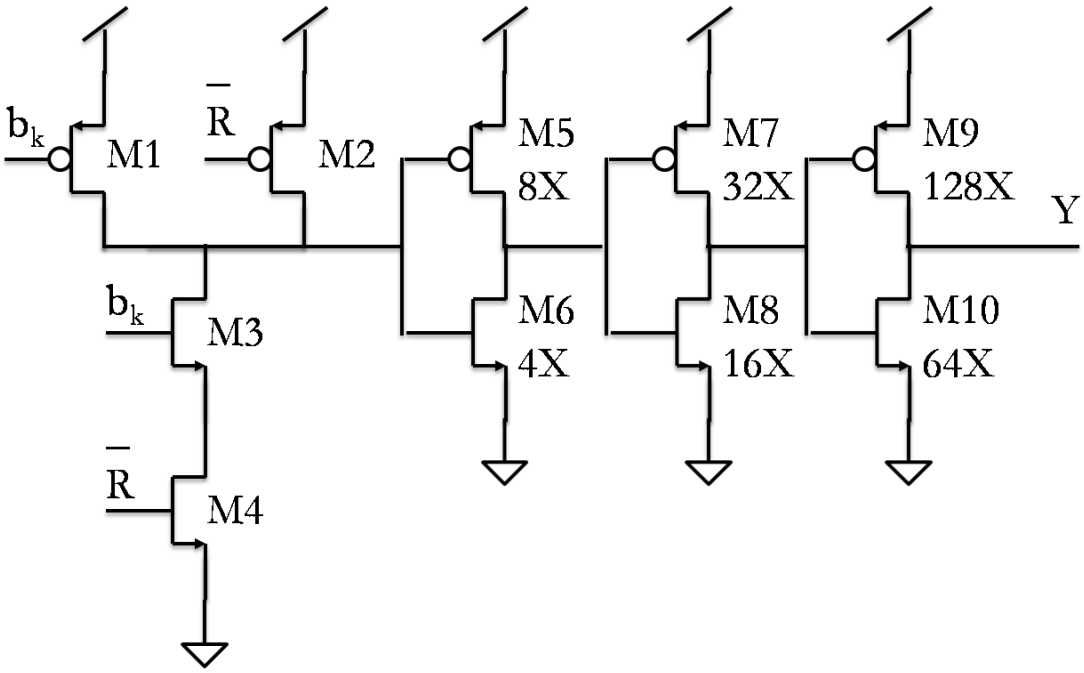


Figure 5.4: Proposed CMOS logic switch for bits $b_0 - b_3$.

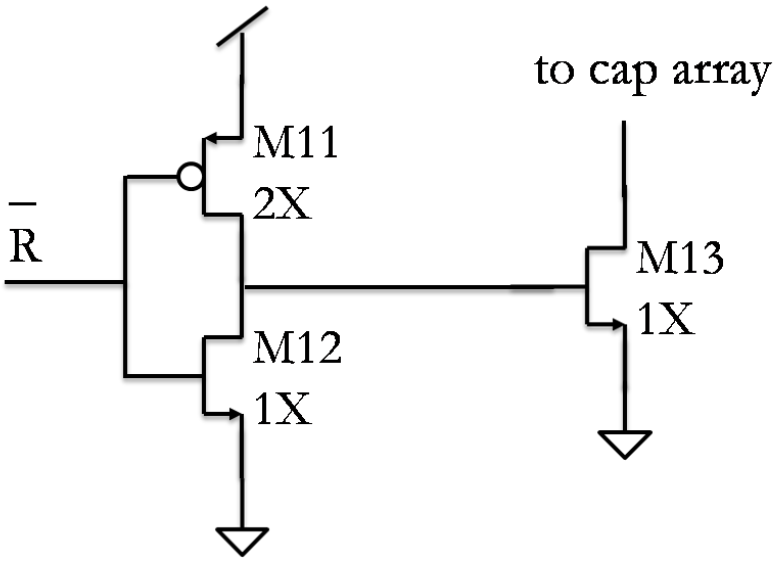


Figure 5.5: Reset switch with low parasitic contribution.

In this architecture only the top third of switches corresponding to bits $b_0 - b_3$ were sized to compensate the delay caused from the large difference in the MSB and the LSB capacitors. This was done by adding transistors $M7 - M10$ as back-to-back inverters forming a strong buffer to charge and discharge the upper capacitors in the same amount of time required for the lower capacitors. In a conventional analog switch the compensation of a large element spread increases the gate capacitance driven by the digital input. Consequently, an additional compensation must be made to prevent race conditions producing large skew and glitch energy.

On the other hand, in the digital switch every bit of the digital input has to drive the same input load capacitance. Therefore, the proposed switching logic greatly reduces skew and glitches at the output. Since the digital switches shown in Fig 5.3 and 5.4 connect the bottom plate of all the capacitors to GND when $\bar{R}$ is asserted, the reset function is faster than with traditional analog switches. This allowed the MOS switch used to discharge the top plate of the capacitors to be sized with a small width to length ratio reducing the nonlinearity effects explained in Section 4.3. This

switch is portrayed in Fig. 5.5. The final sizing of the MSB switch and reset switch are listed in Table 5.2.

Table 5.2: Transistor sizing for the MSB and reset switches.

Transistor	***W***	***L***	**multiplier**
M1	1 μm	400 nm	1
M2	1 μm	400 nm	1
M3	1 μm	400 nm	1
M4	1 μm	400 nm	1
M5	4 μm	400 nm	2
M6	4 μm	400 nm	1
M7	4 μm	400 nm	8
M8	4 μm	400 nm	4
M9	4 μm	400 nm	32
M10	4 μm	400 nm	16
M11	2 μm	400 nm	1
M12	1 μm	400 nm	1
M13	1 μm	400 nm	1

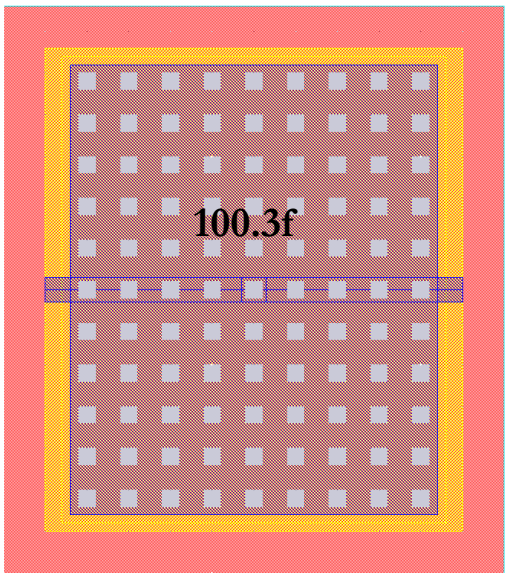


Figure 5.6: PiP unit capacitor used.

A typical layout of a capacitor consists of the overlap of metal-over-metal forming a MiM capacitor. A different approach uses a p or n doped diffusion overlapped with polysilicon to create a linear capacitor $CAPN$ or $CAPP$. Another technique is to use a second polysilicon layer (e.g. electrode) to create a poly-over-poly PiP capacitor. In all of these capacitors, the bigger the area of the overlap, the bigger the capacitance is.

However, a problem arises when two different capacitors must be matched. Irregular gradients and random errors during the fabrication process reduce $ENOB$ if these issues are not addressed properly. In order to minimize the above effect the layout of matched capacitors is done using common centroid geometries. The 0.35μm process from TSMC provides PiP capacitors with a capacitance of 850aF/μm^2. Figure 5.6 illustrates the layout of the unit capacitor used achieving a capacitance of 100.3fF in an area of 12 μm × 14 μm.

The common centroid pattern used for the capacitor array consisted of a matrix built from unit capacitors. The first capacitor C was taken to be the unit capacitor in the center of the matrix, capacitor $2C$ was built from the unit capacitors above and below C, $4C$ was composed of the four

corner capacitors surrounding C, $8C$ was formed by taking the four capacitors closest to the left and right of C. All of these structures have a common centroid which is the center of C. The rest of the capacitors from Fig. 5.2 were built in a similar fashion. This technique results in obtaining binary weighted capacitors regardless of the actual capacitance value of C. Figure 5.6 shows a section of the capacitor array layout used.

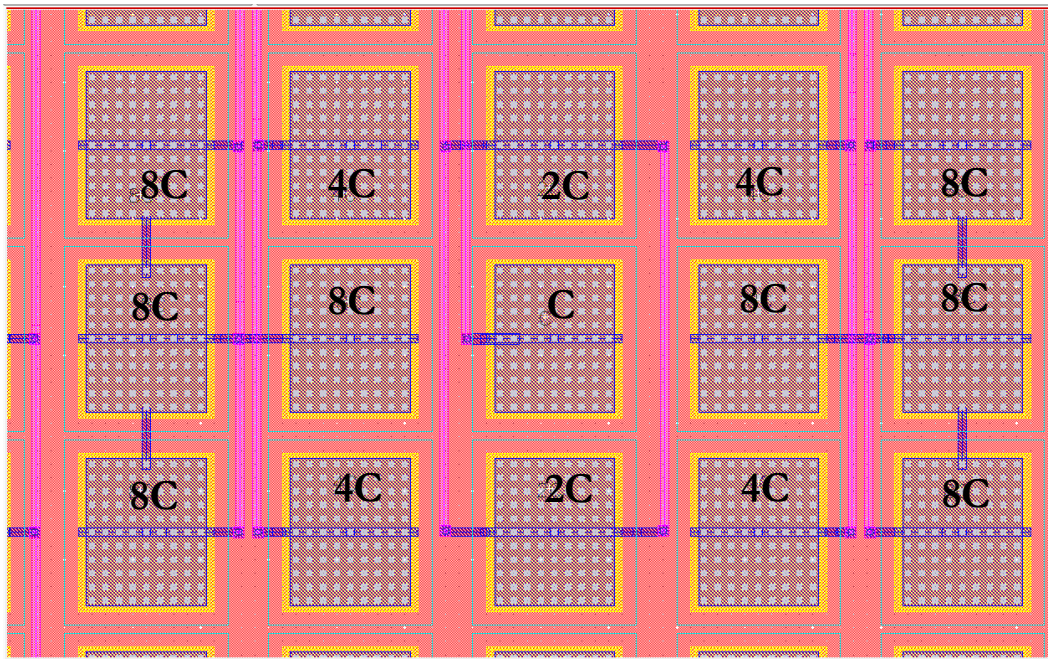


Figure 5.7: Sample section of proposed common centroid capacitor array.

In the layout of Fig.5.7 every capacitor is surrounded by a unit capacitor. However, the outer capacitors forming $2048C$ may not be enclosed. To solve this, a dummy capacitor D was inserted such that every capacitor in the array was bordered by a unit capacitor. The dummy capacitors need not be sized equal to C but need to keep the same spacing between the electrode layers. Figure 5.8 shows the placement of D in one of the corners of the capacitor matrix.

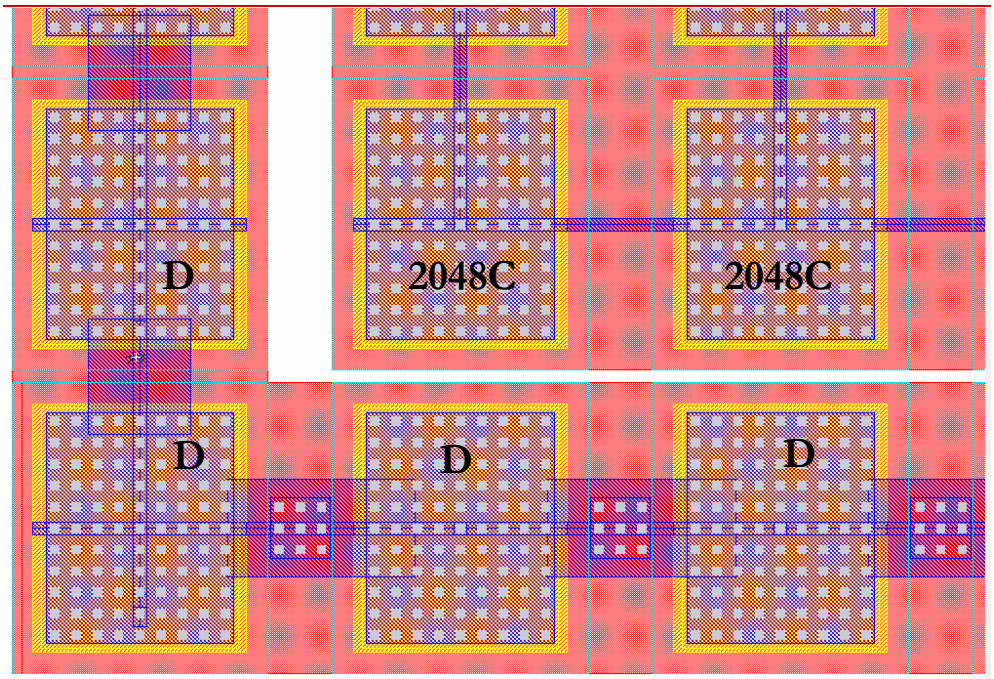


Figure 5.8: Dummy capacitors placed to match 2048C.

5.2 VOLTAGE BUFFER

A voltage buffer was placed to prevent the discharging of the capacitor array by the other blocks of the data system and was implemented as a two-stage unity gain CMOS opamp. This feedback configuration is commonly called a voltage follower. Whenever an opamp is used in a data converter, careful attention is given to the gain bandwidth and slew rate of the amplifier since such parameters will have a negative impact on a DAC.

The two-stage circuit topology consists of a differential input gain stage and a common-source high gain stage hence, the name two-stage amplifier. A third unity-gain (i.e. no gain) stage may be added to drive resistive loads at the expense of a level shift. The biasing network used for an opamp determines the operating range and sensitivity to PVT. Figure 5.9 shows a general block diagram of a two stage opamp. The compensation block is used to maintain stability in feedback configurations.

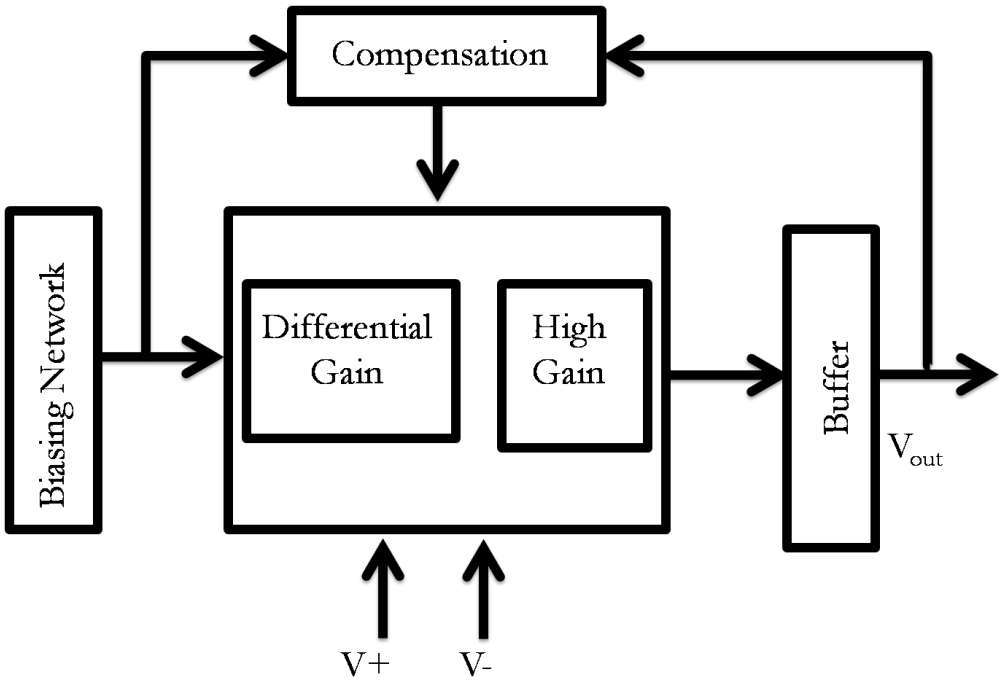


Figure 5.9: General block diagram of two stage opamp.

Transistors $M1 - M3$ from Fig. 5.10 illustrate the pmos differential pair designed with an nmos current mirror active load formed by transistors $M4 - M5$. A pmos input stage as opposed to an nmos input pair was preferred because the slew rate is maximized. Additionally, this decision implies that the second stage be an nmos transistor which results in maximum transconductance. Unwanted poles are correlated to the transconductance of the second stage. So a pmos input pair increases the working unity gain bandwidth. The open loop gain of the first stage is given by

$$\boldsymbol{A_{v1} = g_{m1}(r_{ds2}||r_{ds5})} \tag{5.1}$$

where g_m is the transconductance of a transistor and r_{ds} is the drain to source resistance of a transistor.

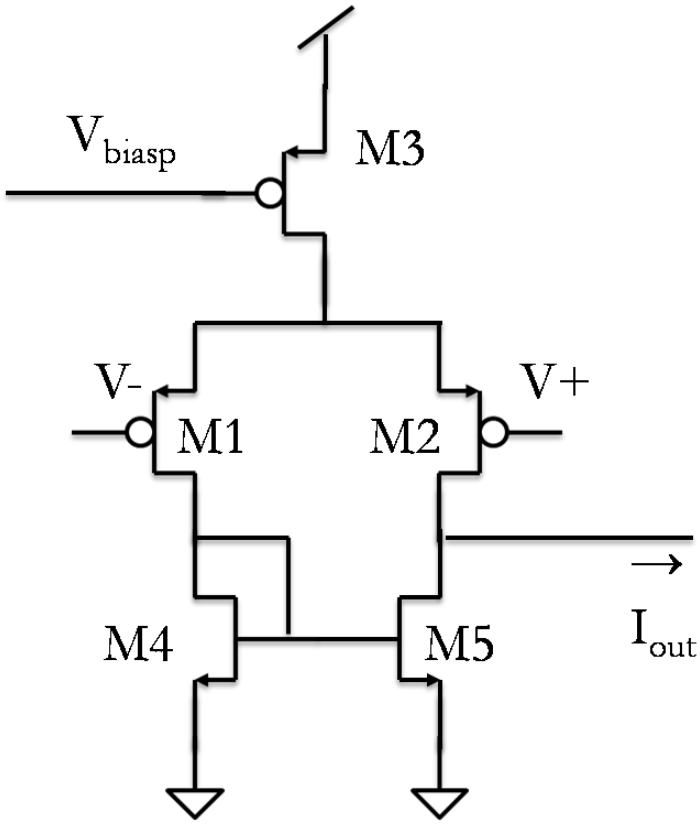


Figure 5.10: Differential amplifier with current mirror load.

The second stage of the opamp is a common source amplifier with a pmos active load, transistors $M13$ and $M12$ form Fig. 5.11. The use of an active load instead of a resistor yields a larger voltage gain at a lower power supply. The open loop gain of the second stage is given by

$$\boldsymbol{A_{v2} = -g_{m13}(r_{ds12}||r_{ds13})} \tag{5.2}$$

The biasing network was designed to tolerate process, voltage, and temperature PVT variations with the purpose of obtaining stable a transconductance. This circuit is shown in Fig. 5.12. Transistor $M6$ and $M7$ form a basic pmos current mirror and transistors $M8 - M11$ form a cascode current mirror with higher output impedance. The cascade structure has retroactive control of the drain to source current of $M6$ therefore; the mirrored current on $M7$ will not depend on the voltage supply. Resistor R_{deg} connected to the source of $M10$ sets a finite limit to the gain of

biasing circuit. This effect is called adding a degeneration resistor because a potential high valued gain that can be harmful to the circuit is degraded. R_{deg} was designed as an off chip component to have a flexible control of the biasing current. Furthermore, R_{deg} can be correlated to the transconductance of $M13$ by

$$\boldsymbol{g_{m13} = \frac{1}{R_{deg}}} \tag{5.3}$$

if and only if the following is true

$$\boldsymbol{\left(\frac{W}{L}\right)_{10} = 4\left(\frac{W}{L}\right)_{11}} \tag{5.4}$$

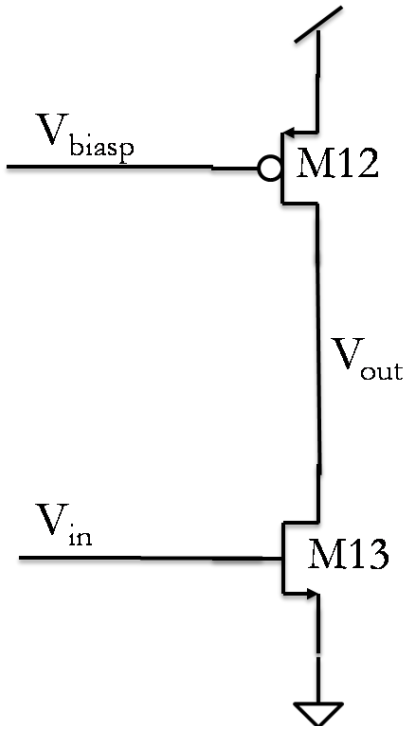


Figure 5.11: Common source amplifier.

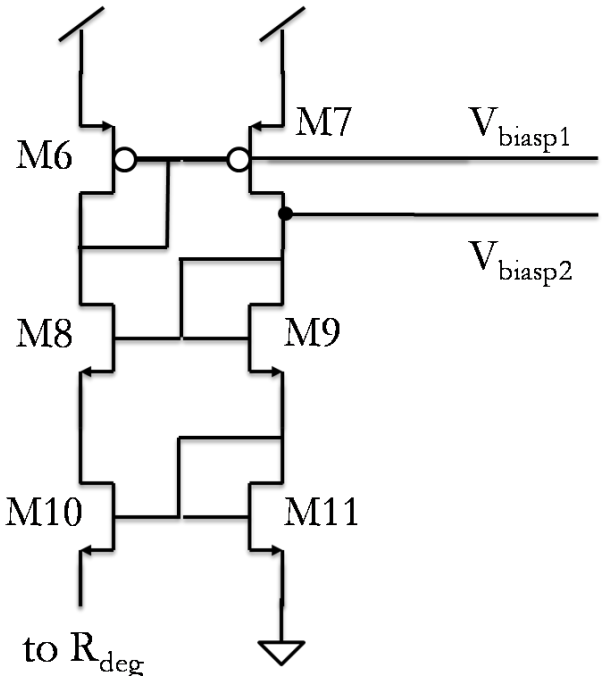


Figure 5.12: Self biasing circuit.

The opamp configuration of a voltage buffer uses negative feedback and requires compensation to avoid unwanted destructive oscillations. The complete circuit of the two stage opamp designed shown in Fig. 5.13 includes two forms of compensation: dominant pole compensation and lead compensation.

Dominant pole compensation was realized with capacitor C connected from the output to the input of the second stage. This technique is also called Miller Compensation. Increasing the value of C moves the dominant pole to a lower frequency but makes the opamp more stable.

Lead compensation was used to introduce a left-half plane zero at frequencies around the unity gain frequency and was implemented by transistor $M14$ which has the gate connected to a cascode of two diode connected nmos transistors $M9$ and $M11$. This arrangement makes the lead compensation independent of process and temperature. Therefore, $M14$ is hard in the triode region

and acts as a linear resistor. The on resistance of $M14$ was chosen large enough to move the left-half plane zero to a frequency slightly greater than the unity gain frequency ω_t satisfying

$$\boldsymbol{r_{on14} = \frac{1}{1.2\omega_t C}} \tag{5.5}$$

Then to size $M14$ as a dynamic resistor the following relationship was used

$$\boldsymbol{r_{on14} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_t)}} \tag{5.6}$$

In [39] the authors show that the necessary condition to ensure that no input-offset voltage is present is to have

$$\boldsymbol{\frac{(W/L)_{13}}{(W/L)_5} = 2\frac{(W/L)_{12}}{(W/L)_3}} \tag{5.7}$$

The final layout of the voltage buffer is found in Fig. 5.14. Each major block was surrounded by guard rings to isolate them from unwanted noise and to prevent latchup. Careful floor planning was necessary to facilitate matching of components. Figure 5.15 shows a better image of the layout of the nmos current mirror and output nmos transistor. Figure 5.16 shows the layout of the pmos current sink and output pmos transistor and Fig. 5.17 shows the layout of the pmos differential pair. In all of the mask designs, dummy transistors were added adjacent to the terminating devices to protect the nearby gate from over etching that may cause a dramatic change in the threshold voltage of the transistor. Table 5.3 lists the transistor sizing used for this opamp.

Furthermore, AC simulations were performed to model the basic characteristics of the opamp: open loop gain, unity gain phase margin, unity gain bandwidth, offset voltage, and slew rate. Figure 5.18 shows the frequency response plots obtained indicated that the opamp has a wide unity gain bandwidth of 15 MHz and a unity gain phase margin of 80º. The summary of these

characteristics is listed in Table 5.4. The simulation load consisted of a 1 MΩ resistor connected in parallel with a 20pF capacitor and setting Resistor $R_{deg} = R_{bias\,1}$ equal to 100 kΩ.

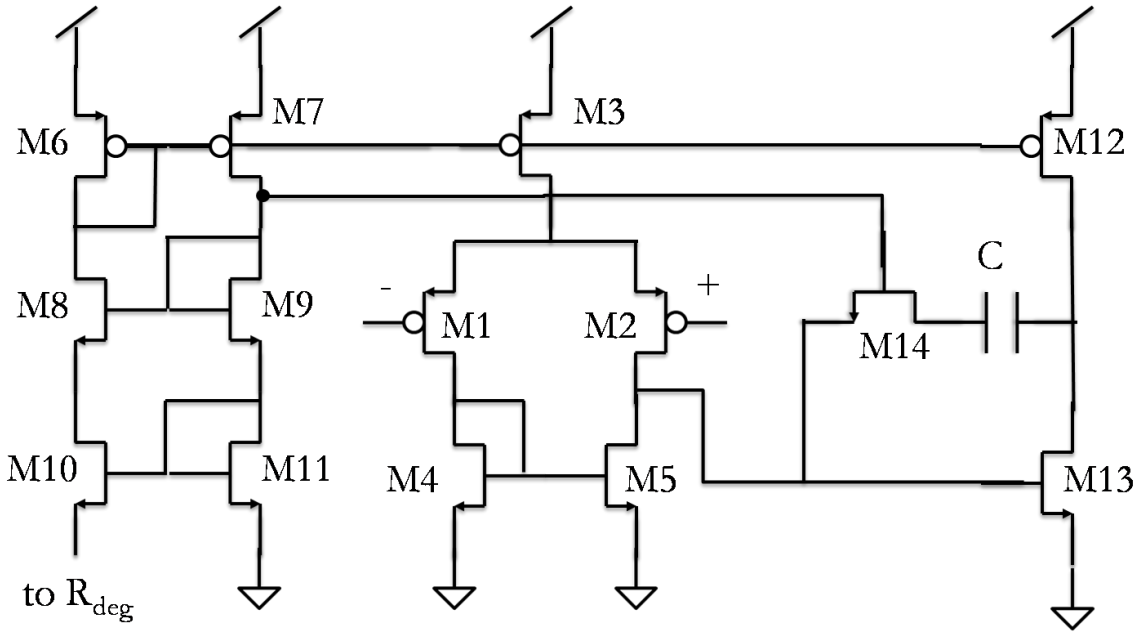


Figure 5.13: Two-stage CMOS opamp with compensation and self biasing circuit.

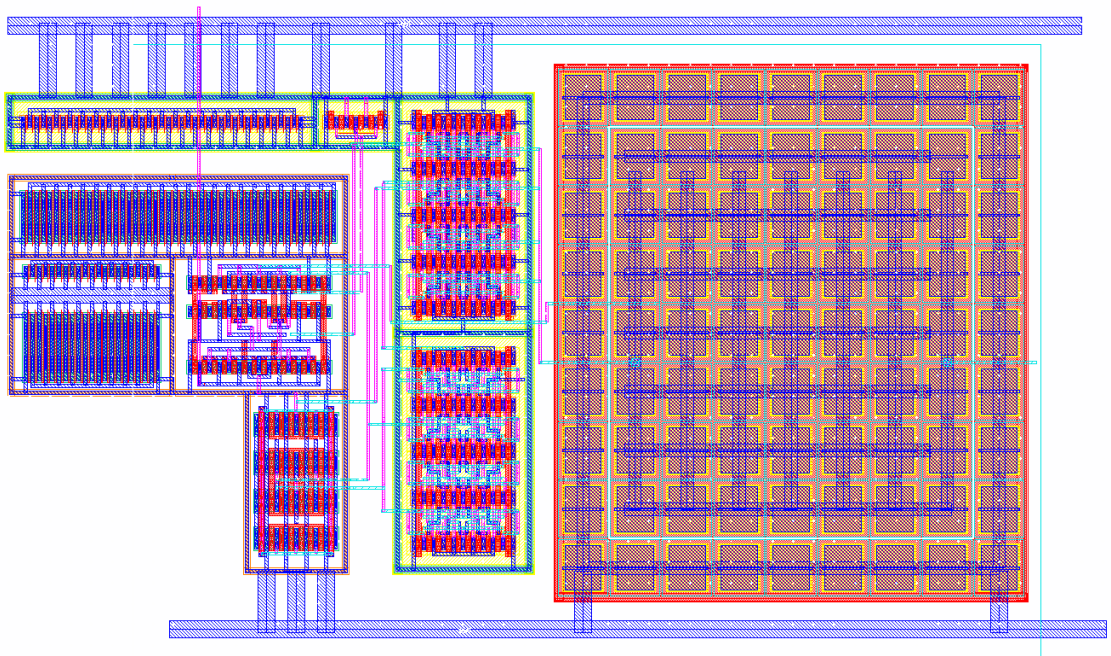


Figure 5.14: Layout of voltage buffer.

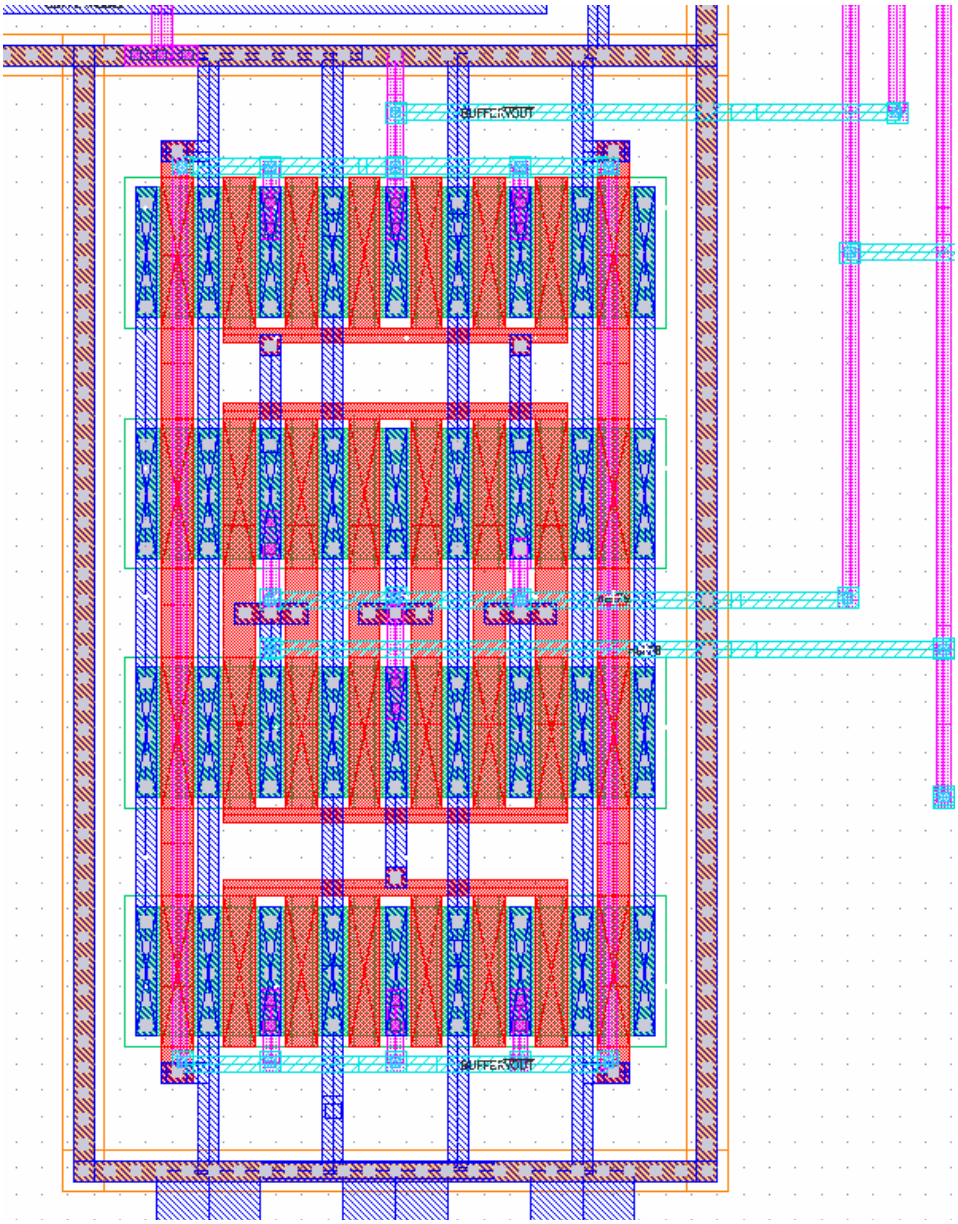


Figure 5.15: Layout of nmos current mirror and output nmos.

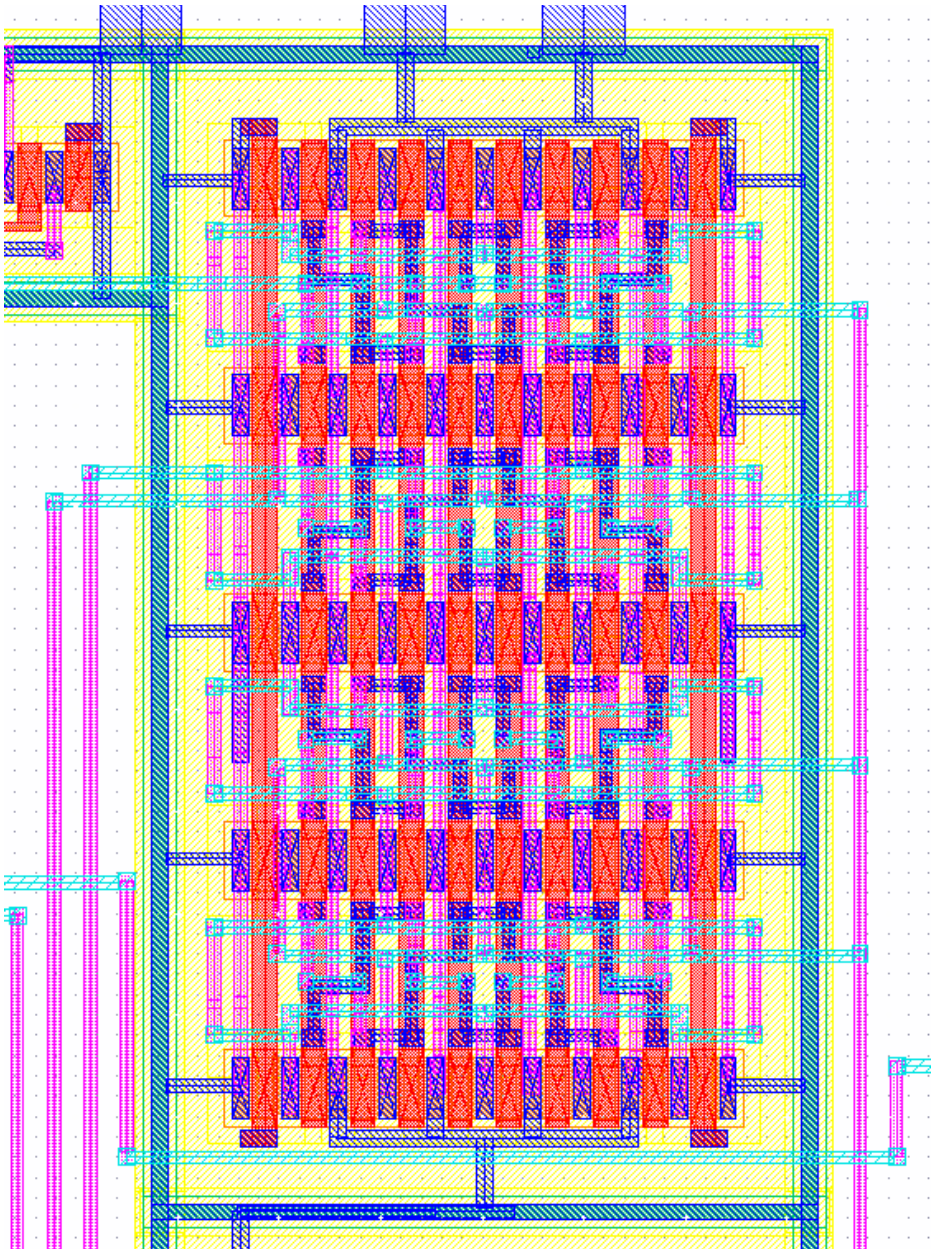


Figure 5.16: Layout of pmos current sink and output pmos.

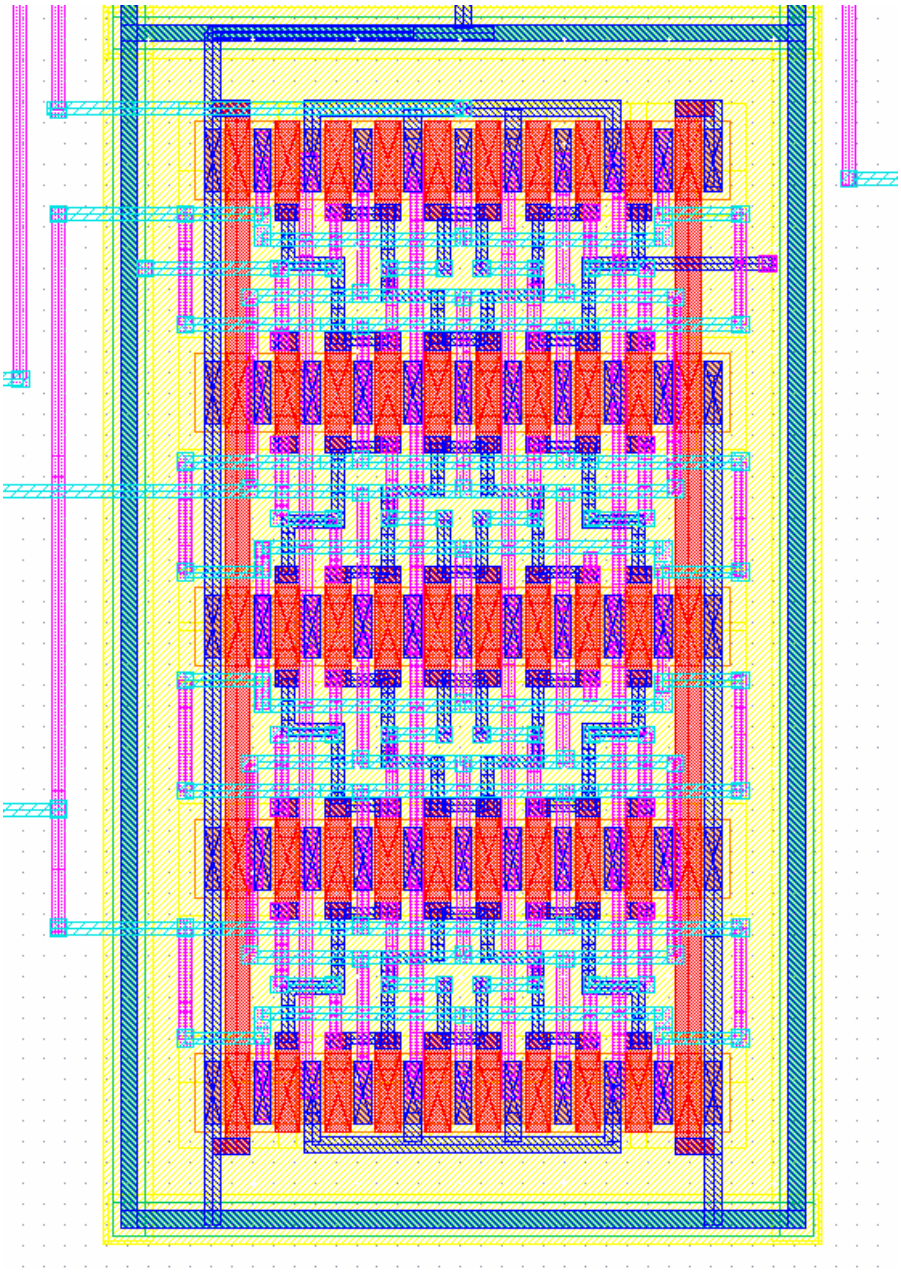


Figure 5.17: Layout of differential pair.

Table 5.3: Transistor sizing of voltage buffer opamp.

Transistor	***W***	***L***	**multiplier**
M1	3 μm	1.2 μm	20
M2	3 μm	1.2 μm	20
M3	3 μm	1.2 μm	20
M4	5 μm	1.2 μm	6
M5	5 μm	1.2 μm	6
M6	2.5 μm	1.2 μm	2
M7	2.5 μm	1.2 μm	2
M8	2.5 μm	1.2 μm	2
M9	2.5 μm	1.2 μm	2
M10	2.5 μm	1.2 μm	8
M11	2.5 μm	1.2 μm	2
M12	3 μm	1.2 μm	20
M13	5 μm	1.2 μm	12
M14	2.5 μm	1.2 μm	8
Capacitor			***value***
C			5 pF

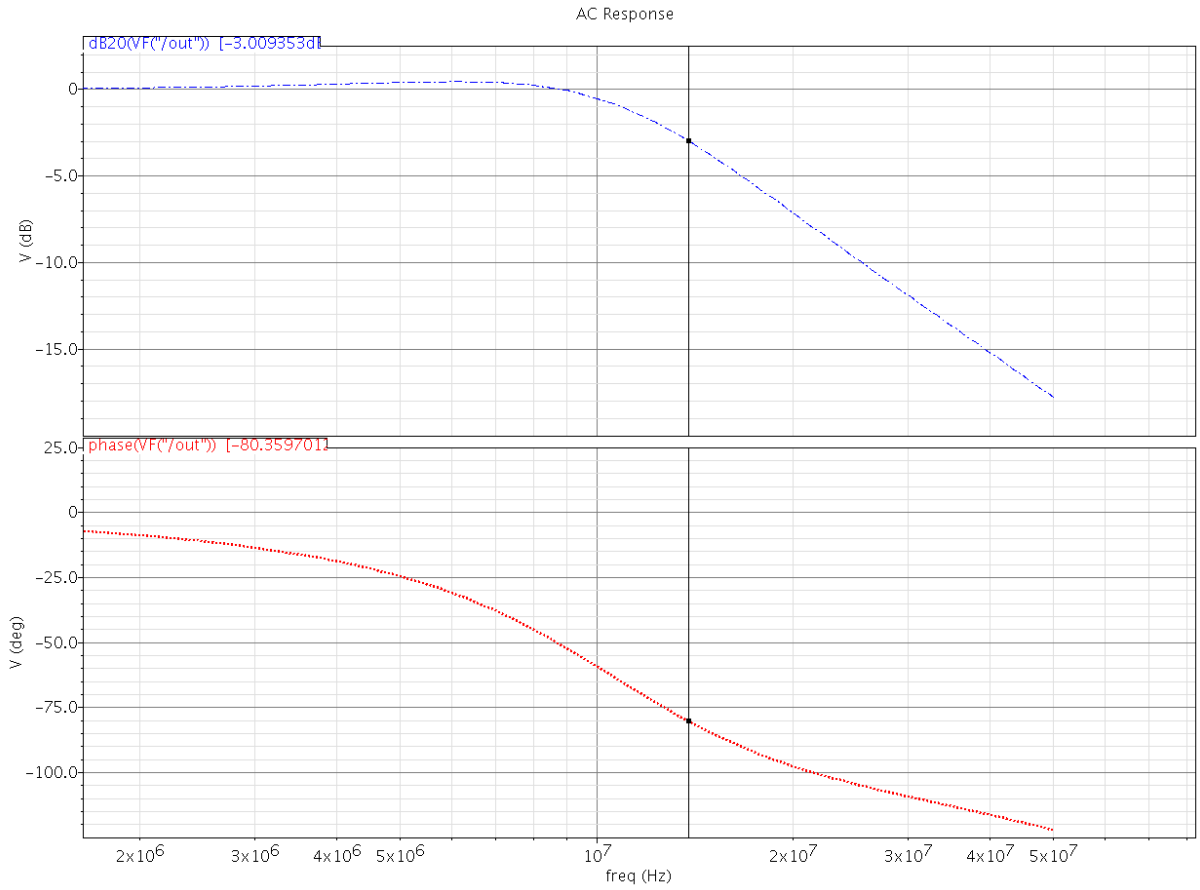


Figure 5.18: Frequency response of voltage buffer.

Table 5.4: Characteristics of voltage buffer opamp.

Parameter	***Value***
Open loop gain	74 dB
Unity gain phase margin	80º
Unity gain bandwidth	15 MHz
Offset voltage	22 mV
Slew rate	3.3 V/μs

5.3 LOW PASS FILTER

The purpose of introducing a filter after voltage buffer was to remove all the glitches caused by imperfect bit transitions from the digital input. A circuit that does exactly this is a sample and hold circuit.

The sample and hold (S/H) circuit shown in Fig. 5.19 uses complementary transistors $M1$ and $M2$ configured as a CMOS transmission gate to track or sample the input signal. Unlike a single pass transistor, the transmission gate has a wide voltage swing and can pass both high and low voltage values, but any noise coming in will also move on. Depending on the control value X the switch will act as either an open circuit or as an active resistor with a resistance equal to the parallel combination of $rds1$ and $rds2$. Consequently, $M1$ and $M2$ were sized to have $rds1 = rds2$. Additionally, the ratio of W/L was kept small to eliminate charge feed through.

In the hold mode, when the switch is in a high impedance state and the input signal has been sampled, the capacitor C_{hold} is used to preserve a constant voltage. The capacitor was made large enough so that leakage currents did not affect the voltage value stored.

The layout of the S/H circuit was dominated by the area of the capacitor. In the layout of the transmission gate shown in Fig. 5.20 dummy transistors were added to prevent over etching of the poly gate. The complete layout of the low pass filter is found in Fig. 5.21. The layout of the 12 bit charge DAC without the output amplifier is shown in Fig. 5.22 occupying an area of 1.2mm × 1.3mm.

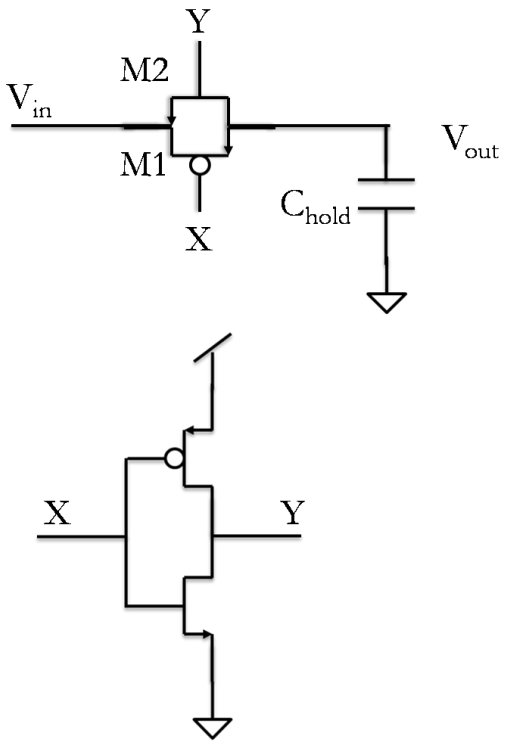


Figure 5.19: Sample and hold circuit.

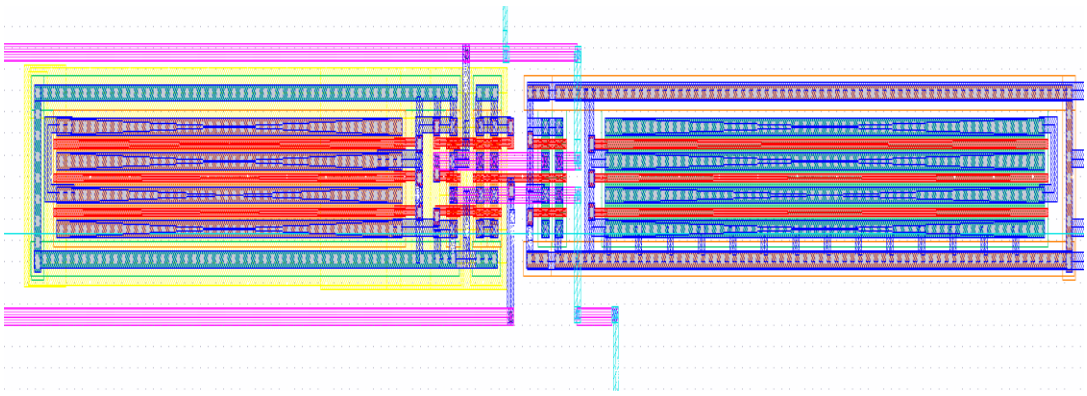


Figure 5.20: Layout of transmission gate switch.

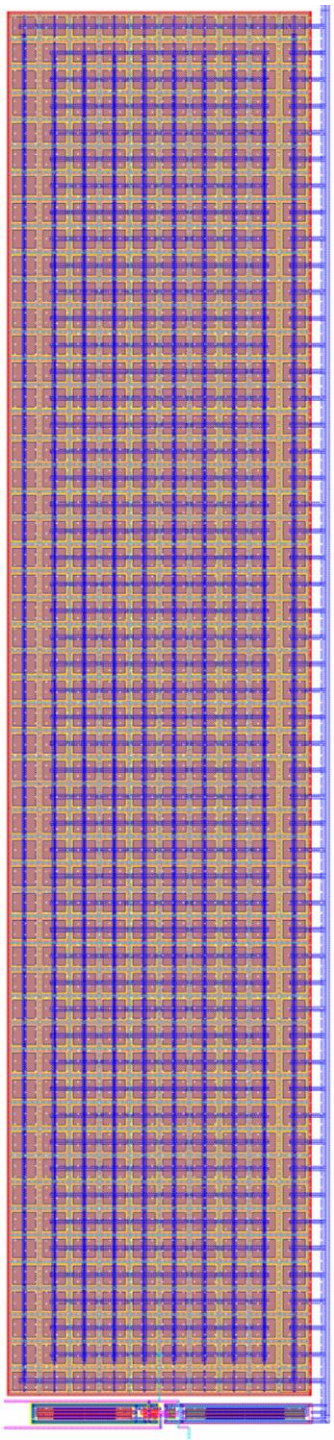


Figure 5.21: Layout of sample and hold circuit

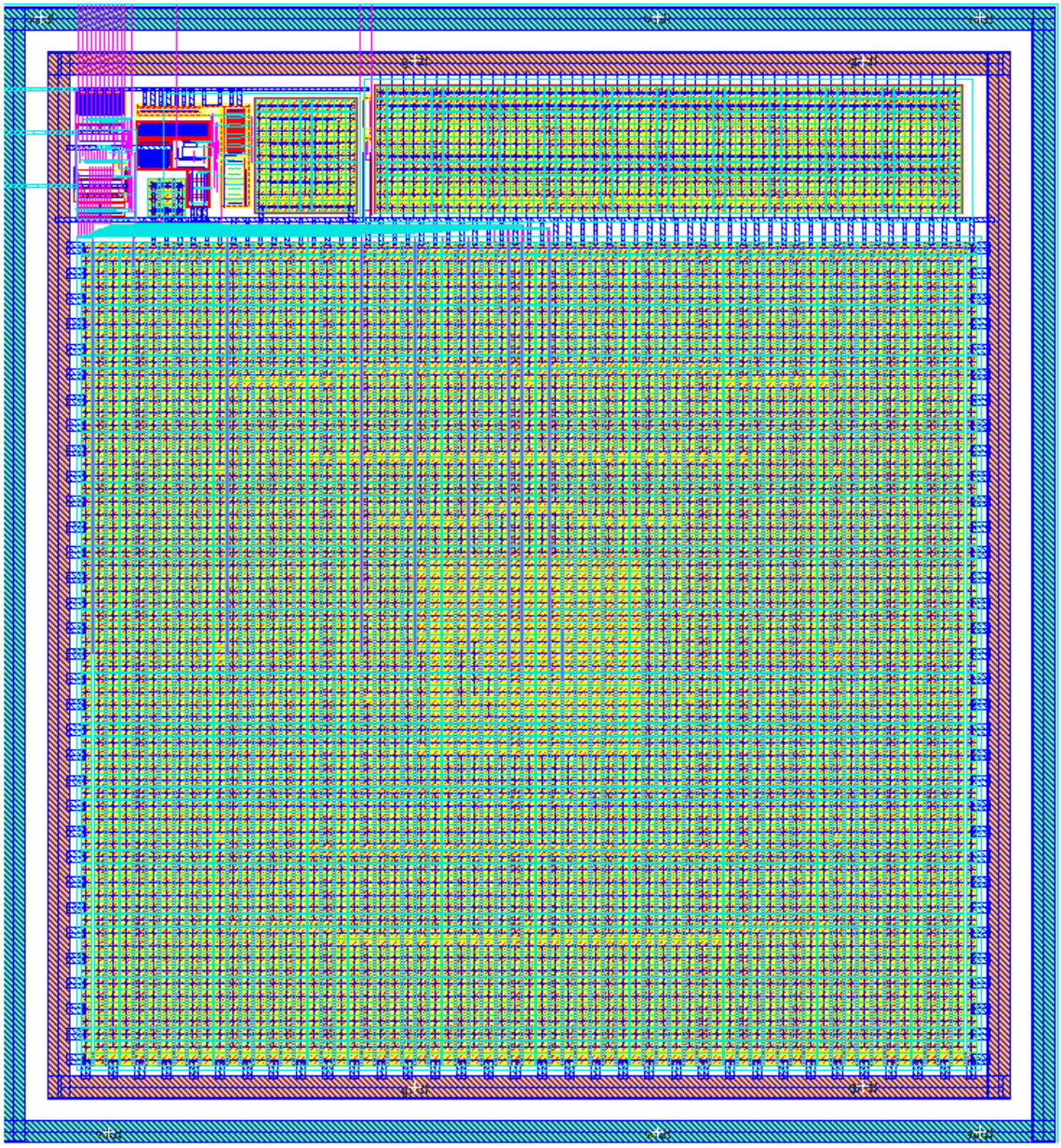


Figure 5.22: Layout of 12 bit charge DAC

5.4 VOLTAGE TO CURRENT OUTPUT AMPLIFIER

The final step to achieve a current output charge DAC was to send the output signal from the filter to a voltage to current converter. A CMOS opamp configured as a transconductance amplifier was selected to carry out this process.

The ideal transconductance amplifier has infinite input and output impedance. This condition is not realizable, but can be approximated with a negative feedback network. Negative series feedback increases input impedance and negative current feedback increases output impedance. The feedback amplifier shown in Fig. 5.23 uses the RTD fluxgate modeled by a load resistance R_L and R_{bias3} to produce a feedback current I_f. An additional voltage source V_{bias} was added to the feedback network to have a bipolar output signal. V_{bias} is essentially a negative DC offset to the output current i_{out}. To find an expression for i_{out}, first recall from Fig. 5.13 that the inverting terminal of the opamp is a pmos gate so the current flowing into this node is zero if leakage currents are ignored and that voltage at both the inverting and non-inverting terminals are made equal since the same drain to source current is forced by the current mirror load. From the above, the output current is

$$\boldsymbol{i_{out} = \frac{v_{out} - v_{in}}{R_L}} \tag{5.8}$$

The above expression is ambiguous because the output voltage is a function of the input voltage. However, the output current can also be expressed in terms of the input voltage as

$$\boldsymbol{i_{out} = \frac{v_{in} - V_{bias}}{R_{bias3}}} \tag{5.9}$$

Equation 5.8 shows that the output current will be constant regardless of the value of the load, an ideal condition for a current source. Nonetheless, R_L has an impact on the permissible input voltage swing. Combining Eq. 5.8 and 5.9 to solve for v_{in} yields

$$v_{in} = \frac{R_{bias3} v_{out} + V_{bias} R_L}{R_L + R_{bias3}} \tag{5.10}$$

Clearly the output voltage is bounded by

$$GND \leq v_{out} \leq V_{DD} \tag{5.11}$$

Taking the maximum and minimum values for v_{out}, the limits of vin can be expressed as

$$GND < \frac{V_{bias} R_L}{R_L + R_{bias3}} \leq v_{in} \leq \frac{R_{bias3} V_{DD} + V_{bias} R_L}{R_L + R_{bias3}} < V_{DD} \tag{5.12}$$

Therefore the input voltage need not be rail-to-rail.

The layout of the output amplifier occupies a chip area of 480 μm × 450 μm and is shown in Fig. 5.24. As in the layout of the voltage buffer, common centroid techniques were used to match the differential pairs and all current mirrors. Additionally, several interconnect traces were designed with widths many times that of the minimum design rule to bear the high current drawn for the load. For the 0.35 μm process from TSMC the current density for the first layer of metal is rated at 1 mA/μm. So if a metal trace was expected to carry a current of 5 mA, the connecting wire was drawn with a width of 5μm plus a ten percent overhead.

In addition, the AC characteristics of the output amplifier were extracted by simulating the opamp configured as: open loop and closed loop (e.g. unity gain). A transient simulation with a half scale step signal as the input was also performed to extract parameters like slew rate and offset voltage. Figure 5.25 shows the frequency response plots obtained, indicating that the output opamp has a wide unity gain bandwidth of 400 MHz and a unity gain phase margin of 88º. The summary of these characteristics is listed in Table 5.5 and Table 5.6 lists the sizing of transistors used. The simulation load consisted of a 1MΩ resistor connected in parallel with a 20 pF capacitor and Resistor $R_{deg} = R_{bias\,2}$ was set to 200 Ω.

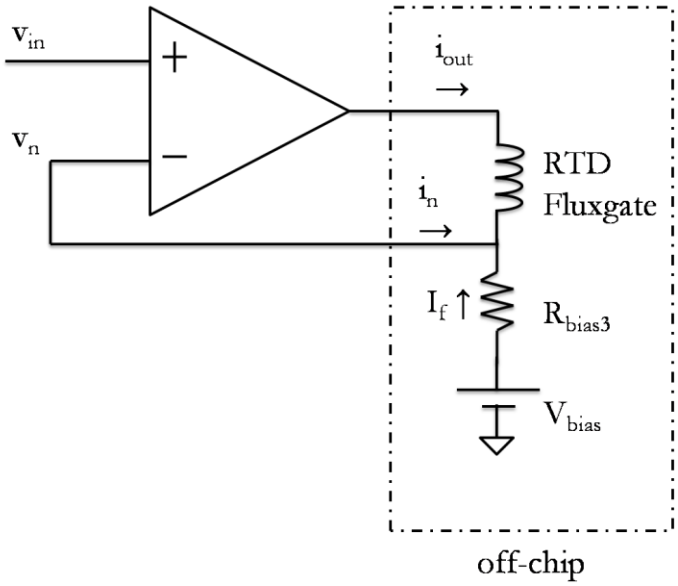


Figure 5.23: Output amplifier with off-chip components.

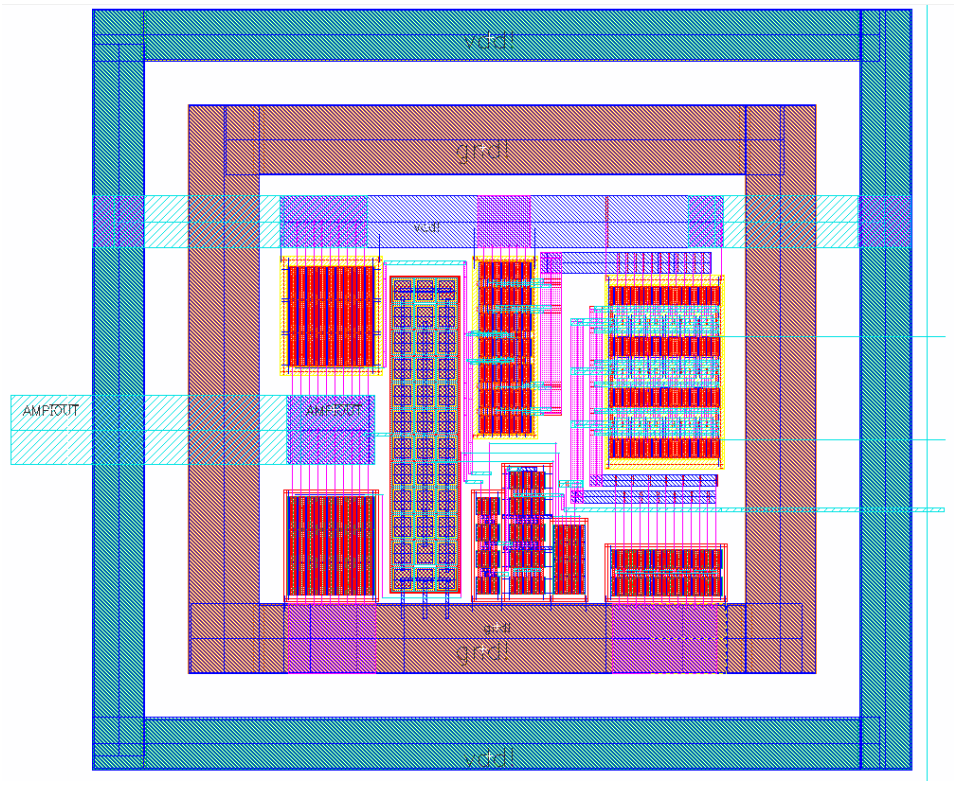


Figure 5.24: Layout of output amplifier

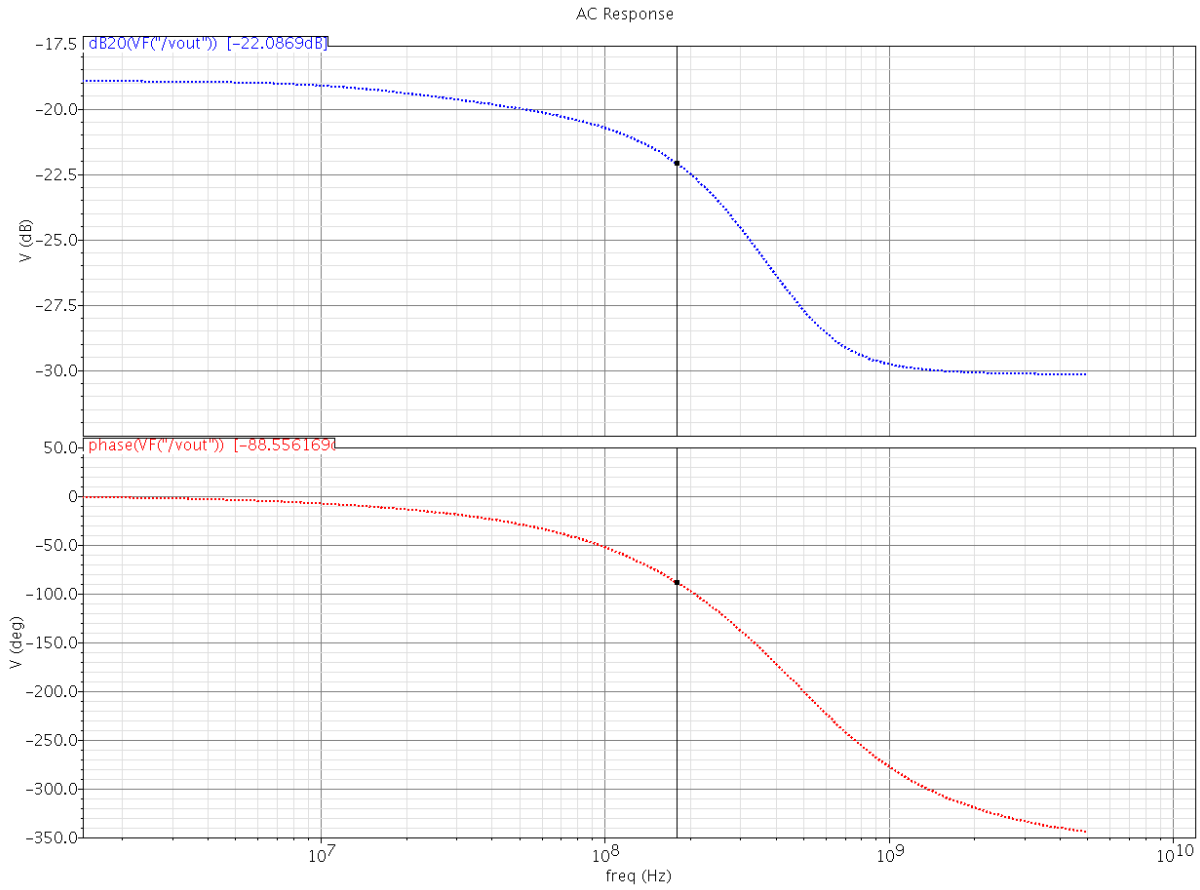


Figure 5.24: Layout of output amplifier

Table 5.5: Characteristics of output amplifier

Parameter	***Value***
Open loop gain	48 dB
Unity gain phase margin	88º
Unity gain bandwidth	400 MHz
Offset voltage	165 mV
Slew rate	650 V/µs

Table 5.6: Transistor sizing of voltage to current opamp.

Transistor	***W***	***L***	**multiplier**
M1	9.8 μm	1.2 μm	48
M2	9.8 μm	1.2 μm	48
M3	9.0 μm	1.2 μm	52
M4	9.8 μm	1.2 μm	24
M5	9.8 μm	1.2 μm	24
M6	9.0 μm	1.2 μm	6
M7	9.0 μm	1.2 μm	6
M8	9.0 μm	1.2 μm	6
M9	9.0 μm	1.2 μm	6
M10	9.0 μm	1.2 μm	24
M11	9.0 μm	1.2 μm	6
M12	18 μm	1.2 μm	54
M13	18 μm	1.2 μm	154
M14	9.0 μm	1.2 μm	20
Capacitor			***value***
C			1 pF

Chapter 6: Design Verification

Before any serious circuit design is sent to fabrication extensive verification is performed to guarantee proper operation under worst case scenarios. Circuit simulation was done at the transistor level using SPICE models. These models or cards as referenced in the past due to the original storage form include many parameters that are used to solve the nonlinear differential equations describing the primitive components: transistor, resistor, capacitor, and energy source.

Results from simulations are only as good as the model used. The Shichman-Hodges model describing the typical quadratic equation for the drain to source current is a Level 1 model and has low accuracy for short channel designs (e.g. < 1 μm). The bsim3v3 level 49 model developed originally at Berkeley stands as the standard model card used by circuit designers.

5.1 Electronic Design Automation

The Front-to-Back End design was done with Cadence's Custom IC platform. Cadence provides sophisticated tools to the digital, analog, and mixed-signal designer. Design entry was done with Virtuoso Schematic Editor. The inclusion of bindkeys made way for a fast and flexible environment. Block-level and Chip-level simulations were performed with Virtuoso Spectre Circuit Simulator. This simulator was able to interpret SPICE netlists as well as verilogA netlists. Physical implementation was made at the symbolic level with Virtuoso Layout Suite. Bindkeys were again a valuable resource to speed up a mask design as well as SKILL scripts. Parasitic extraction was completed with Diva. Following extraction, the simulations were repeated with the inclusion of parasitic resistors and parasitic capacitors. Ocean scripts were used to speed up the analysis and to generate ASCII data files. The text files were the loaded in MATLAB for post-processing to characterize the behavior of the circuits designed.

5.2 Simulation Results

In order to simulate a circuit a test bench schematic was designed with input stimuli and output loads. Buffers were used to achieve realistic rise and fall times unlike the ones obtained from ideal sources. Figure 6.1 shows the test bench used to simulate the 12 bit charge DAC and characterize the static and dynamic parameters.

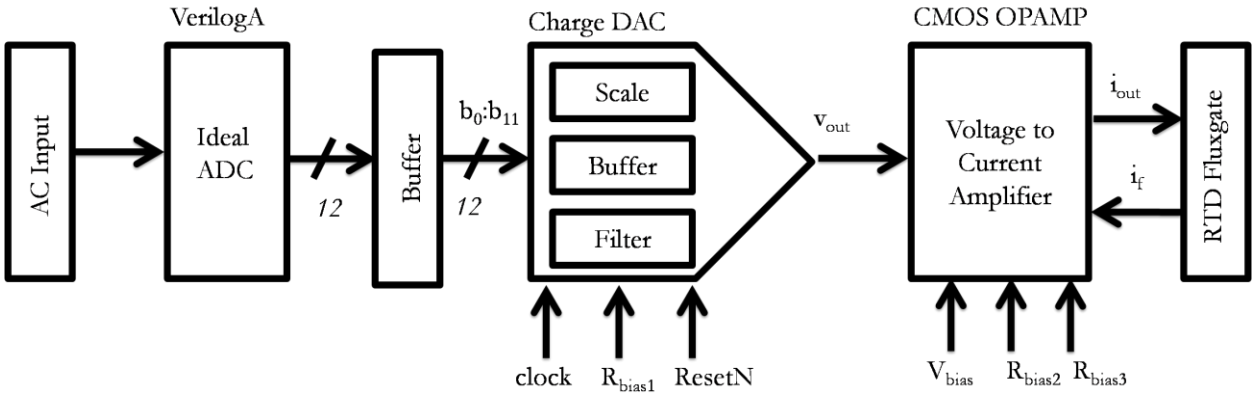


Figure 6.1: Block diagram of simulation test bench.

The setup shown in Fig. 6.1 includes an ideal 12 bit ADC. This element was designed in VerilogA, a behavioral language describing hardware components for analog and mixed signal systems. The value of the off-chip components used in the simulation are listed in Table 6.1

Table 6.1: Summary of off-chip components.

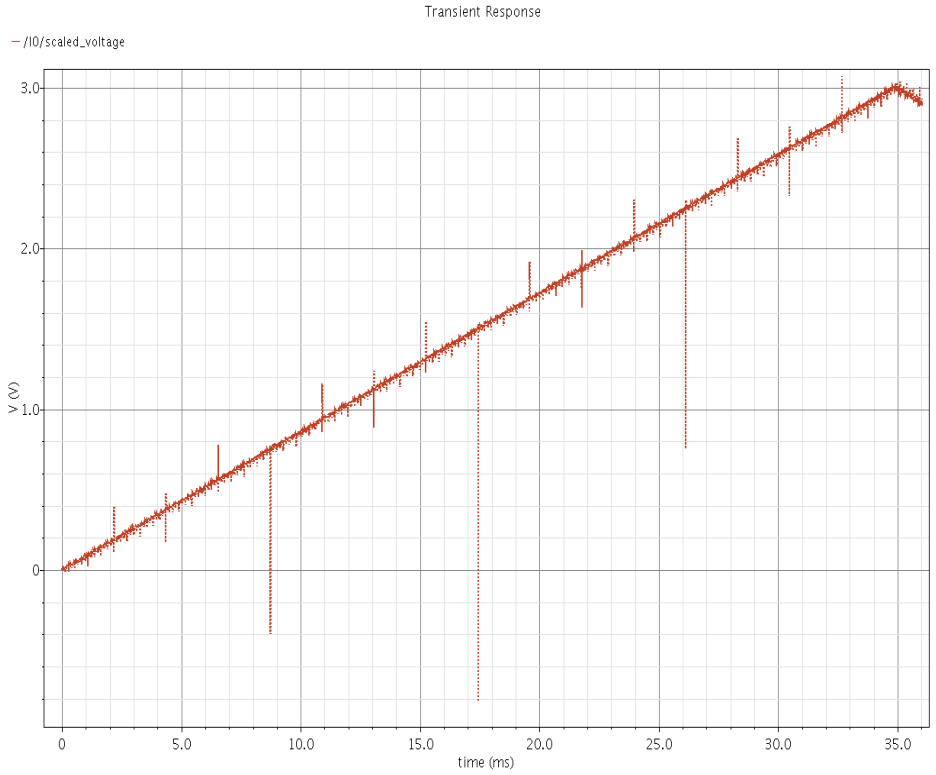
Compoent	***Value***
$R_{bias\,1}$	10 kΩ
$R_{bias\,2}$	200 Ω
$R_{bias\,3}$	60 Ω
V_{bias}	1.5 V
V_{dd}	3.0 V

The input-output characteristic was acquired by sending an increasing full-scale ramp signal to the ADC and measuring the transient output signal of the DAC. Figure 6.2 shows the post-layout data obtained at the four points of interest: capacitor array, voltage buffer, low pass filter, and voltage to current amplifier. In Fig. 6.2 (a) a linear signal with a 3 V swing and noticeable glitches is shown. In Fig. 6.2 (b) the voltage buffer with negative feedback has reduced some of the noise, but has also reduced the voltage swing because negative values cannot be resolved. In Fig. 6.2 (c) the sample and hold circuit has eliminated unwanted frequencies and no glitches are visible. In Fig. 6.2 (d) the bipolar output current changes linearly in the voltage range specified by Eq. (5.11).

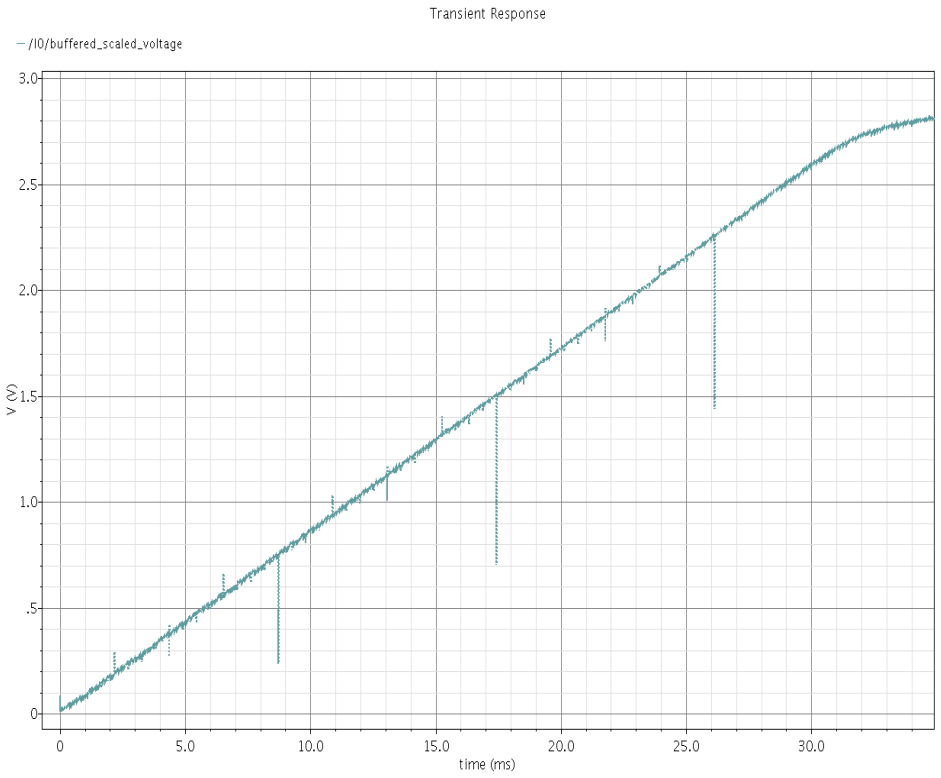
The Spectre Circuit Simulator offers a set of automated mathematical functions to post process the computer-generated signals. However, the included algorithms are hard coded and may be different to what the designer needs to correctly analyze the circuit's behavior. On the other hand, MATLAB offers more flexibility and more computing-performance to complete data analysis. Different algorithms were written in a MATLAB script file to calculate the static parameters of Table 6.2. The offset and full-scale errors were measured at the linear endpoints of the input-output characteristic. The gain was calculated with Eq. (3.11) and DNL with Eq. (3.12). The relative integral nonlinearity was obtained by using a best-fit line to compensate for E_{offset} and E_{gain}. The above analysis was performed for all the DAC sub blocks as well as for the output amplifier. Figure 6.3, 6.4, 6.5 and 6.6 show the static behavior obtained for the scale, buffer, filter, and amplifier blocks respectively in units of LSB.

Table 6.2: Simulated DAC static parameters.

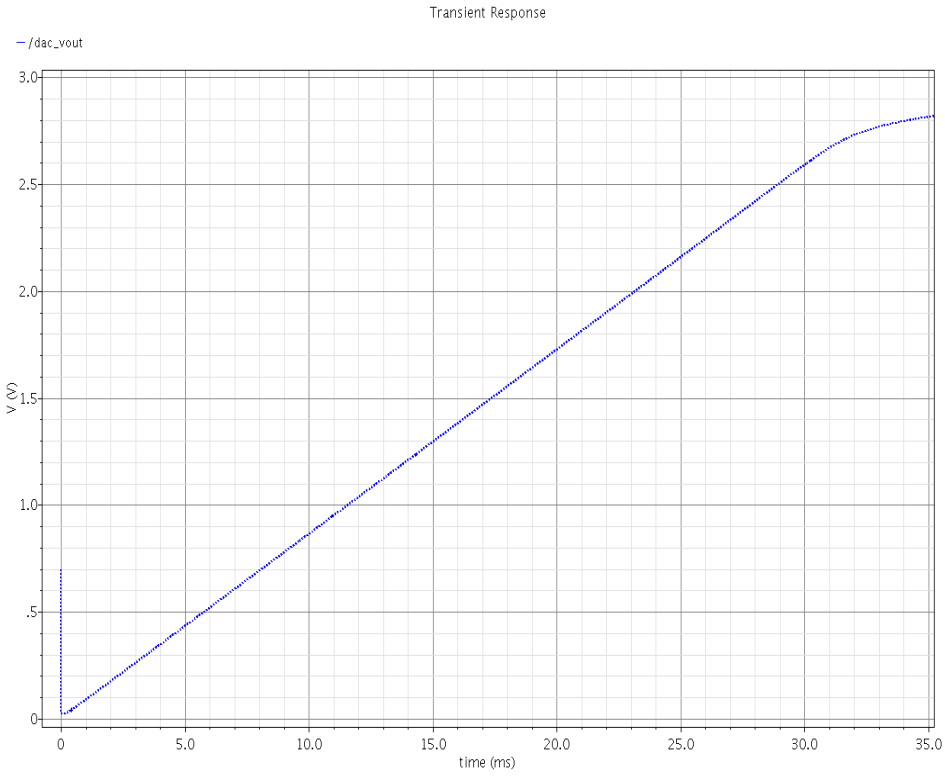
Block	E_{offet}	$E_{full-scale}$	E_{gain}	DNL_{max}	INL_{max}
Scale	1.36	-733	-731	±0.8	±1
Buffer	31.2	-729	-698	±1	±2
Filter	31.2	-729	-698	±1	±2
Amplifier	744	-1016	-271	±0.5	±2



(a) Output signal after capacitor array.



(b) Output signal after voltage buffer.



(c) Output signal after filter.

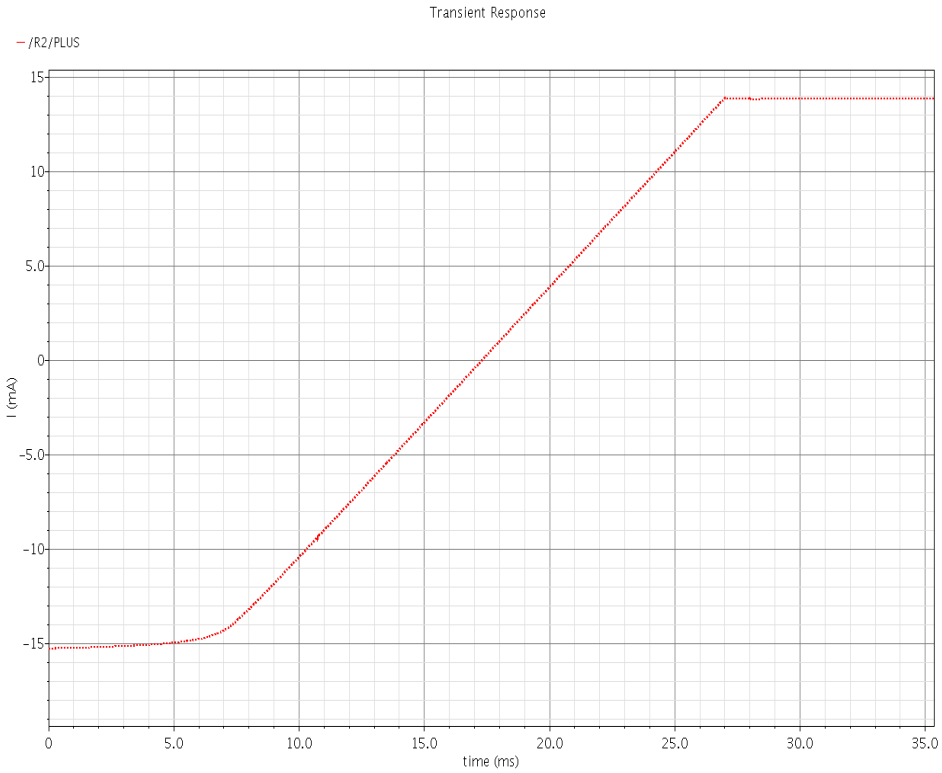
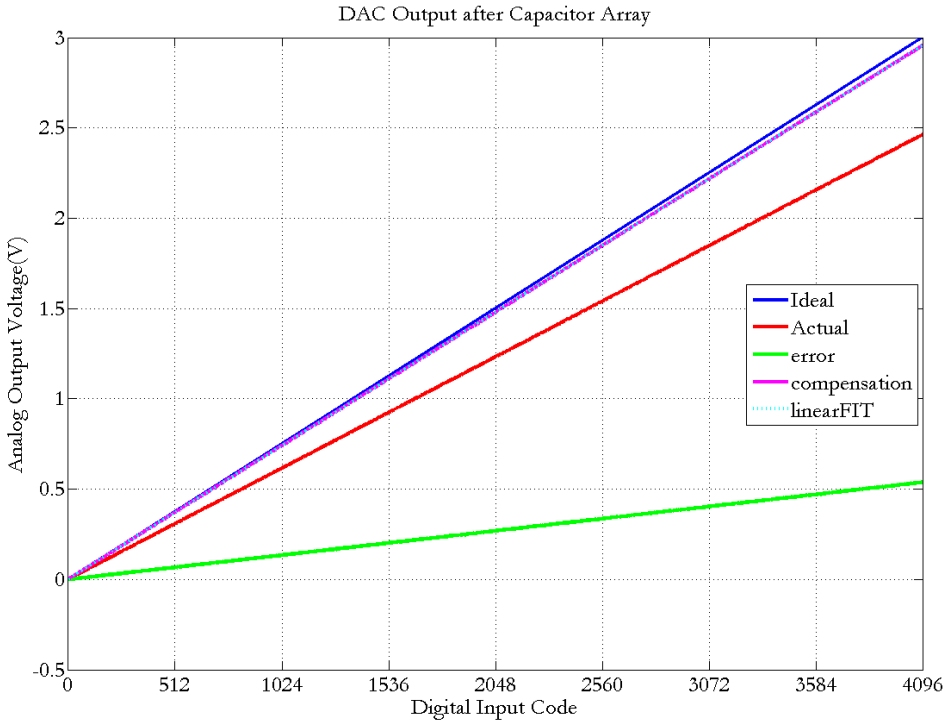
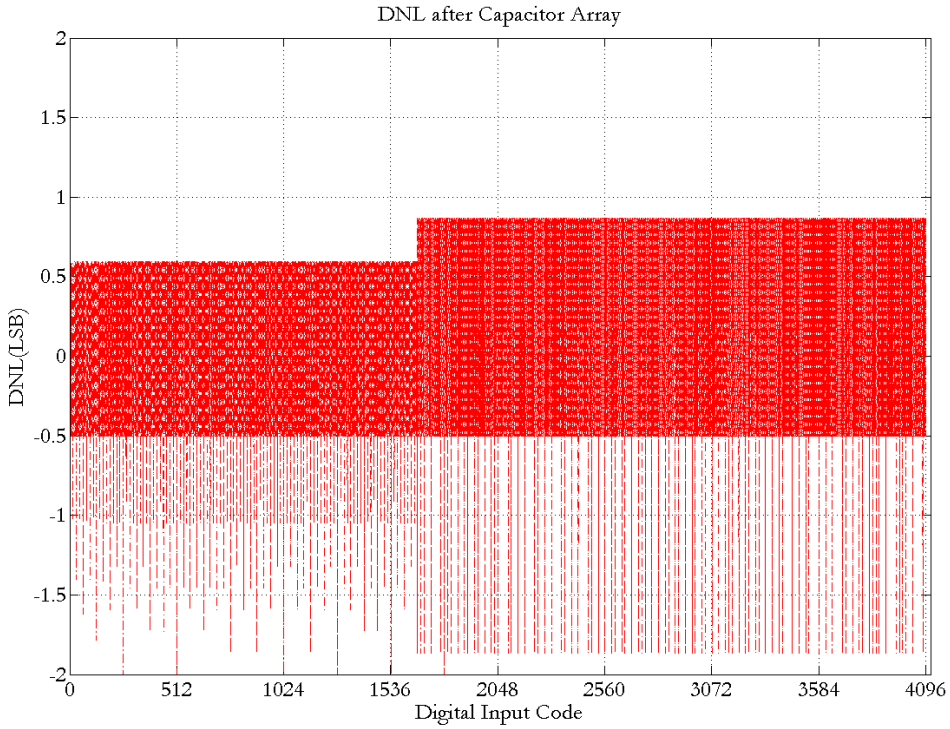


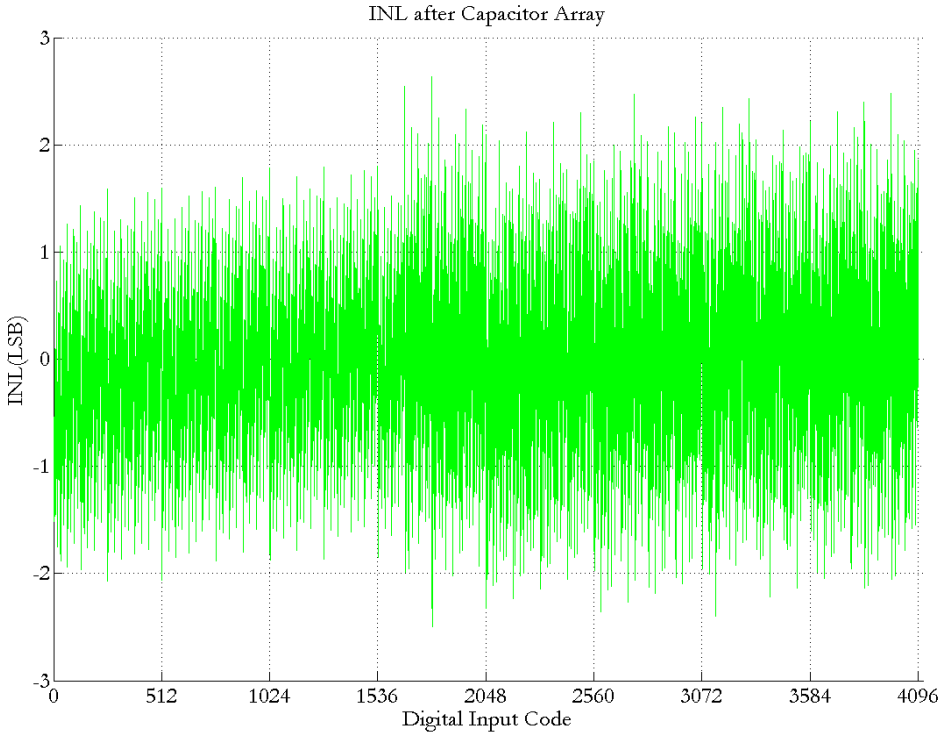
Figure 6.2: Simulated linear response of designed DAC.



(a) Ideal and actual response.

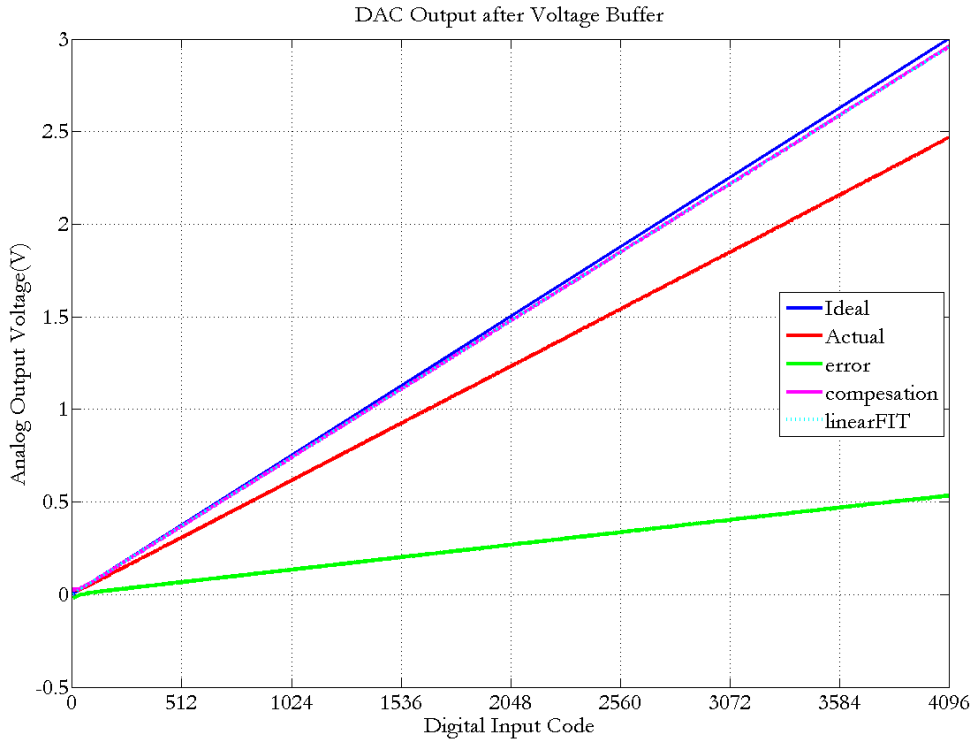


(b) DNL

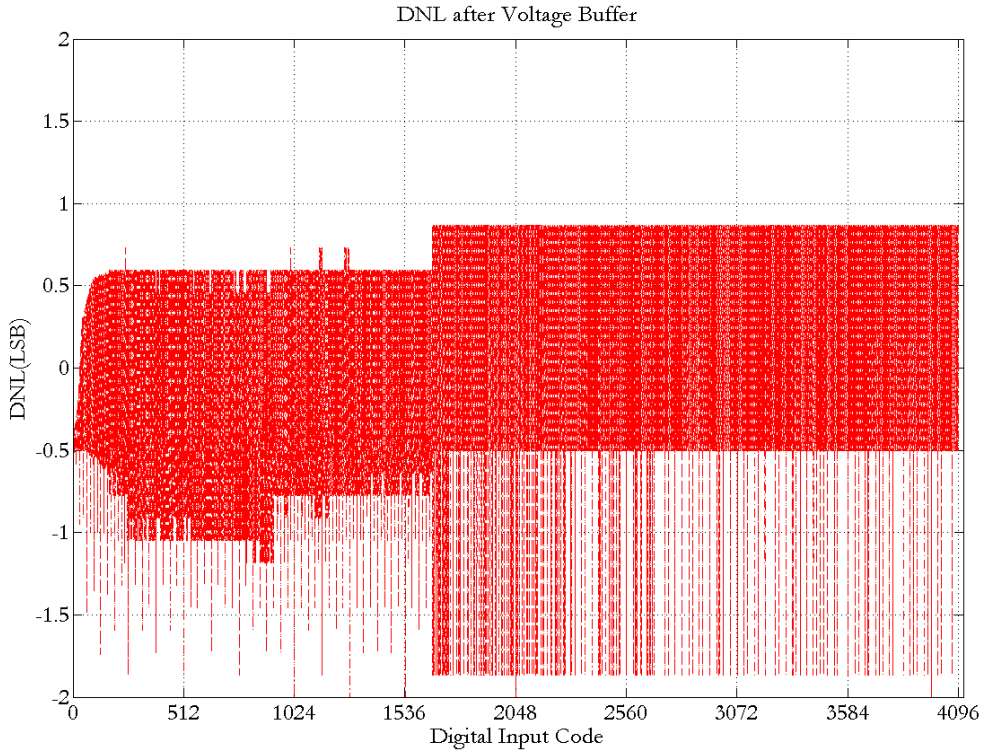


(c) INL

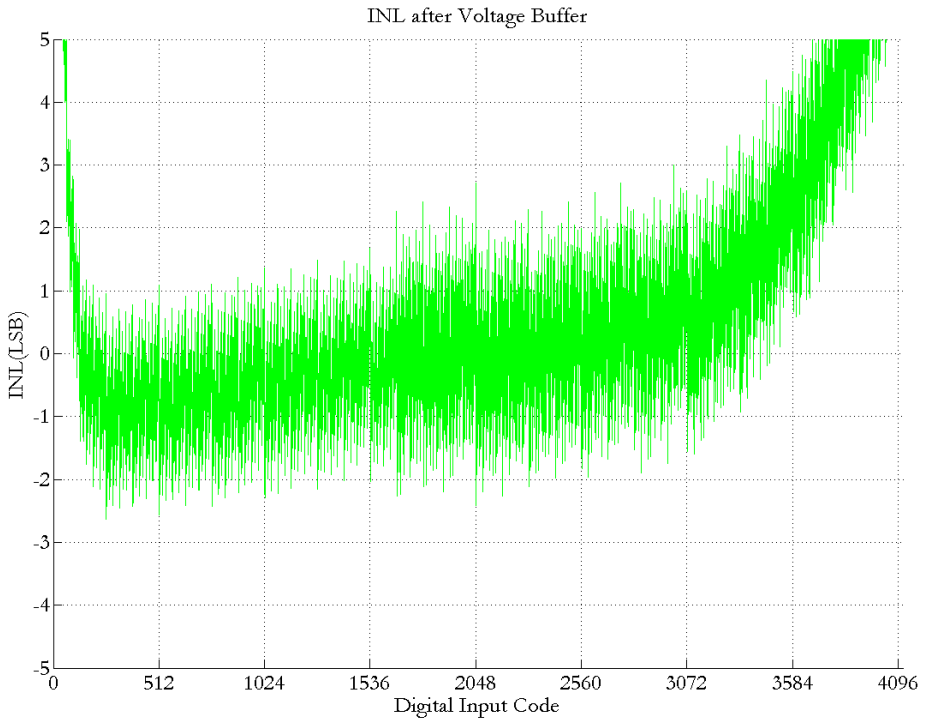
Figure 6.3: Simulated static behavior after capacitor array.



(a) Ideal and actual response.

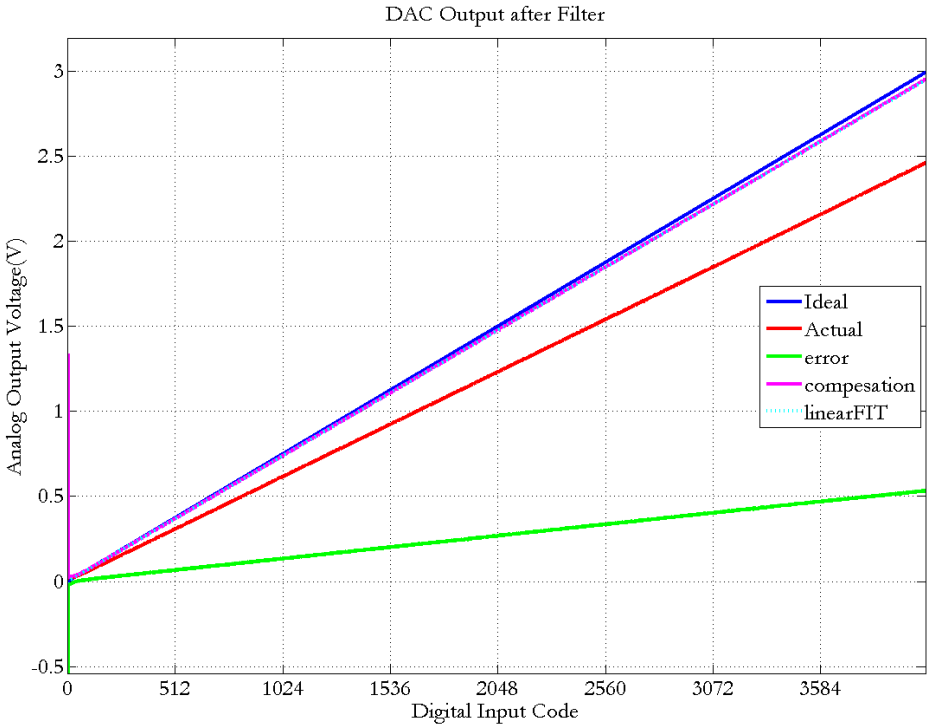


(b) DNL

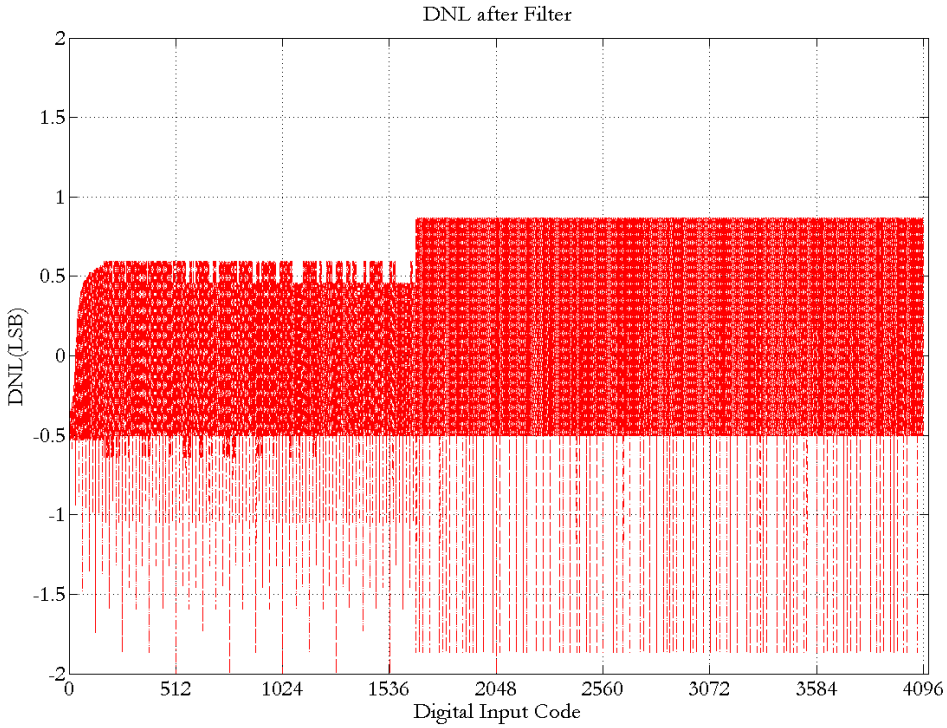


(c) *INL*

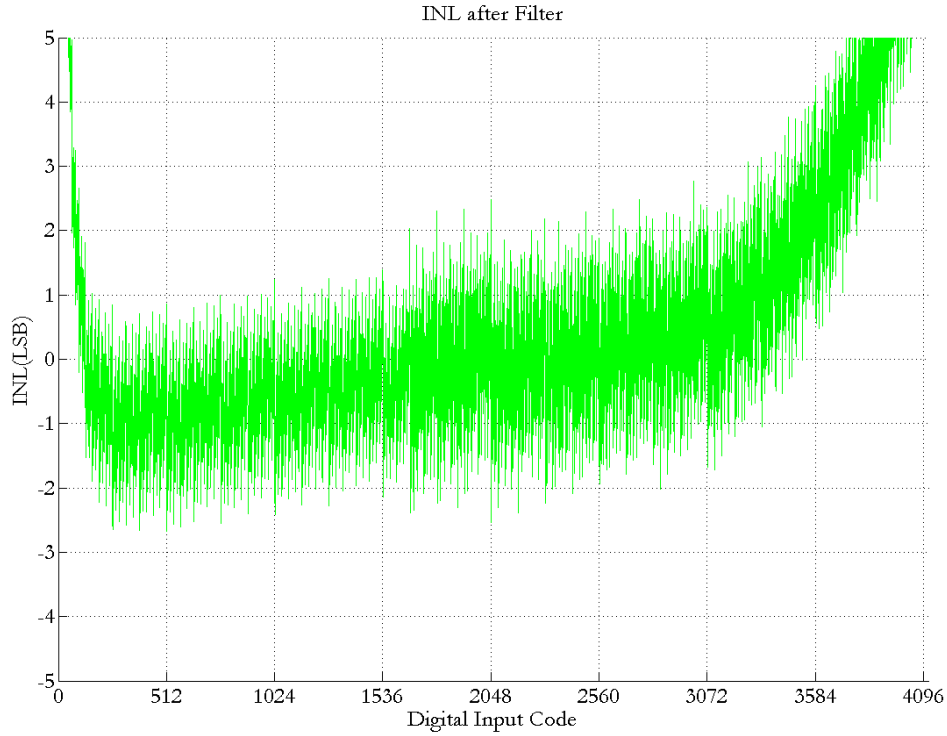
Figure 6.4: Simulated static behavior after voltage buffer.



(a) Ideal and actual response.

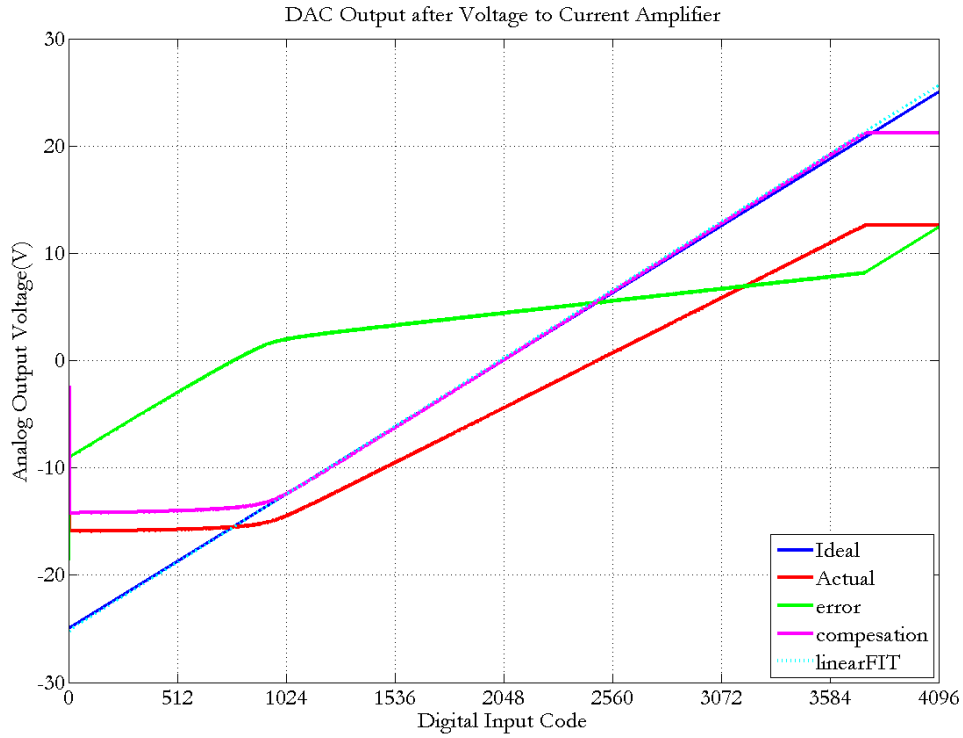


(b) DNL

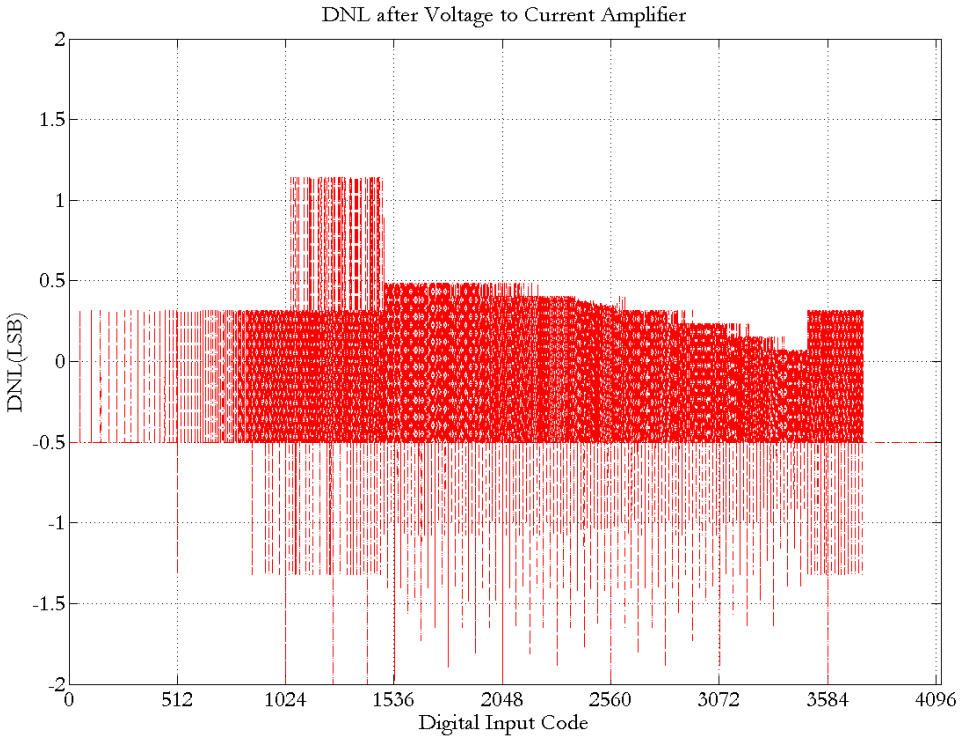


(c) INL

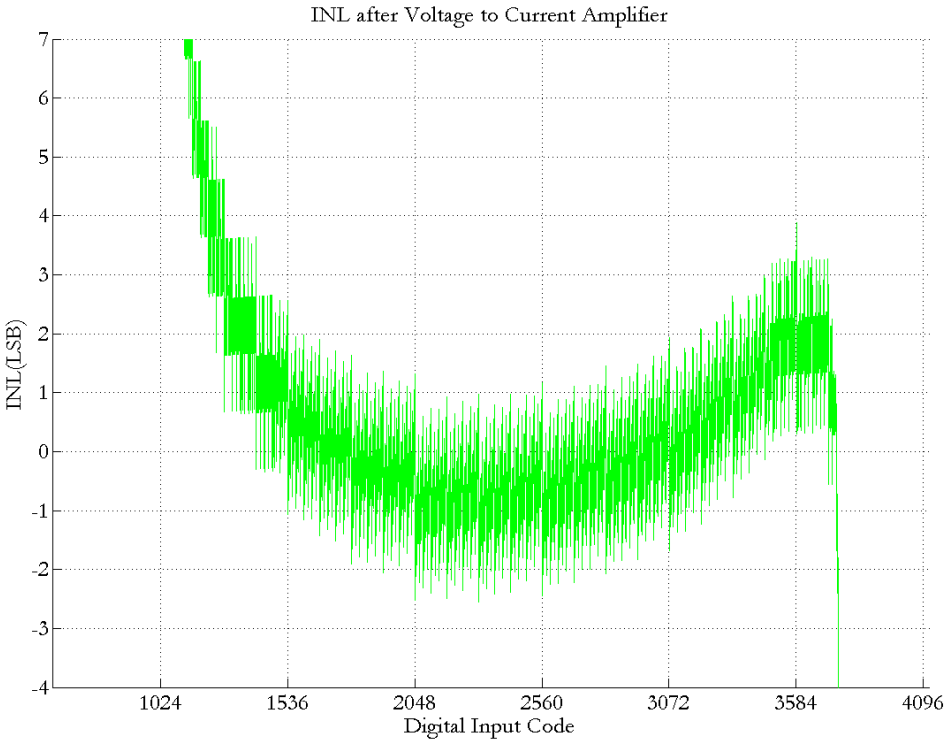
Figure 6.5: Simulated static behavior after filter.



(a) Linear Response



(b) DNL



(c) INL

Figure 6.6: Simulated static behavior after output amplifier.

The dynamic testing of a DAC was done in two parts. The time domain parameters were calculated by sending a half scale step signal since changing the MSB results in the highest settling time and glitch energy. The resulting waveform is show in Fig. 6.7. Notice that the voltage at the capacitor array has a very sharp spike due to clock feed through. This effect is more noticeable at the output of the buffer where the glitch energy was equal to 828 nV-s.

To estimate the frequency domain parameters a signal of known amplitude and frequency was sent to the ideal ADC and the resulting buffered digitized signal was then applied to the DAC input. Afterwards, a Fast-Fourier-Transform (FFT) was applied to reveal the spectrum of the output signal. The spectral analysis was done for the full Nyquist bandwidth as well as over the band of interest for the fluxgate magnetometer. The value of $SFDR$ was obtained directly from the FFT.

However, $SNDR$ and THD required further processing of the spectrum and $ENOB$ was estimated using Eq. (3.19).

A special mention is given to the recording of frequency domain dynamic parameters. Each recorded value is not absolute and only represents the behavior observed for a given input setup. In order to compare these parameters across different designs, one must know the used input range, sampling speed and signal frequency.

Table 6.3 lists the dynamic parameters obtained when the input of the test system was a 350Hz 1.5 Vpp sine wave with DC offset of 1.5 V and the sampling frequency was 118k samples per second. Figure 6.8 shows a plot of the analog output voltage from the DAC and Fig 6.9 shows the plot of the spectrum obtained up to the full Nyquist band and Fig. 6.10 shows the spectrum for the window of interest.

Table 6.3: Simulated DAC dynamic parameters.

Block	***settling time***	***glitch energy***	**Latency (μs)**	***SNR*** **(dB)**	***SNDR*** **(dB)**	***SFDR*** **(dBc)**	**THD**	**ENOB**
Scale	100 ns	48 nV-s	3.6	60	38.2	55	5.9%	6.1
Buffer	2000 ns	828 nV-s	5.5	60	38.4	55	5.8%	6.1
Filter	1700 ns	0	6.7	92.5	76.7	84	0.07%	12.44
Amplifier	1600 ns	0	6.8	92.5	55.1	84	0.86%	8.86

Realistic designs are sensitive to process, voltage, and temperature variations. In order to guarantee the functionally of the DAC, simulations were run at all five process corners. Table 6.4 lists the power consumption estimated.

Table 6.4: Simulated DAC power consumption

Block	***TT*@27°C (mW)**	***FF*@-40°C (mW)**	***SS*@125°C (mW)**	***FS*@27°C (mW)**	***SF*@27°C (mW)**
DAC	0.602	0.469	.842	0.607	0.597
Amplifier	63.3	45.8	58.2	59.0	65.7
Total	**64**	**47**	**60**	**60**	**67**

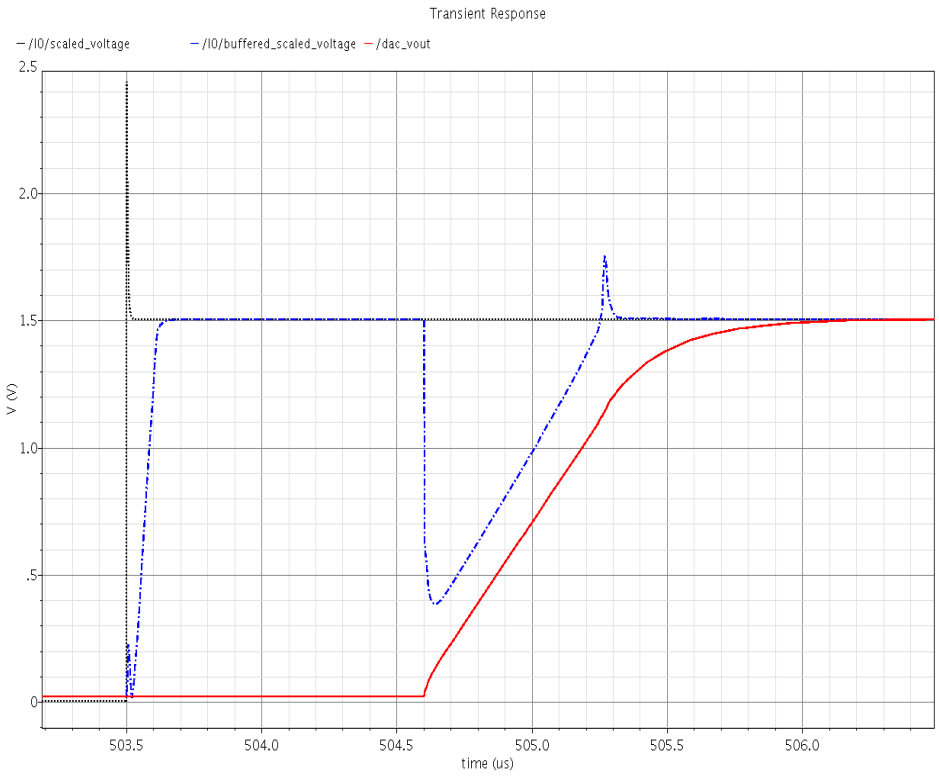


Figure 6.7: Simulated settling time response.

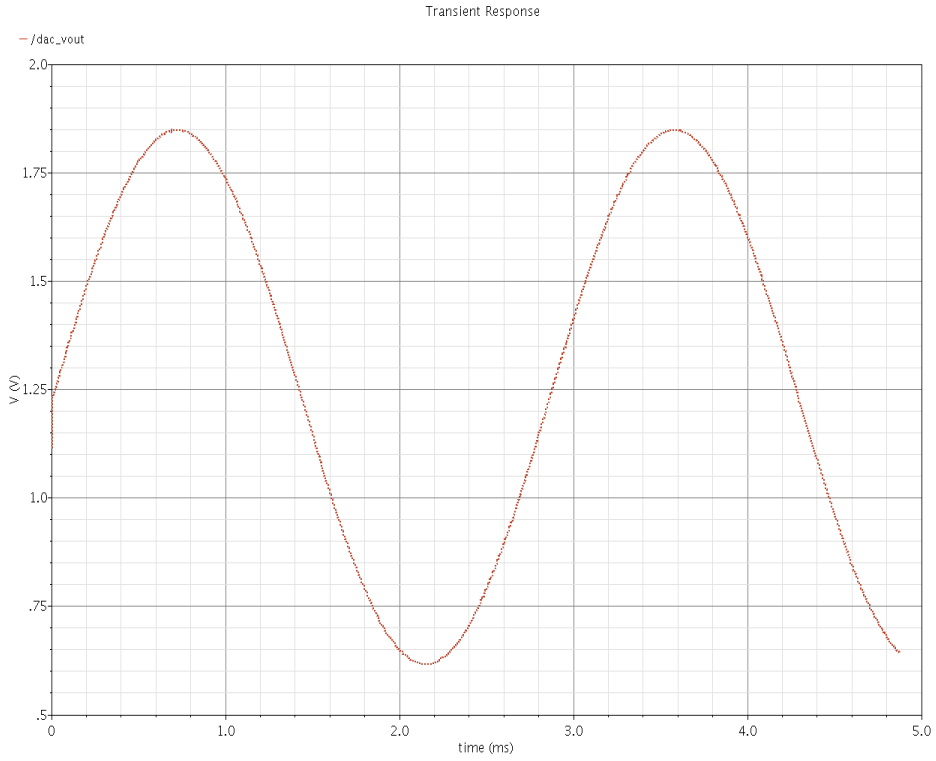


Figure 6.8: Simulated conversion of sine wave $f = 350\ Hz, 1.5\ Vpp$ $(118kS/s)$.

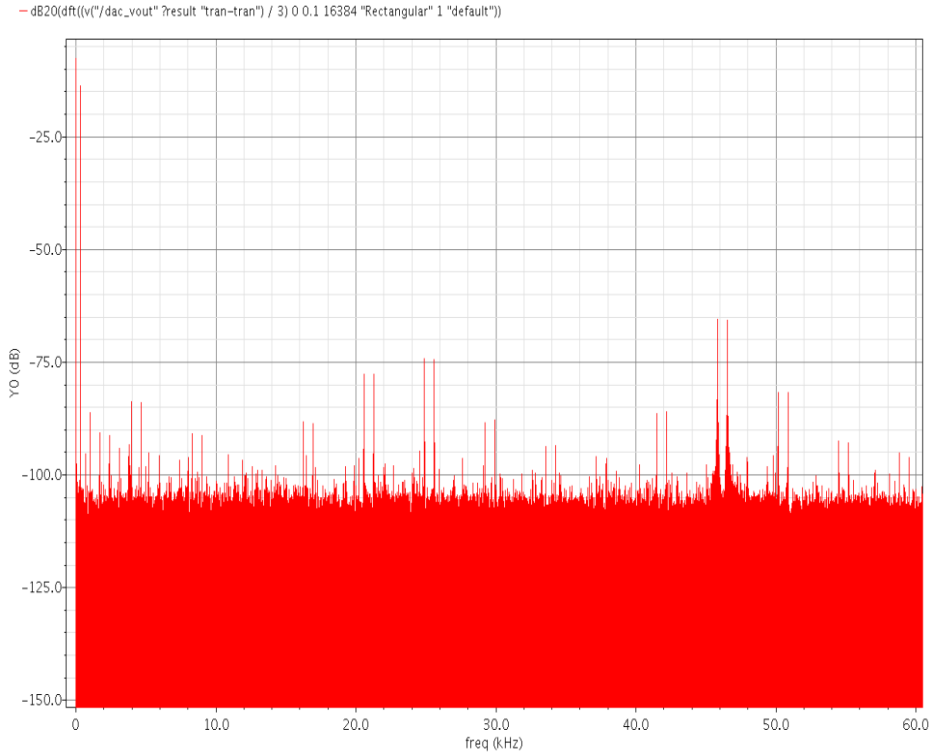


Figure 6.9: Simulated spectrum of sine wave $f = 350\ Hz, 1.5\ Vpp$ $(118kS/s)$.

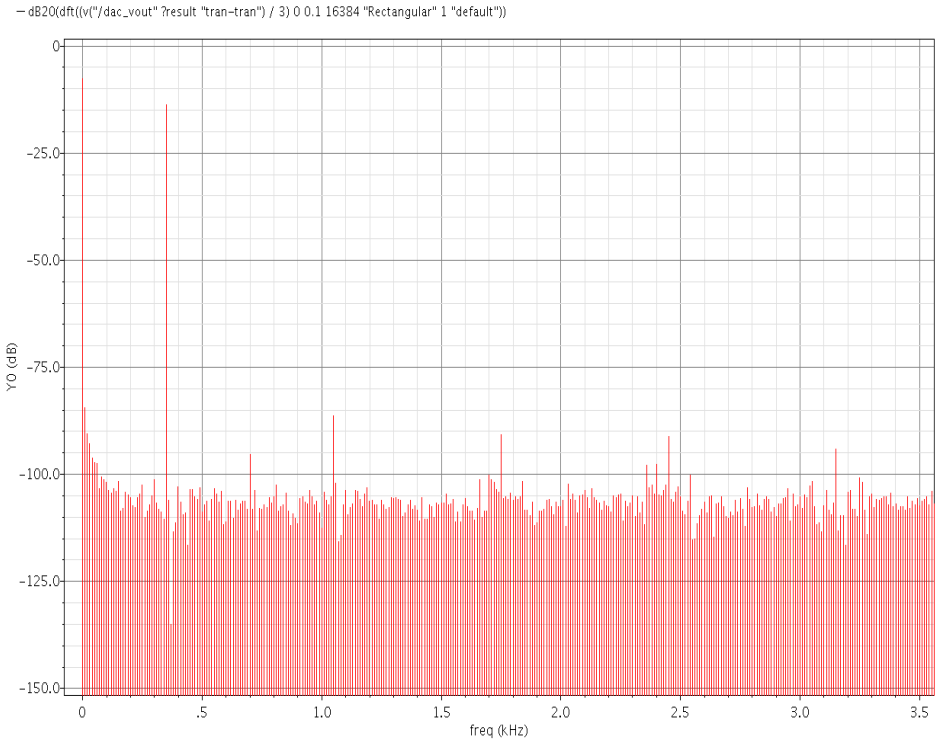


Figure 6.10: Simulated spectrum at window of interest.

Chapter 7: Conclusion and Future Work

A low power 12 bit charge DAC was designed in standard 0.35 μm double poly four metal CMOS technology. The DAC was tested for all 4096 digital input combinations. After the voltage to current converter a step size is roughly 12 μA. The converter operates with a 3 V supply and can be configurable for different operating regions via the off chip resistors and voltage source. The main results of the DAC are a chip area of 1.2 mm × 1.3 mm, power consumption of $0.6\,mW$, $INL = \pm 2\ LSB, DNL = \pm 1\ LSB, and\ SFDR = 84\ dBc$.Th design was integrated with digital and analog blocks. This work achieved a low power mixed-signal ASIC which has the capabilities to control the excitation and pick up coils of a fluxgate magnetomer based on the novel RTD principle.

This thesis laid the foundation for the Intellectual Property (IP) of a low power DAC suitable to generate a periodic signal to energize the RTD fluxgate magnetomer and assist the efforts of reducing size, cost, and energy to achieve a portable and high sensitivity magnetic vector field sensor. The charge DAC presented here may be incorporated in future Successive Approximation Register ADCs. The common centroid layout for large capacitors may also be valuable to other mask designs like switch capacitor circuits and charge pumps.

The immediate future work needed is the full re-characterization of the designed DAC parameters from measured values. The static performance can be measured via a fast oscilloscope. The digital input combinations from 0 to 4096 can be generated from a FPGA board emulating a simple counter designed in Verilog. To measure the dynamic performance a spectrum analyzer should be connected to the output of the DAC driven by an off the shelf ADC that has low noise and high resolution. The input of the ADC should be a single tone sine wave. Alternatively, a LABVIEW workbench can also be designed to measure both static and dynamic metrics.

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Appendix A VerilogA

VerilogA is a hardware description language developed for analog design and used to describe behavioral models of analog circuits at a high level of abstraction. The main advantage of VerilogA is that block or modules written in this high level language may be instantiated together with blocks written in a low level language like Spectre a derivative language of the original Berkeley protocol SPICE.

```
////////////////////////////////////////////////////////////
// Ideal 12 bit Analog to Digital Converter
//
// PARAMETERS:
//   slack = The smallest time interval considered negligible for
// cross event on clock [S]
//   tconv = Delay from threshold crossing to output change [S]
//   trise = Rise time for digital output signals [S]
//   trise = Rise time for digital output signals [S]
//    vmax = ADC Full scale output voltage [V]
//    vmin = ADC Zero scale output voltage [V]
//    vone = The voltage of a logical 1 on digital outputs [V]
//     vth = Threshold value of clock signal [V]
//   vzero = The voltage of a logical 0 on digital outputs [V]
//

`include  "discipline.h"
`include  "constants.h"
`define NUM_ADC_BITS   12

module a2d_ideal (vin, clk, dout);
 input   vin, clk;
 voltage vin, clk;
```

```
output  [`NUM_ADC_BITS-1:0] dout;
voltage [`NUM_ADC_BITS-1:0] dout;

 parameter real  vmax = 3;
 parameter real  vmin = 0;
 parameter real   one = 3;
 parameter real  zero = 0.0;
 parameter real   vth = 1.8;
 parameter real slack = 10.0p from (0:inf);
 parameter real trise = 200p from (0:inf);
 parameter real tfall = 200p  from (0:inf);
 parameter real tconv = 2.0u from [0:inf);
 parameter integer traceflag = 0;

   real   sample, vref, lsb, voffset;
   real   vd[0:`NUM_ADC_BITS-1];
   integer ii, binvalue;

  analog begin
    @(initial_step or initial_step("dc", "ac", "tran", "xf"))  begin
      vref = (vmax - vmin) / 2.0;
      lsb  = (vmax - vmin) / (1 << `NUM_ADC_BITS) ;
      voffset = vmin;

      if (traceflag)
      $display("%M ADC  range ( %g v ) /  %d bits  = lsb %g volts.\n",
                vmax - vmin, `NUM_ADC_BITS, lsb );

      generate i ( `NUM_ADC_BITS-1, 0) begin
         vd[i] = 0 ;
      end
```

```
    end

    @(cross ( V(clk)-vth,  1, slack, clk.potential.abstol)) begin
      binvalue = 0;
      sample = V(vin) - voffset;
      for ( ii = `NUM_ADC_BITS -1 ; ii>=0 ; ii = ii -1 ) begin
       vd[ii] = 0;
       if (sample > vref ) begin
         vd[ii] = one;
         sample = sample - vref;
         binvalue = binvalue + ( 1 << ii );
       end
       else begin
        vd[ii] = zero;
       end
       sample = sample * 2.0;
      end
      if (traceflag)
        $strobe("%M at %g sec. digital out: %d   vin: %g  (d2a: %g)\n",
                $abstime, binvalue,  V(vin), (binvalue*lsb)+voffset);
    end

    generate i ( `NUM_ADC_BITS-1, 0) begin
      V(dout[i])  <+   transition ( vd[i] , tconv, trise, tfall );
      end
  end
endmodule
`undef NUM_ADC_BITS
////////////////////////////////////////////////////////////////////////////////
```

Appendix B OCEAN

Open Command Environment for Analysis (OCEAN) is a text based process that can be run from a UNIX shell or form Virtuoso's Command Interpreter Window (CIW). OCEAN allows the creating of scripts to automate circuit verification. Parametric analyses, corners analyses, and statistical analyses are performed more efficiently and can also be useful to run simulations from a non graphic, remote terminal.

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;      OCEAN script to calculate power and plot spectrum of 12 bit charge DAC      ;;;;;;
simulator( 'spectre )
design(
"/users/eesunz/faculty/cdsemac/cadence/simulation/mm_driver/spectre/sim_05032010/
netlist/netlist")
resultsDir(
"/users/eesunz/faculty/cdsemac/cadence/simulation/mm_driver/spectre/sim_05032010"
)
modelFile(
   '("/users/eesunz/faculty/cdsemac/spawar/models/native_tsmc35/hspice.mdl" "")
)
analysis('tran ?stop "1m"  )
save( 'v "/analog_input" "/dac_vout" )
save( 'i "/R2/PLUS" )
temp( 27 )

out1=outfile("./thesis_scaled_voltage_r.data" "w")
out2=outfile("./thesis_buffered_scaled_voltage_r.data" "w")
out3=outfile("./thesis_dac_vout_r.data" "w")
out4=outfile("./thesis_coil_current_r.data" "w")
```

```
run()
selectResult( 'tran )

plot(getData("/V0/PLUS") getData("/analog_input") getData("/dac_vout")
getData("/R2/PLUS") getData("/I0/64") getData("/I0/78"))

plot(dB20(dft(v("/dac_vout" ?result "tran-tran")/3 0 1m 16384 "Rectangular" 1 "default" )))


for(tt 1 8193
    time=tt*.0000085-1*.0000085
    fprintf(out1 "%f ", time)
    fprintf(out2 "%f ", time)
    fprintf(out3 "%f ", time)
    fprintf(out4 "%f ", time)
    fprintf(out1 "%e\n" value(VT("/I0/scaled_voltage"),time))
    fprintf(out2 "%e\n" value(VT("/I0/buffered_scaled_voltage"),time))
    fprintf(out3 "%e\n" value(VT("/dac_vout"),time))
    fprintf(out4 "%e\n" value(IT("/R2/PLUS" ),time))
 )
close(out1)
close(out2)
close(out3)
close(out4)

power= integ(i("/V0/PLUS" ?result "tran-tran") 0 1m )*3/1m
printf("power consumption = %e\n", power)

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
```

Appendix C MATLAB

MATLAB is a powerful interactive system for doing numerical computations which provides an extensive set of proven algorithms so that complex calculations may be trusted. MATLAB is friendly to UNIX users as batch mode runs are possible.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%          MATLAB script to calculate DNL and INL       %%%%%%%
clear
clc
clf
%load ../miguel/dacvout6.data
%dacdata = '../miguel/thesis_caparray_linear.data.txt';
%fd1 = fopen( data, 'r');
%temp = fscanf(fd1, '%g %g', [2 inf])';
time=data(:,1);
vout=data(:,2);
%fclose(fd1);

lsb=.05/4096;
Rref=60;
iout_bandwidth=3.0/Rref;

%dacvout = dacvout6(:,2)
%x=[0:1e-6:.036];

%y=-83.33*x+3;
%x1=linspace(0,10,200);
%q1=quantizer('float','ceil');
%range(q1)
%y2=quantize(q1,x1);
```

```
%Quantize a signal to n bits.  This code assumes the signal is between -1
%and +1.

b=12;                   %Number of bits;
N=34808;
%N=120;                  %Number of samples;
n=0:(N-1);              %Index

x=(lsb*n)*4096/34808-iout_bandwidth/2;

xq=vout';
xe=x-xq;                %Error

x1=15000;
x2=26000;
offset_error=xq(x1)-x(x1);
xq_no_offset=xq-offset_error;
gain_error=xq_no_offset(x2)-x(x2);
xq_slope=(xq_no_offset(x2)-xq_no_offset(x1))/(x2-x1);
best_line=n*xq_slope-iout_bandwidth/2-.0002;

figure(1)
%stem(x,'b');
x=x*1000;   %convert to mA for plotting purposes
plot(x,'b','LineWidth',3);
hold on;
%stem(xq,'r');
xq=xq*1000;         %convert to mA for plotting purposes
plot(xq,'r','LineWidth',3);
hold on;
%stem(xe,'g');
```

```
xe=xe*1000; %convert to mA for plotting purposes
plot(xe,'g','LineWidth',3);
xq_no_offset=xq_no_offset*1000;        %convert to mA for plotting purposes
plot(xq_no_offset,'m','LineWidth',3);
p=polyfit(n,xq_no_offset,1);        %%%best line fit of xq_no_offset--generate polynomials
f=polyval(p,n);                    %%%fit\..evalute polynomial
%plot(f,'g')
best_line=best_line*1000;            %convert to mA for plotting purposes
plot(best_line,':c','LineWidth',3)
legend('Ideal','Actual','error','offset compesation','linearFIT','Location','SouthEast')
title('DAC Output after Voltage to Current Amplifier','FontName','Garamond','FontSize',20
);
ylabel('Analog Output Voltage(V)','FontName','Garamond','FontSize',20)
xlabel('Digital Input Code','FontName','Garamond','FontSize',20)
%ylim([-1 3])
xlim([0 34808])
set(gca,'XTick',0:4351:34808)       %set no. of ticks
set(gca,'XTickLabel',{'0','512','1024','1536','2048','2560','3072','3584','4096'})
grid
hold off

x=x/1000;   %convert to A for
xq=xq/1000;         %convert to A
xq_no_offset=xq_no_offset/1000;        %convert to A
best_line=best_line/1000;            %convert to A

for k=1:34807
dnl(k) = xq(k+1)-xq(k);
end
dnl=dnl/lsb-1/2;
figure(2)
plot(dnl,'-.r','LineWidth',1)
```

```
title('DNL after Voltage to Current Amplifier','FontName','Garamond','FontSize',20)
ylabel('DNL(LSB)','FontName','Garamond','FontSize',20)
xlabel('Digital Input Code','FontName','Garamond','FontSize',20)
set(gca,'XTick',0:4351:34808)      %set no. of ticks
set(gca,'XTickLabel',{'0','512','1024','1536','2048','2560','3072','3584','4096'})
ylim([-2 2])
grid

figure(3)
hold on
inl1=(xq_no_offset-f)/lsb;
inl2=(xq_no_offset-x)/lsb;
inl3=(xq_no_offset-best_line)/lsb-20;
%inl4=(xq-f)/lsb;
%plot(inl1,'b')
%plot(inl2,'r','LineWidth',3)
plot(inl3,'-g','LineWidth',0.5)
title('INL after Voltage to Current Amplifier','FontName','Garamond','FontSize',20)
%legend('Compesated-Ideal','Compesated-LinearFit','Location','Northeast')
ylabel('INL(LSB)','FontName','Garamond','FontSize',20)
xlabel('Digital Input Code','FontName','Garamond','FontSize',20)
set(gca,'XTick',0:4351:34808)      %set no. of ticks
set(gca,'XTickLabel',{'0','512','1024','1536','2048','2560','3072','3584','4096'})
ylim([-5 5])
grid
hold off
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

Vita

Miguel Angel Alamillo Jr. was born on October 8, 1985 in El Paso, Texas. The second born son of the late Miguel A. Alamillo Sr. and Tommy Reyes, he graduated from Escuela Preparatoria Federal por Cooperacion EMS-2/3 "El Chamizal" in Cuidad Juarez in 2003. He entered the University of Texas at El Paso (UTEP) in the Fall of 2003 to pursue a Bachelor of Science Degree in Electrical Engineering. In the summer of 2006, he carried out research at Cornell University in the area of nanophotonics. Afterwards, he went on to work fulltime for IBM as a digital circuit design intern between August 2006 and January 2007. Miguel graduated with honors in the Spring of 2008 and started to work on his Master of Science Degree in Computer Engineering at UTEP. His research area has been VLSI with a focus on CMOS Mixed Signal Circuit Design. Upon graduation, he will be joining Intel Corporation, in Hillsboro, Oregon as part of the Rotational Engineering Program.

Permanent address: 1509 Ruth Deerman Pl.

El Paso, TX 79912

This thesis was typed by the author.