2009-01-01

Microstructure And Electrical Performance Of Sputter-Deposited Hafnium Oxide (hfo2) Thin Films

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MICROSTRUCTURE AND ELECTRICAL PERFORMANCE OF SPUTTER-DEPOSITED HAFNIUM OXIDE (HfO_2) THIN FILMS

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Dedication

To my parents and siblings.

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by

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THESIS

Presented to the Faculty of the Graduate School of

The University of Texas at El Paso

in Partial Fulfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE

Department of Electrical and Computer Engineering

THE UNIVERSITY OF TEXAS AT EL PASO

December 2009

Acknowledgements

First of all I want to thank Jehovah God for giving me the opportunity and help me to finish this work. I want to express my sincere gratitude to Dr. David Zubia, Dr. C. V. Ramana and Dr. Stella Quinones for supporting me and guiding me through my graduate studies and allowing me to be part of the nanoMIL research group at UTEP. Their professional experience, enthusiasm and passion inspired me to perform good research work and to continue my education after earning my bachelor's degree. I want to thank also Dr. John McClure and Dr. Greg Lush for their advice and overall support.

I want to thank present and past nanoMIL student generations for their support and useful discussions that made possible this work: Arev, Aryzbe, Ivan, Jose, Jacobo, Luis, Mario, Michelle, Noel, Oscar, Rafael, Rama and Sandy; and also, Guillermo and Francisco from their feedback and input to my research work. I want to thank my parents Estela and Rodolfo and my siblings Zoe and Rodolfo for motivating and supporting me during moments of stress and difficulty that come together with any research work.

Last but not least, I thank the Environmental Molecular Sciences Laboratory, a national scientific user facility sponsored by the Department of Energy's Office of Biological and Environmental Research and located at Pacific Northwest National Laboratory for their contribution to a portion of the results in this research. I also sincerely thank the Louis Stokes Alliance for Minority Participation Bridge to the Doctorate (LSAMP-BD) program for its financial support through part of my Master's degree

Abstract

Hafnium oxide (HfO_2) based dielectrics have been currently considered as the possible replacements for the traditional gate-oxide (SiO_2) of the complementary metal-oxide semiconductor (CMOS) devices. The high dielectric constant, wide band gap, and thermal stability in contact with Si make HfO_2 a potential material for application in CMOS devices. The performance of HfO_2 as a gate oxide material, however, depends on its quality and interface structure with Si. In this work, HfO_2 thin films have been deposited by rf sputtering onto Si(100) substrates under varying growth temperatures (T_s). The objective of the work is to understand the growth and microstructure of sputter-deposited HfO_2 films and optimize the conditions to produce high-quality materials. A HfO_2 ceramic target has been employed for sputtering while varying the substrate temperature, T_s, from 25 °C to 500 °C. The effect of growth temperature on the microstructure of the deposited HfO_2 films has been studied using grazing incidence x-ray diffraction (GIXRD), X-ray photoelectron spectroscopy (XPS) and high-resolution scanning electron microscopy (HR-SEM). The results indicate that the HfO_2 films grown at Ts<200 °C are amorphous. An amorphous-to-crystalline transition occurs at T_s = 200 °C. Nanocrystalline HfO_2 films crystallized in a monoclinic structure with a particle size of ~20 nm. Cross-sectional HRSEM and capacitance analyses of metal-oxide-semiconductor capacitors indicate the presence of an interfacial layer between HfO_2 and Si that increases in thickness as the substrate temperature increases. Energy dispersive spectroscopy (EDS) shows that the interfacial layer is composed of HfSiO and has a dielectric constant much lower than 25. In contrast, dielectric constants as high as 25 were obtained from HfO_2 films grown at room temperature.

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1. Introduction

Since the invention of the integrated circuit (IC) in the 1950's, technology has progressed dramatically. We have faster computers, sophisticated research equipment, and in general better electronics. The electronics industry's evolution can be summarized in Moore's law, which predicts that in order to keep up with demand of new electronics, the number of metal-oxide-semiconductor field effect transistors (MOSFETs) per IC will have to double every 2 years. This means that the size of MOSFETs has to be reduced in order to place more transistors inside an IC. The cross sectional view of a MOSFET, basic building block of ICs is shown in Figure 1.

The gate stack of a MOSFET is essentially a metal oxide semiconductor (MOS) capacitor. In order to turn on a transistor, voltage is applied to the gate terminal and an inversion layer known as the channel is formed just right below the oxide layer that is used as a conduction path for electrons. The bigger the capacitance of the gate stack the better the control of the gate over the channel. A critical part of transistors that is affected by size reduction is the gate oxide. As the dimensions of MOSFETs are scaled down, the thickness of the oxide film has been reduced in order to have a better control (high capacitance) over the channel of smaller devices.

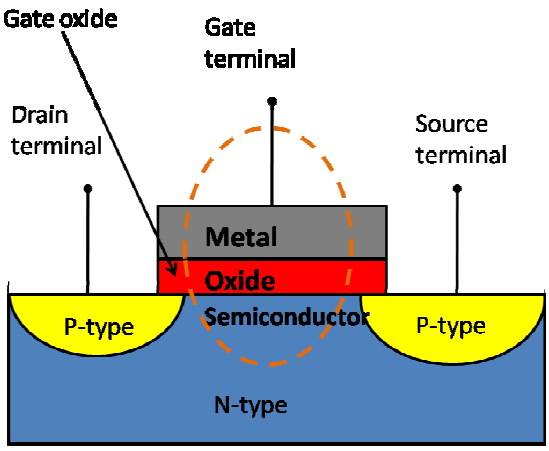

Figure 1 Metal-oxide-semiconductor field effect transistor (MOSFET) drawing. Circled in dotted lines is the gate stack of a MOSFET consisting of a top metal electrode or polysilicon, an oxide thin film and the semiconductor substrate.

The capacitance of the oxide layer in a MOS structure is given by the following formula:

$$C(acc) = C_0 = \frac{K_0 \varepsilon_0 A_G}{x_0} \quad (1)$$

where k_0 is the oxide dielectric constant, ε_0 = 8.85 x 10^{-4}, A_G is the gate area, and x_0 is the oxide thickness. From Equation (1) it is clear that the capacitance of a MOS structure can be increased by reducing the oxide thickness, increasing the gate area (which is opposite to scaling down transistors) and increasing the dielectric constant which implies using a new oxide material.

1.1 BACKGROUND

For more than four decades, silicon dioxide (SiO_2) has served the electronics industry as the gate oxide of MOSFETS due to its excellent electrical and material properties. Since SiO_2 is grown thermally from the Si wafer, it is very easy to grow amorphous SiO_2 thin films with uniform and controlled thickness and with very few defects in the silicon (Si)/SiO_2 interface and in the bulk [1]. SiO_2 is very stable at high temperature processing. Moreover, it has a large band gap (9 eV) and the conduction band and valance band offsets with respect to silicon makes it an excellent insulator material for CMOS applications [1].

As mentioned above, the thickness of the SiO_2 layer has been reduced concomitant with device scaling to increase capacitance of the gate [2]. However, a fundamental limit in SiO_2 thickness reduction is imposed by the nature of the material and quantum mechanics. Below 7 Å, SiO_2 starts losing its insulating properties and cannot be used as gate oxide in MOSFETs fabrication anymore. A minimum of two monolayers (MLs) thick SiO_2 is required in order to have the advantage of its full band gap [3]. Two MLs of SiO_2 measure 7 Å in thickness, suggesting that the minimum thickness for the SiO_2 gate oxide is ~7 Å. Below this thickness SiO_2 does not behave as an insulator anymore and leakage becomes a huge problem. Additionally, at thickness below ~1.2 nm, leakage current due to quantum mechanical

tunneling starts to become a problem. For very thin layers, electrons start behaving as waves instead of particles and tunnel through the thin SiO_2 layer, causing unacceptable leakage current [2]. Figure 2 shows a schematic representation of the wave behavior of electrons and the finite probability for electron tunneling through a 1.2 nm oxide layer.

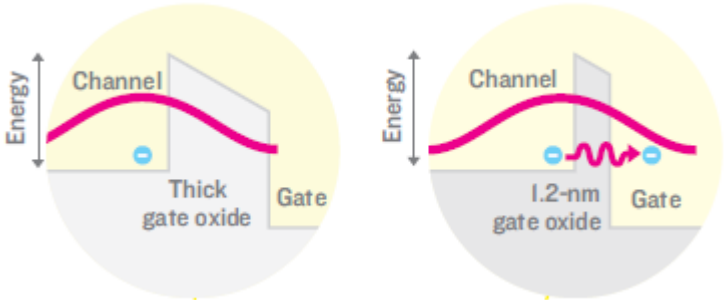

Figure 2 Quantum mechanical tunneling current in a 1.2 nm SiO_2 film [2].

Reliability is another problem encountered by reduction in the thickness of SiO_2. As the SiO_2 thickness is reduced and temperature is increased, the maximum gate voltage ($V_{G,max}$) that can be applied to an oxide layer before breakdown occurs is reduced [4]; in other words, less voltage is needed to produce an electric breakdown of SiO_2 as its thickness is reduced and temperature is increased.

1.2 REQUIREMENTS FOR NEW GATE OXIDE MATERIAL

Since decreasing the oxide thickness is not a suitable solution to increase MOS capacitance anymore, this has created the need for new materials with higher dielectric constant (k) to substitute SiO_2 as the gate oxide material in MOSFETs. The dielectric constant reflects the extent of polarization of a specific material [2]. Molecules inside high-k dielectrics are reoriented easier in the presence of an electric field than in low-k materials [2], resulting in larger capacitances and therefore, better control of a MOSFET's channel. However, in addition to the requirement of a high dielectric constant, the new

material must also exhibit other properties to make it suitable as a gate dielectric for CMOS applications. In general, the new material must have the following six characteristics [5]:

- High dielectric constant that permits further scaling down of MOSFETs in the future.
- Thermodynamic stability with silicon.
- Kinetically stable and availability to be processed under 1000 °C.
- It must be an insulator.
- There must be a good electrical interface between the oxide and the silicon.
- Few defects in the bulk.

As described earlier, a high dielectric constant is needed to have better control of a transistor's channel and to keep scaling down transistors. There are many oxides with high dielectric constants, but for most of them, their band offset with respect to silicon decreases as the dielectric constant increases [5]. It was found that a band offset of 1eV or greater for the conduction and valance band is needed between the Si and the new oxide material bands in order to prevent electron or hole carrier injection [5]. For example, strontium titanium oxide ($SrTiO_3$, referred to STO) and barium strontium titanate (BaSrTiO3, referred to BST) are high-*k* materials, however they are unsuitable because their band offsets with silicon are too small [6].

Additionally, the new oxide material must be thermodynamically stable with Si in order to prevent the formation of unwanted interfacial layers that might degrade the performance of the gate stack. For example, silicide layers have low resistance [7] and can lead to leakage current [3]. Also, thick interface layers with low dielectric constant will reduce the overall capacitance of the gate stack [3].

A large stable band gap is another characteristic that is desired. The new oxide material has to retain its insulating and dielectric properties when it is exposed to high temperature during IC

processing. An oxide material that can stay amorphous for high temperature processing is desired in order to prevent leakage current through grain boundaries [8]. Oxides that crystallize at low temperatures can still be used if they are alloyed with SiO_2 or Al_2O_3 to form silicates or aluminates (pseudo-binary alloys) that will not crystallize at low temperatures and that will keep a high dielectric constant [3].

Finally, since electrons travel very close to the Si/oxide interface, it is very important to have an interface without silicides or a polycrystalline structure that might introduce defects and lower the mobility of carriers [3]. Another concern is defects in the bulk of oxides since they give rise to high threshold voltages. In summary, a stable, high-*k* dielectric with large band gap, large offset and low density of defects is required for CMOS applications.

1.3 HfO_2 AS A GOOD GATE OXIDE CANDIDATE

Hafnium oxide (HfO_2), also known as hafnia, is a leading candidate as the next generation gate dielectric among other high-*k* oxides such as ZrO2, CeO_2, TiO_2 and Ta_2O_5. Figure 3 is a plot of band gap versus dielectric constant of various materials and shows that there is a general inverse relationship between these two parameters. HfO_2 falls in the middle of this relationship with a dielectric constant of approximately 25 [9] and a band gap of 5.68 eV [10]. HfO_2 has a dielectric constant that is 6.5 times larger compared to SiO_2 (3.8) which can increase the gate capacitance of MOSFETs significantly according to Equation 1. Moreover, the 5.68 eV band gap of HfO_2 [10] is large enough to allow it to behave as an insulator in CMOS. In addition to exhibiting a high dielectric constant and acceptable band gap, HfO_2 has a high density (9.68 g/cm^3) that makes it impermeable to impurity diffusion [11].

Good thermal stability is desired to prevent the formation of silicides or interfacial layers with low dielectric constant that would decrease the overall capacitance of gate stacks in MOSFETs [6].

Thermal stability with Si at temperatures up to 900 °C is one of the advantages of HfO_2 over other high-k materials such as ZrO_2 [14].

Although HfO_2 crystallizes at very low temperatures, the leakage current among crystalline HfO_2 has been found to be similar to the amorphous phase [6]. However, in an attempt to reduce leakage current further, some research has focused on forming silicates based on HfO_2 and the addition of nitrogen to increase the crystallization temperature and maintain an amorphous structure [8,12,13].

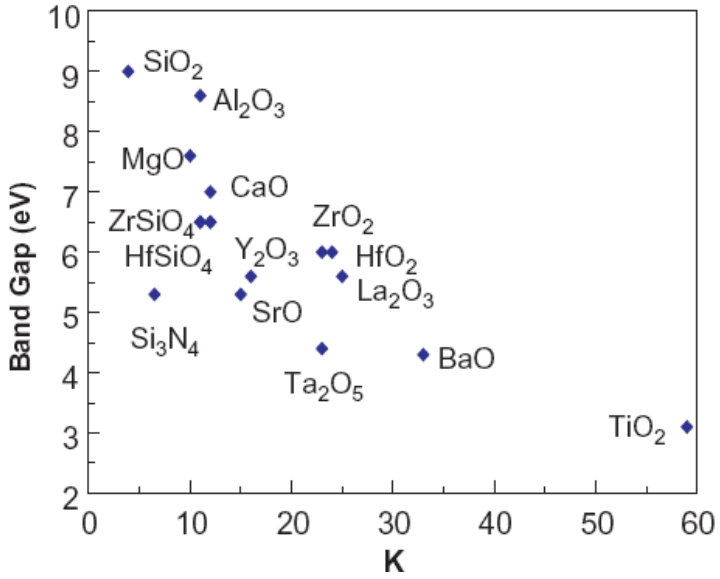

Figure 3 Band gap of oxide materials as a function of their dielectric constant from J. Robertson [13].

2. Motivation to the Present Work

Hafnium oxide posses many qualities that makes it ideal to substitute SiO_2 as the gate dielectric of MOSFETs in future IC manufacturing; however, there are still challenges and a lack of a complete understanding of this material that prevents taking full advantage of its merits. A very important problem with high-*k* dielectrics is the large amount of defects of the as-deposited films that contribute to the increment of oxide charges in the bulk and at the interfaces [15]. In order to employ HfO_2 as a base material for the gate oxide in MOSFETs it is necessary to enhance the quality of the HfO_2 deposited films. Importantly, the amount of defects present in the deposited films depends on the deposition technique used to grow the films.

2.1 PREVIOUS WORK

Various HfO_2 film deposition techniques have been investigated for CMOS applications including; sputtering a pure HfO_2 target, reactive sputtering from an Hf target in an oxygen ambient, atomic layer deposition (ALD), pulsed laser deposition and electron beam evaporation. Unfortunately, all the techniques indicate the formation of an undesirable interfacial layer (IL) between the oxide and the Si substrate [18 - 21]. A challenging problem therefore has been developing deposition conditions and concomitant post deposition processing such that the films possess the desired characteristics outlined in Chapter 1. Various studies have focused on optimizing of deposition and post processing conditions to reduce the interfacial layer, bulk and interface charge traps, and leakage current.

Prevention of the formation of ILs at the HfO_2-Si interface or alternatively passivating their effect is critical to the performance of MOSFETs. ILs can modify the band offset between HfO_2 and Si and introduce defects that can potentially trap charges and affect reliability of devices. [13] In addition, IL's resulting from a compositional mixture of the Hf-Si-O system have a lower dielectric constant

compared to HfO_2 and can dramatically reduce the overall capacitance of the gate stack [22]. Although HfO_2 is very stable, it shows a propensity to form silicate interfaces [23]. The IL forms during high temperature oxidation steps in the MOSFET fabrication processes [24] and during annealing treatments [25, 26]. In one study, the effect of rapid thermal annealing (RTA) at 600 °C in a N_2 atmosphere after depositing HfO_2 using reactive sputtering was investigated [16]. It was found that a hafnium silicate (HfSiO) interfacial layer formed after the samples were annealed; and its thickness increased with annealing time.

Different methods have been proposed to eliminate the ILs and their associated effects. For example, deposition of a thin Hf film on top of Si substrate prior to HfO_2 deposition was found to be effective to prevent oxygen diffusion to the Si substrate [27, 28]. Additionally, nitridation of the Si substrate before oxidation was found to reduce the silicate IL formation [29]. However, a detailed understanding of the effect of substrate temperature, T_s, on IL formation is still a compelling challenge.

Oxide charge traps that form during deposition is a severe problem encountered in high-*k* dielectrics. Optimizing processing parameters such as sputtering voltage, substrate bias, and annealing temperature are among the approaches taken to reduce oxide charge and leakage current. In one study, it was discovered that lowering sputtering voltage and substrate bias reduced leakage current as shown in Figure 4 and Figure 5, respectively [15].

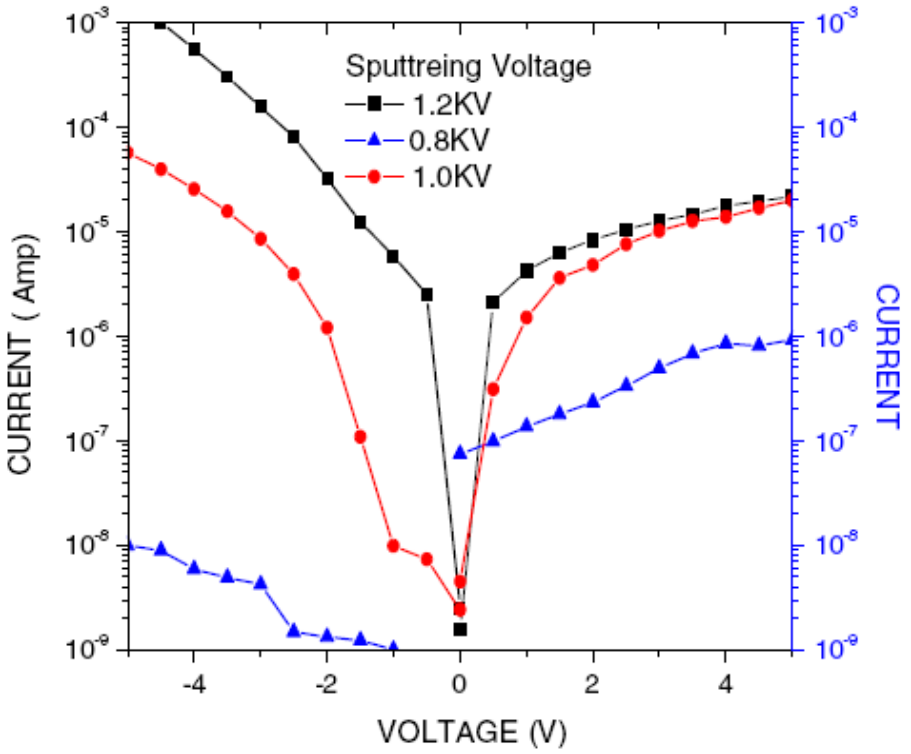

Figure 4 Leakage current as a function of sputtering voltage [15].

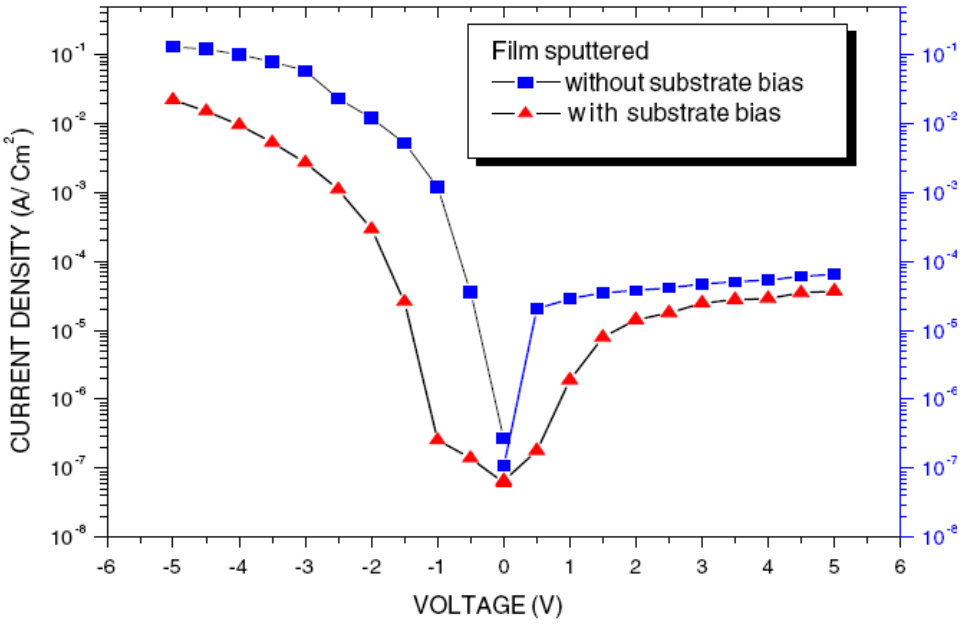

Figure 5 Leakage current as a function of substrate bias [15].

High temperature treatments are usually required in MOS fabrication processes. These processes can potentially crystallize amorphous HfO_2 if it is used as the new gate oxide material of MOSFETs. Because amorphous HfO_2 starts crystallizing at relatively low temperatures, severe leakage current could occur through the grain boundaries of its crystals. In an attempt to reduce the minimum temperature required to crystallize amorphous HfO_2, different techniques have been proposed. For example, alloying HfO_2 with SiO_2 will form a Hafnium silicate compound that will require higher temperature to crystallize; and therefore, it will stay amorphous during MOS high temperature processing and leakage currents will be prevented [17]. Li-ping Feng *et al.* compared HfO_2 and HfSiO films grown by RF sputtering. As deposited HfO_2 films were reported to be amorphous while HfO_2 films annealed at 400 °C and 600 °C were crystalline with monoclinic phase. In contrast, HfSiO films remained amorphous from room temperature up to 800 °C annealing.

2.2 CONTRIBUTION OF THIS THESIS

This work will contribute to find the suitable deposition conditions needed to grow good stoichiometric and high quality HfO_2 films using RF magnetron sputtering. A deep understanding of the HfO_2 electrical properties and microstructure depending on substrate temperature during deposition is also developed. This work will also contribute to understand the thickness of the interface layer formed between HfO_2 and Si as a function of temperature. Finally, oxide charges in HfO_2 films of MOS structures are reduced with a post deposition annealing treatment.

3. Experimental Details

3.1 Deposition Technique

SiO_2 (the current gate oxide of MOSFETs) is grown thermally and therefore its manufacturing process is very simple. HfO_2 on the other hand has to be deposited using one of the many available deposition techniques such as electron beam deposition, atomic layer deposition, metal organic beam epitaxy [25], and radio frequency (RF) magnetron sputtering. RF magnetron sputtering was chosen to deposit HfO_2 thin films in this work due to its availability in the NanoMaterials Integration Lab and its advantage of industrial large-area deposition. The basic components of an RF magnetron sputtering system are shown in Figure 6.

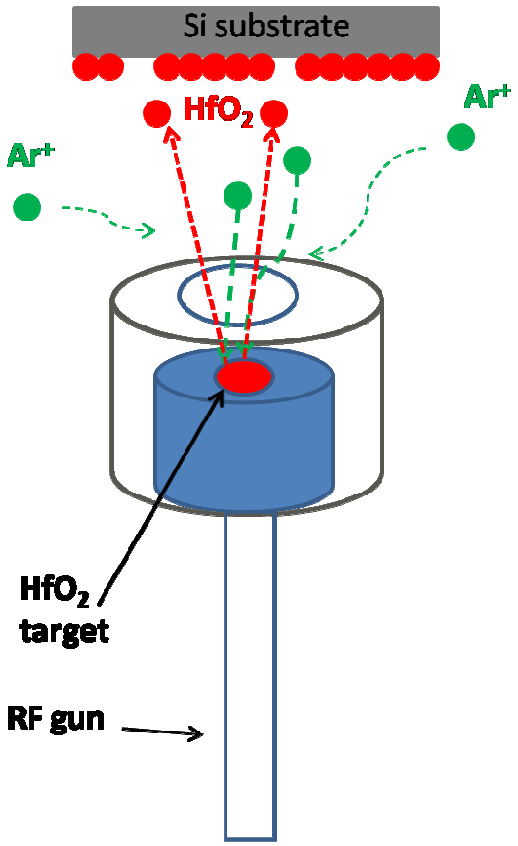

Figure 6 The basic components needed in an RF sputtering deposition system.

An RF deposition system consists of a vacuum chamber, a RF magnetron sputtering gun and an inert gas (usually argon). To start with a deposition, the chamber is pumped down to pressures in the 10^{-6} to 10^{-7} Torr range. Such a high vacuum will prevent contamination from any other material in the oxide films and high quality oxides will be deposited. Then, the magnetron sputtering gun is turned on and argon (Ar) is introduced into the chamber. Ar atoms are ionized and attracted to the magnetron gun by an electromagnetic field to bombard the HfO_2 source of material (HfO_2 target) and eject material from the surface. The bombardment of the HfO_2 target by Ar ions is continuous until the desired HfO_2 film is deposited on to the substrate.

A picture of the actual high vacuum deposition system used in this work is shown in Figure 7. This system can reach pressures as low as 10^{-7} Torr and the RF power supply uses a 13.6 MHz signal with almost no reflective power (1 W or less) to sputter oxide materials.

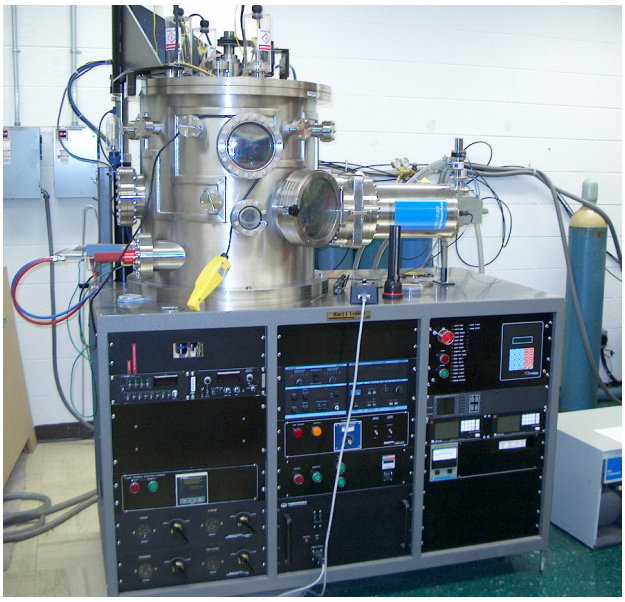

Figure 7 High vacuum deposition system used to grow HfO_2 films in this work

3.2 SUBSTRATE PREPARATION

HfO_2 thin films were deposited on Si substrates for both surface and cross-sectional analysis. HfO_2 was also deposited on Si to fabricate metal oxide semiconductor (MOS) structures and analyze the electrical properties of the films. Silicon was selected as substrate since HfO_2 is planned to be used on future integrated circuit applications. For either microstructure or electrical analysis, substrates have to be properly cleaned in order to remove contaminants that might act as dopants and affect the electrical performance and structural quality of the materials deposited. Also, a proper cleaning process is needed to protect the processing equipment from contaminants. Si substrates were cleaned with the standard RCA (Figure 8) cleaning process which consists of two steps called standard clean 1 (SC-1) and standard clean 2 (SC-2).

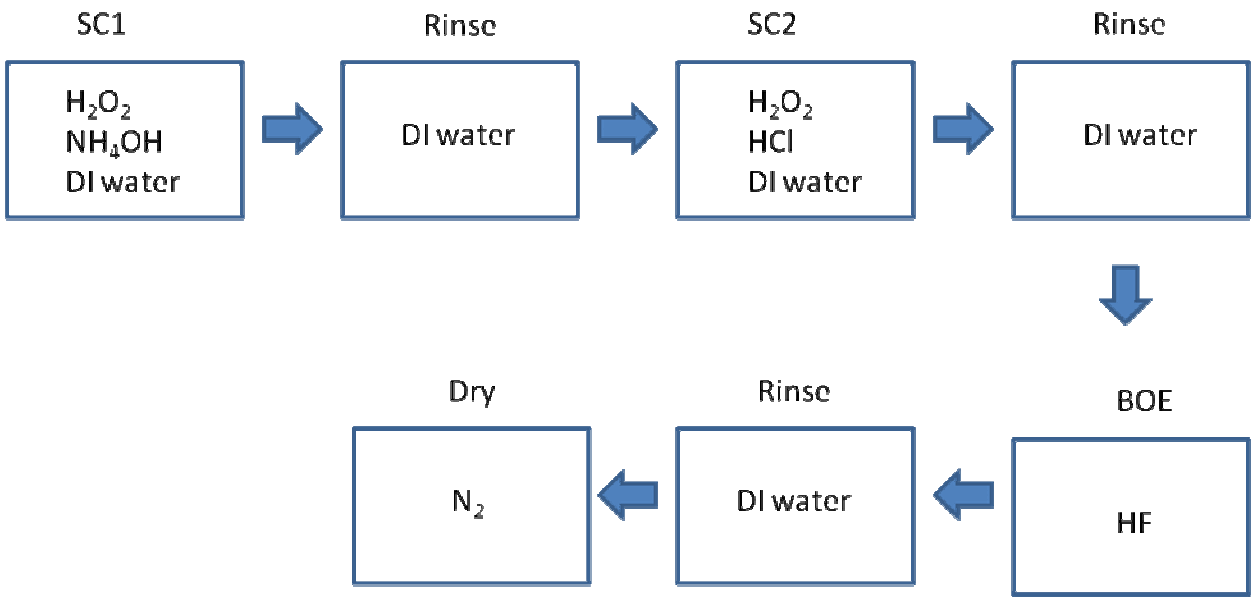

Figure 8 Standard RCA cleaning process for Si substrates.

SC-1 consists on removing organic residues from silicon which might prevent proper adhesion of oxide films to the substrate. The chemicals used during the SC-1 cleaning process are hydrogen peroxide

and ammonium hydroxide. When preparing the SC-1 solution, 150 ml of de-ionized (DI) water are heated to boiling point. Then, 10 ml of hydrogen peroxide and 10 ml of ammonium hydroxide are added (in the specified order) to only 50 ml of boiling DI water. This solution has to boil before wafers are cleaned with it.

SC-2 consists of removing ions from the silicon substrates. Ions present in the silicon might act as dopants and affect electrical response of HfO_2 films. The chemicals used during the SC-2 cleaning process are hydrogen peroxide and hydrochloric acid. To prepare the SC-2 solution, 10 ml of hydrogen peroxide are added to 50 ml of DI water. Then, 10 ml of hydrochloric acid are added to the mixture and the solution is stirred.

Si wafers were placed for 10 min. in the SC-1 solution. Then they were rinsed in DI water for 1 min. and placed in the SC-2 solution for another 10 min. After SC-2, wafers were rinsed in DI water for another minute and placed in buffered oxide etch (BOE) for 7 min. BOE is needed to remove SiO_2 that is formed as a result of the SC-1 process. Since SiO_2 can potentially act as an interface layer, it has to be removed to prevent dielectric constant degradation in the fabrication of MOS capacitors. Finally, the Si wafers were rinsed in DI water and dried with N_2.

3.3 HfO_2 FILM DEPOSITION PROCESS

HfO_2 films were grown using sputter-deposition. A 2" HfO_2 target (99.99%) was used for sputtering. The substrates were (100) p-type silicon (Si) wafers with a resistance of 10 Ω. The substrates were cleaned using the standard RCA cleaning process as described above. Then the native SiO_2 was etched from substrates just before deposition with buffered oxide etch 6:1 for 5 min. Samples were kept under vacuum right after native oxide removal. Besides removing the native oxide, this process left a hydrogen terminated surface that prevented the formation of an interfacial layer between Si substrates and the HfO_2 deposited films. The deposition system was pumped down to a base pressure of 1.5×10^{-6}

Torr. During depositions, argon flow was kept constant at 22.5 sccm to maintain a pressure of 1.5 mTorr to sputter HfO_2 target. The temperature of the substrate, T_s, was varied ranging from room temperature to 500 °C. The temperature was gradually increased from room temperature to the desired temperature in a time period of 5 min before HfO_2 film deposition. Before each deposition, the HfO_2 target was pre-sputtered for 5 min at 40 W for cleaning purposes and then depositions were run at 70 W. Two sets of HfO_2 films were grown. Deposition was made for a constant time of 30 min to produce ~ 100 nm thick films in order to understand the ILs formation and to derive quantitative information for contact film thickness. The second set of films was grown to produce ~40 nm thick HfO_2 films specifically for use in XPS measurements. The reason is that the photoelectrons emitted from samples are mostly from near the surface, therefore, information pertaining to the interface between the HfO2 and silicon wafer can be enhanced by having thinner films.

GIXRD measurements were performed using Bruker D8 advanced x-ray diffractometer. HRSEM measurements were performed using a high-performance Hitachi S4800 FE-SEM. Secondary electron imaging analysis was performed to obtain information on the surface morphology as a function of T_s. The cross-sectional analysis was also performed. For the EDS analysis, samples were positioned carefully in the SEM and the spot mode was selected in order to obtain chemical information on the substrate, film and substrate-film regions separately.

The HfO_2 films on Si were mounted onto the XPS sample solder and secured by stainless steel screws. The sample holder was then placed into the XPS vacuum introduction system and pumped to < $1x10^{-6}$ Torr using a turbomolecular pumping system prior to introduction into the main ultra high vacuum system. The main vacuum system pressure is maintained at $<5x10^{-9}$ Torr during analysis and pumped using a series of sputter ion pumps. XPS measurements were performed using a Physical Electronics Quantum 2000 Scanning ESCA Microprobe. This system uses a focused monochromatic Al Kα x-rays (1486.7 eV) source and a spherical section analyzer. The instrument has a 16 element multichannel detector. The X-ray beam used was a 100 W, 100 mm diameter beam that was rastered

over a 1.3 mm by 0.2 mm rectangle on the sample. The X-ray beam is incident normal to the sample and the photoelectron detector was at 45° off-normal. Wide scan data was collected using a pass energy of 117.4 eV. For the $Ag3d_{5/2}$ line, these conditions produce FWHM of better than 1.6 eV. The high energy resolution photoemission spectra were collected using pass energy of 23.5 eV. For the $Ag3d_{5/2}$ line, these conditions produced FWHM of better than 0.81 eV. The binding energy (BE) scale is calibrated using the $Cu2p_{3/2}$ feature at 932.62 ± 0.05 eV and Au 4f at 83.96 ± 0.05 eV for known standards.

3.4 MOS STRUCTURE FABRICATION PROCESS

1st step: *Cleaning Si wafer/surface preparation*

All Si substrates were cleaned using the regular RCA cleaning. Just right before the aluminum (Al) deposition, the Si substrate was dipped in BOE for 5 min. to remove any native oxide that could have grown after the RCA cleaning and also to create a hydrogen-terminated silicon surface. Hydrogen termination prevents the formation of SiO_2 before and during pumping down of the chamber. The Si substrate was then kept under vacuum.

2nd step: *Ohmic back contact formation*

The first step taken to fabricate the MOS capacitors was to deposit aluminum onto the back side of a silicon (Si) wafer to form an Ohmic contact with silicon. This contact is needed to make Ohmic electrical connection to the silicon. The aluminum-silicon Ohmic contact is required since the probes used for electrical measurement are metallic and will usually form a Schottky barrier if contacted directly to the silicon. In order to overcome this effect, an aluminum film is deposited on the bare Si and then annealed to ensure an Ohmic contact to the silicon. With this arrangement, the metal probes make Ohmic electrical connection to the aluminum film.

RF sputtering was chosen as the deposition method for the back contact of the MOS structures because it is more reliable, simpler and faster than thermal evaporation in our current deposition systems. The deposition conditions were as follows:

- Base pressure: 6×10^{-6} Torr.
- Deposition pressure: 10.27 mTorr.
- Ar flow: 48.9 sccm.
- Forward (fwd.) power: 120 W.
- Reflected power: 1 W.
- Deposition time: 20 min.

As-deposited aluminum makes a Schottky barrier contact with silicon; therefore an annealing step is required to convert it into an Ohmic contact. Samples in this work were annealed using halogen lamps at 450 °C under a nitrogen (N_2) atmosphere as follows **(**Figure 9**):**

- N_2 pressure: 500 mTorr.
- Temperature was raised from 32 °C to 450 °C in 5 min.
- Annealing temperature: 450 °C.
- Annealing time: 30 min.

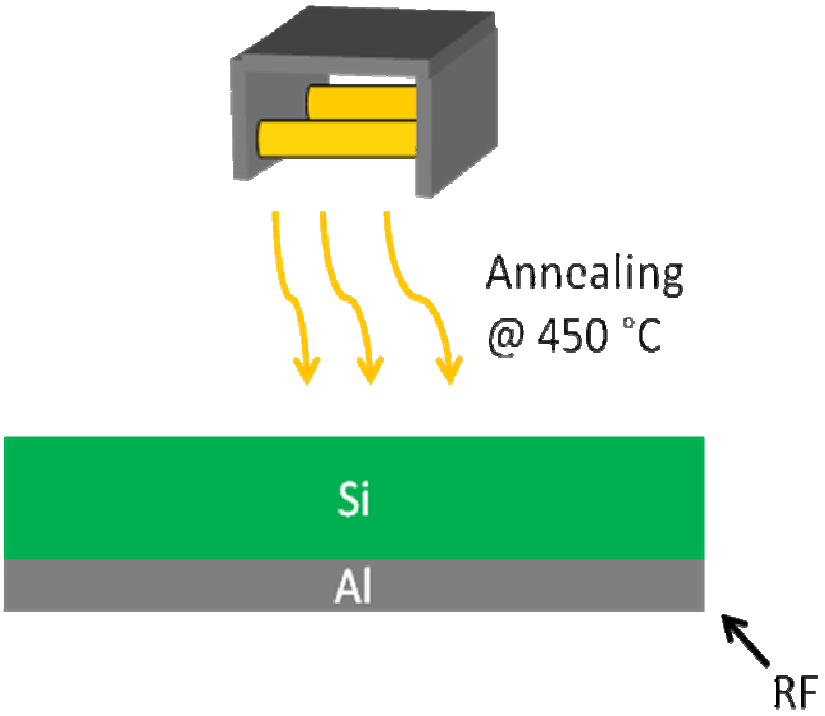

Figure 9 Illustration of Ohmic back contact formation.

Experiments were performed to determine the resistance between the Al contacts and the Si wafer. Al/Si/Al structures were fabricated under different conditions and current vs voltage (IV) measurements were made to determine the resistance. Figure 10 shows the IV curves obtained for different Ohmic contact formation conditions. Samples C6B and C8 were annealed for 30 min at 400 °C and 450 °C, respectively. The higher temperature yielded a lower resistance indicating that 450 °C is better than 400 °C. Sample C7A was also annealed at 450 °C for 30 min but in contrast received a BOE treatment immediately inserting the silicon wafer into the deposition chamber. The result was that sample C7A displayed by far the smallest resistance; approximately 4 times smaller compared to sample C8. The smaller resistance was attributed to the removal of the native oxide from the silicon surface prior to aluminum deposition.

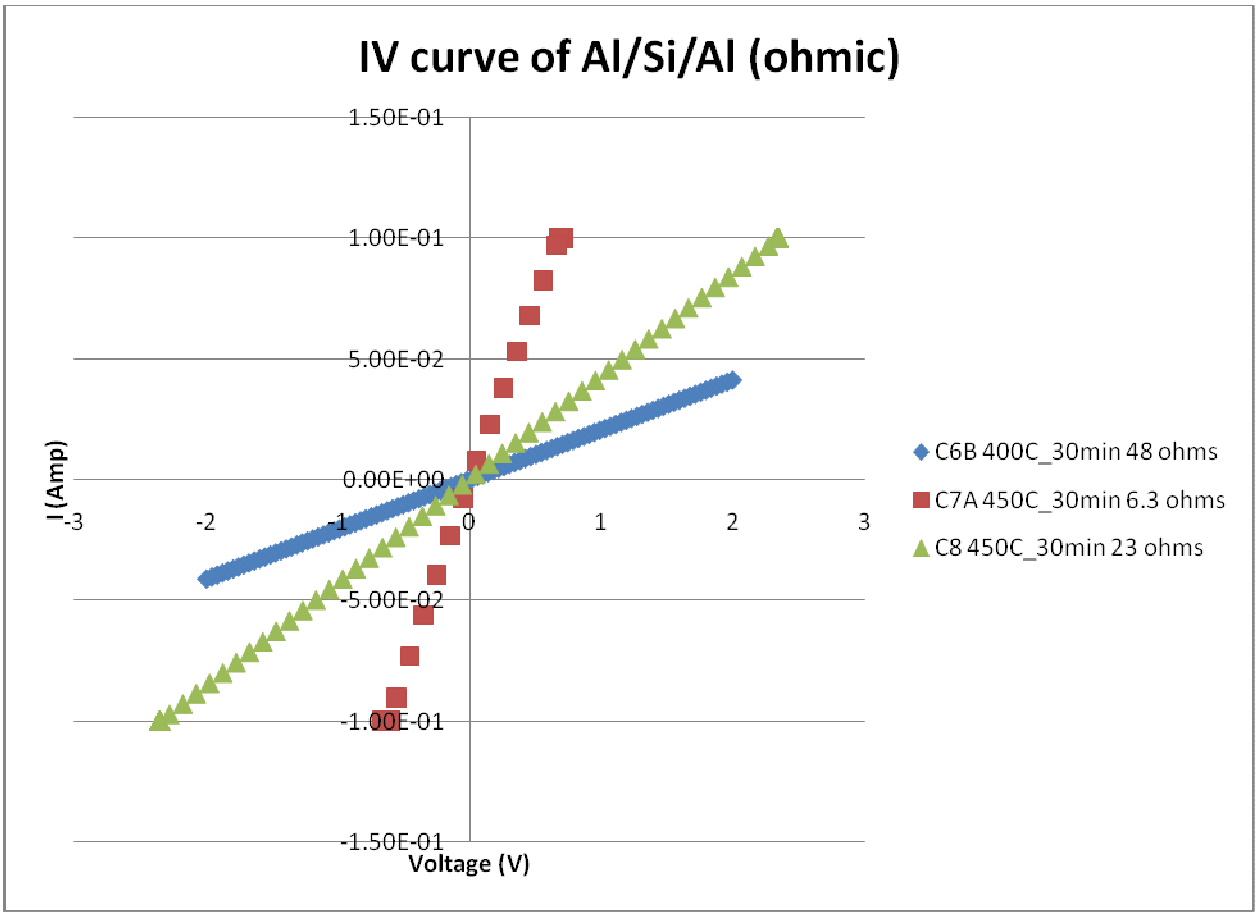

Figure 10 IV curves for three different Ohmic back contact formation conditions

3rd step: *HfO_2 thin film deposition*

After the Ohmic contact between Al and Si was formed, the wafer was cut into several pieces. HfO_2 was deposited in each piece with different thicknesses. HfO_2 depositions were performed using RF magnetron sputtering in a high vacuum deposition chamber, and the deposition conditions were as follows:

- Base pressure: 2×10^{-6} Torr.

- Dep. Pressure : 1.5 mTorr.
- Pre-dep. Annealing: temperature was raised from 50 °C to 300 °C or 400 °C in 5 min.
- Ar flow: 26.8 sccm.
- Fwd. power: 60 W.
- Reflec. Power: 0 W.
- Annealing during deposition: 300 °C and 400 °C.
- Dep. Time: change for every sample to obtain thickness variation.

A base pressure of 2×10^{-6} Torr was selected in order to have a clean ambient inside the chamber within the capabilities of the equipment. A pressure of 1.5 mTorr was selected as the sputtering pressure in order to grow films slowly, with better quality and in a reasonable amount of time. The Ar flow had to be set in order to achieve a deposition pressure of 1.5 mTorr with the size of the deposition chamber and with the current position of the high vacuum valve for conductance position. Deposition power was set to 60 W in order to grow HfO_2 films slowly and to protect the HfO_2 target from physical damages such as cracking as a result of high temperatures in the RF sputtering gun and annealing temperatures. For the samples that were deposited at temperatures above room temperature, a pre-deposition heating process was initiated consisting of incrementing the substrate temperature gradually in order to prevent substrate cracking and a uniform and correct distribution of heat across all the sample prior deposition of HfO_2.

Hafnium oxide thin films of different thickness were deposited under different temperatures to study the capacitance as a function of thickness. In order to reduce the number of variables among samples, only deposition time was changed to achieve different thickness, and all other variables such as deposition pressure, and deposition power were kept constant.

4th step: *Forming gas (FG) thermal annealing treatment*

Forming gas (FG) thermal annealing was performed on some of the HfO_2 films before the complete MOS structures were fabricated. This was done with the purpose of studying the effect of hydrogen (H_2) on trapped charges, interface charges and the overall quality of HfO_2 deposited films. A tube furnace and two gas tanks (one of UHP nitrogen and another of FG) were used. The forming gas tank consisted of 95% N_2 and 5% H_2 and a second tank of pure N_2 was used to dilute the concentration of H_2 further and prevent H_2 ignition. FG annealing treatment was performed in the tube furnace at 450 °C. The samples were placed vertically in a quartz boat and then the boat was introduced inside the furnace's quartz tube before any gas valve was opened and with the furnace turned off. Once samples were placed right at the middle point of the furnace, the quartz tube was closed using a quartz cap with a small orifice to prevent any ambient gas from coming in. The first gas valve opened at 40 sccm was the N_2 valve. N_2 was flown inside the quartz tube before the furnace was turned on in order to remove the ambient gasses from the furnace while the temperature of the heaters rose up to 450 °C. In this way, samples were kept under N_2 atmosphere and were not oxidized while the temperature set point was achieved.

When the furnace's heaters reached a temperature of 440 °C, the H_2 valve was opened and set at the same flow as the N_2 valve (40 sccm). This was done with the objective of reducing the H_2 concentration close to half (2.5%) of the percentage of the FG tank and prevent accidents. Due to restricted capabilities on the temperature controller of the furnace, temperature raised up to 460 °C. Samples were annealed for 10 min. with an average temperature of 450 °C. H_2 concentration was monitored at the orifice of the quartz cap during the annealing process and it was 3% on average.

After the 10 min. of annealing, the H_2 valve was closed and N_2 was left flowing for the entire cold down of the furnace to prevent oxidation of samples. The samples were removed from the furnace until temperature inside the furnace was 25 °C, and then they were kept under high vacuum for top contact metallization.

5th step: *Top contact metallization*

The following step after HfO_2 deposition was top contact metallization. In this step, the gate electrode of a MOS structure was deposited using thermal evaporation. Thermal evaporation was chosen for the top electrode (instead of sputtering) because this deposition technique does not affect the HfO_2 deposited layer. (In contrast, sputtering causes high energy atoms that can penetrate the oxide films.) A tungsten basket and two Al pellets are required to performed thermal evaporation of Al metal. The first groups of MOS capacitors were fabricated without a proper cleaning of the Al pellets and tungsten basket. It was discovered later that a lack of cleaning of this deposition elements constituted a source of contaminants for the top electrodes that diffused to the HfO_2 films and produced charges in the oxide that affected the electrical characteristics of the MOS capacitors. Tungsten baskets and Al pellets were cleaned with acetone, methanol and DI water (for five minutes each) using an ultrasonic cleaner. Right after cleaning the thermal evaporation deposition elements they were kept under vacuum along with the substrates. A high vacuum deposition reactor with thermal evaporation capabilities was used to deposit the top contact and the deposition conditions are described below.

- Base pressure: 2×10^{-6} Torr
- Supply current: 10 A for 3 min.
- Supply current: 15 A for 3 min
- Final supply current: 17 A

The deposition pressure was kept at $2x10^{-6}$ Torr to have a good quality deposition ambient under the capabilities of the deposition system. The supply current of the thermal evaporation power supply has to be increased gradually to prevent Al from blowing out and also to prevent physical damage of the tungsten basket such as bending or breaking.

The size of the top contact for MOS capacitors is very important because it is one of the variables that is directly proportional to the capacitance. If the area of the top contact is too big, the capacitance could increase above the capacitance limits of the CV meter. This issue actually occurred

during the first set of capacitors and therefore new stainless steel masks were designed and fabricated outside the university with smaller feature sizes. The new masks were designed rounded and with circular features arranged in a square shape. The reason behind this was to be able to place the round masks in the current substrate holder used for the high vacuum deposition systems. The diameter of the holes was set to 1.5 mm due to limitations given by the CV probe station and the equipment used to make the masks. A schematic of the actual mask used for top contact deposition is shown in Figure 11. After top contact metallization, MOS structures were ready to be tested.

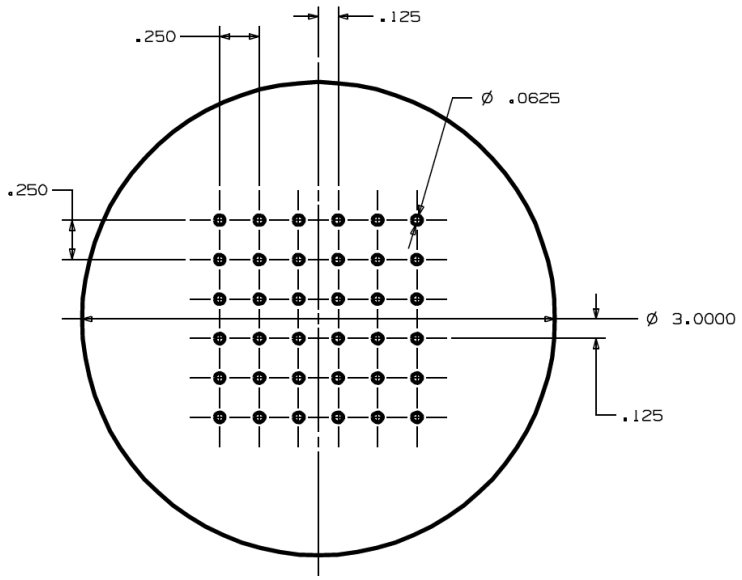

Figure 11 Schematic of the stainless steel mask used for aluminum top contact metallization

A cross-sectional representation of the MOS structures is shown in Figure 12 as well as the deposition methods used to grow each of the films.

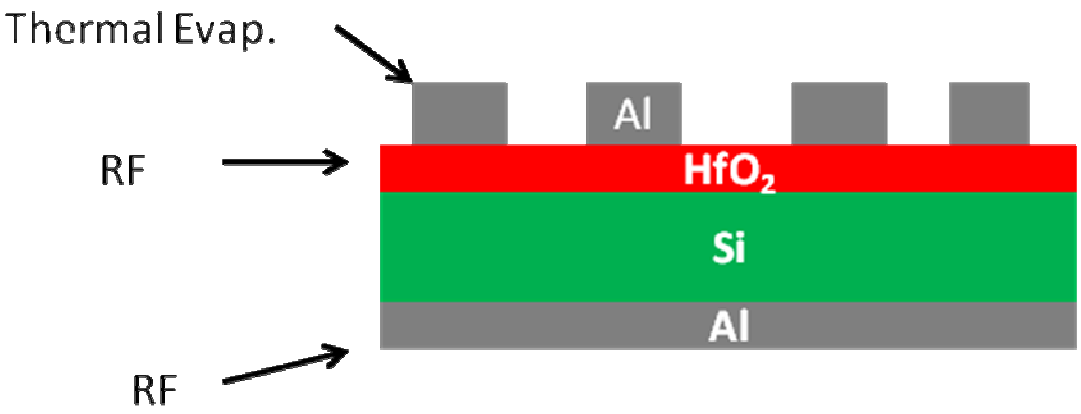

Figure 12 Representation of a complete MOS structure used to characterize electrically HfO2 films. Deposition techniques used to deposit each of the films in the MOS structures are also shown.

4. Results and Discussion

4.1 MICRO-STRUCTURAL ANALYSIS

Microstructural analysis of the sputtered deposited HfO_2 films was performed for films grown at substrate temperatures ranging (T_s) from RT to 500 °C. Film thicknesses were measured optically using a Filmetrics instrument. The range of the light's wavelengths used for thickness measurements was set from 337 nm to 850 nm. A 0.99 Goodness of fit (GOF) was achieved for each of the thickness measurements taken. X-ray diffraction (XRD), grazing incidence x-ray diffraction (GIXRD), scanning electron microscopy (SEM), energy dispersive x-ray spectroscopy (EDS) and x-ray photoelectron spectroscopy (XPS) characterization techniques were used to analyze the deposited HfO_2 thin films. Table 1 shows a summary of the thickness achieved for samples grown from room (RT) temperature to 500 °C.

Table 1 Thickness measurements for samples grown at T_s = RT – 500 °C.

Sample name	T_s (°C)	Thickness (nm)
A11	Room Temp	124
A18	200	171
A16	300	143
A10	400	149
A17	500	113

4.1.1 HfO_2 films grown at T_s = RT

Sample A11, which was grown at RT, did not exhibit any crystalline growth and it is totally amorphous. XRD spectrum (Figure 13) of the deposited film shows no peaks indicating any crystallization or orientation preference. A broad peak corresponding to (-111) planes can be seen in the XRD curve suggesting that small particles with extremely small size may be present on the film surface.

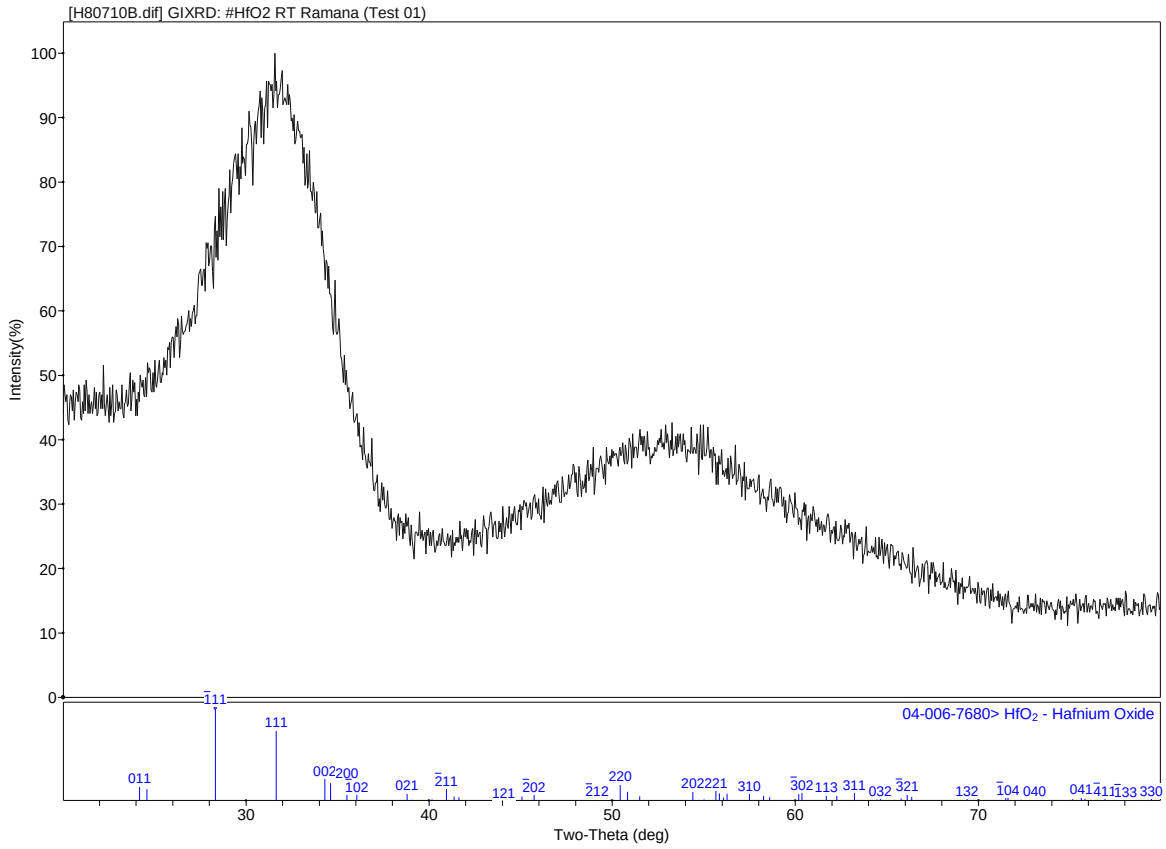

Figure 13 XRD data for sample A11 grown at T_s = RT.

SEM images from the surface reveal an amorphous surface morphology of sample A11. From Figure 14 it is clear that HfO_2 is grown randomly without a define pattern. Figure 14 correlates the results obtained from XRD in Figure 13.

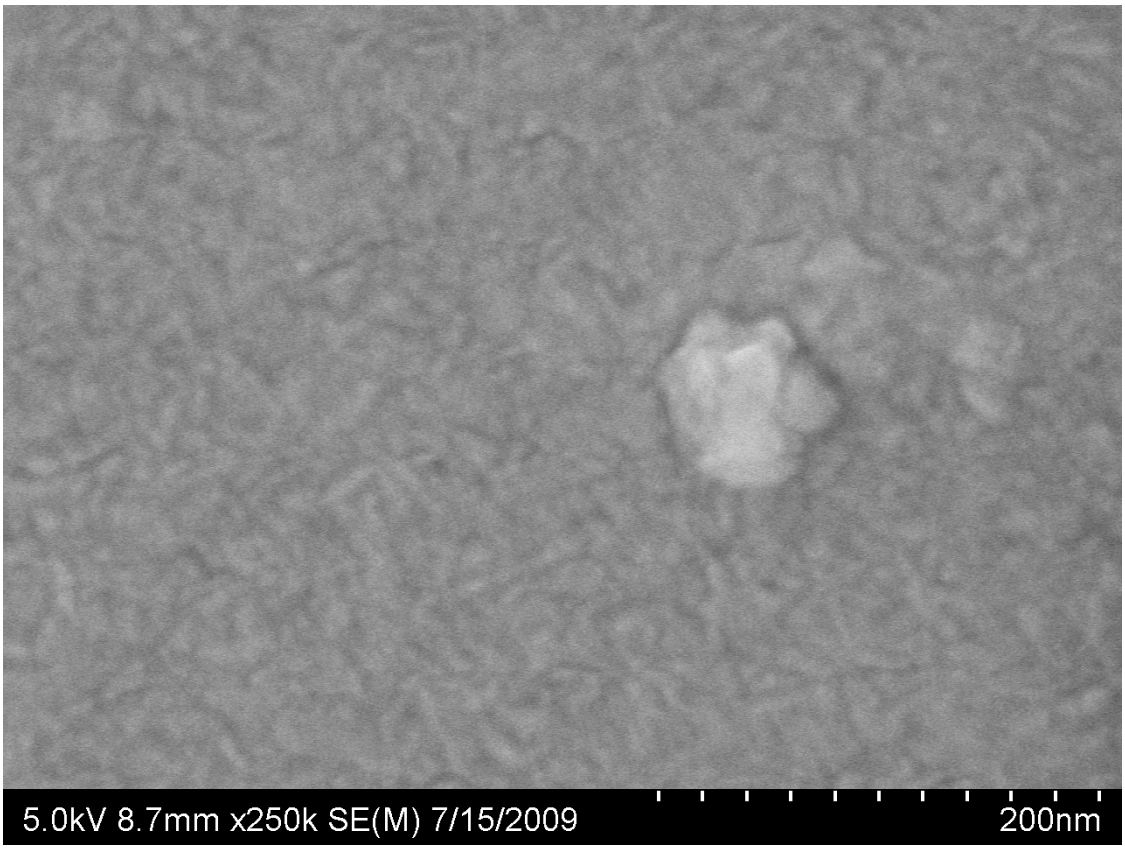

Figure 14 Surface morphology of sample A11 grown at T_s = RT.

The oxide-semiconductor interface was also studied as a function of substrate temperature. Figure 15 shows a cross-sectional image of sample A11. A sharp interface is seen between the Si substrate and the HfO_2 layer. Sample A11 was tilted a few degrees and the top part of the HfO_2 surface is imaged as shown in the micrograph. At RT there is no reaction of the Si substrate with the deposited HfO_2 film. This result was expected since no energy such as heat is being applied to activate a chemical reaction and to form compounds at the Si-HfO_2 interface. However, a totally different scenario is evident from HRSEM and XPS measurements for films grown at higher temperatures. The results are presented and discussed below.

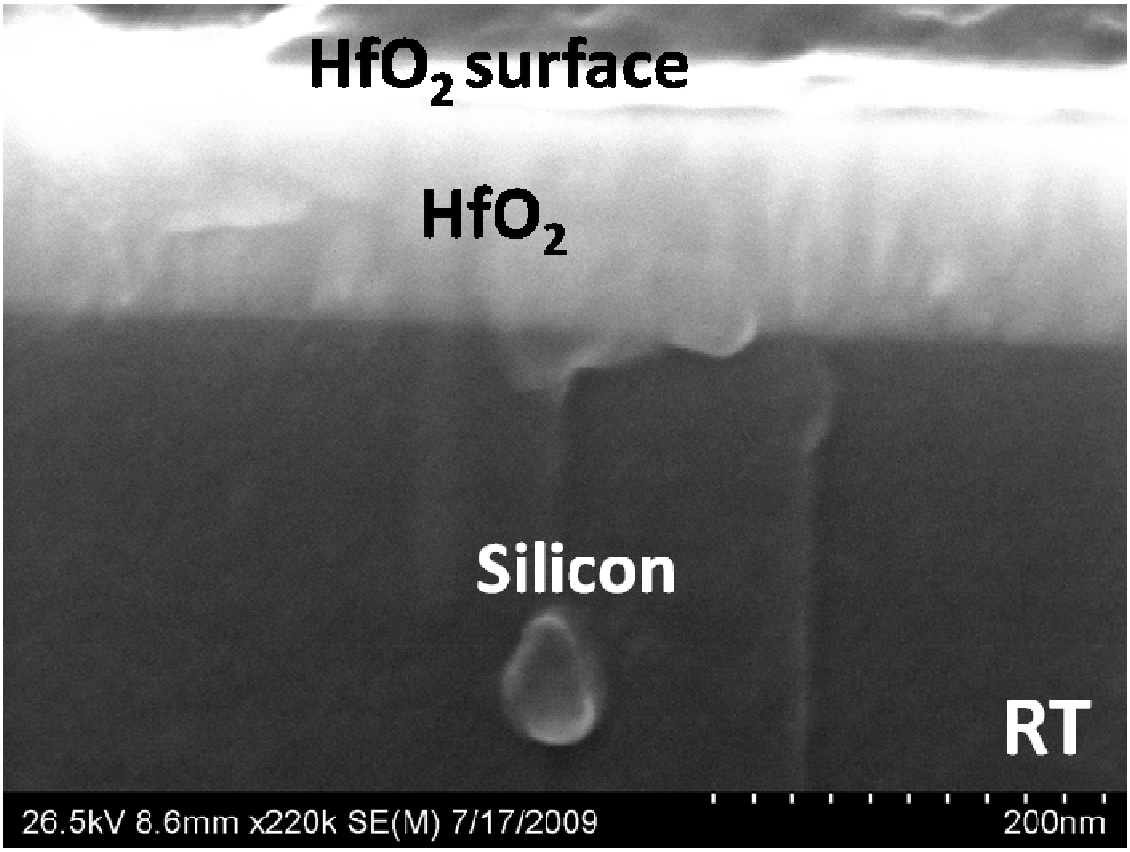

Figure 15 Cross section view of sample A11 grown at T_s = RT.

4.1.2 HfO_2 films grown at T_s = 200 °C

Sample A18 was grown at 200 °C. GIXRD data shown in Figure 16 was taken from this sample at five different fixed incident angles: 0.1 °, 0.3, ° 0.5 °, 0.7 ° and 1.0 °. The x-ray source step size was 0.06 °, and it spent 1 s/step for a total scan of 18 min. The spectrum in Figure 16 shows a small peak at 2θ = 28 ° revealing the onset of crystallization in HfO_2 film at 200 °C. It appears that, for the given set of experimental conditions, a temperature of 200 °C is favorable to provide the sufficient energy to HfO_2 film crystallization. This observation in our work is in good agreement with that reported by Aygun [30].

The other notable feature of the GIXRD pattern shown in Figure 16 is the crystal structure of the resulting HfO_2 films at 200 °C. The pattern corresponds to mocnoclinic phase of HfO_2. However, a strong peak at 2θ 28 ° indicates that the HfO_2 films have a preferred (-111) orientation. Also the crystal size is very small. Based on these observations, it is proposed that the monoclinic phase HfO_2 formation occurs at 200 °C; resulting films are nano crystalline.

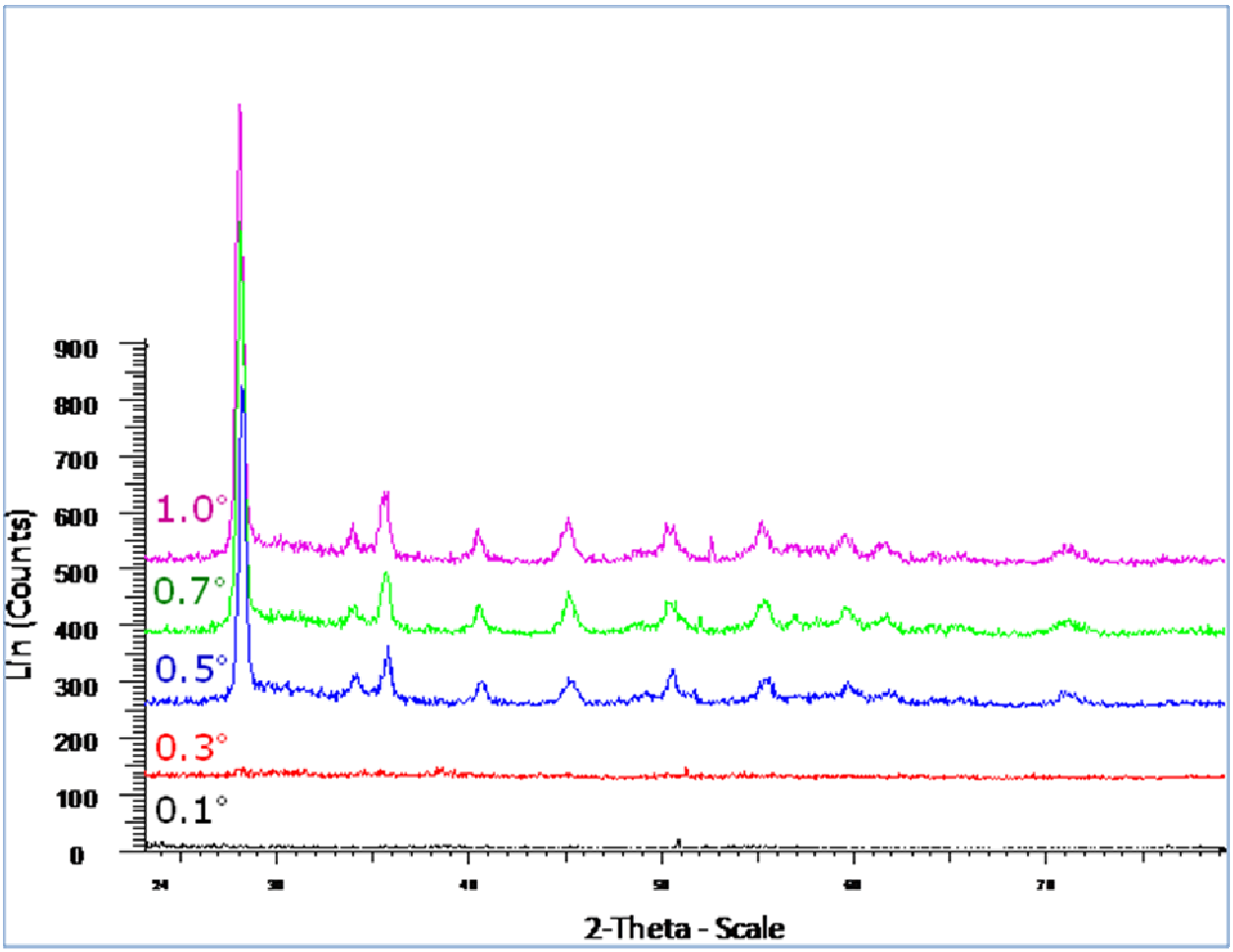

Figure 16 GIXRD data for sample A18 grown at T_s = 200 °C.

The surface morphology of sample A18 was analyzed with SEM. In Figure 17 it is clear that HfO_2 starts to grow in ordered structures of nano-crystals. This nano-crystalline structure is confirmed

with the GIXRD spectrum shown in Figure 16 with the peak at 2θ = 28 °. Combined results of GIXRD and SEM indicates that the films grown at 200 °C are nano crystalline, monoclinic HO_2 with a smooth surface morphology.

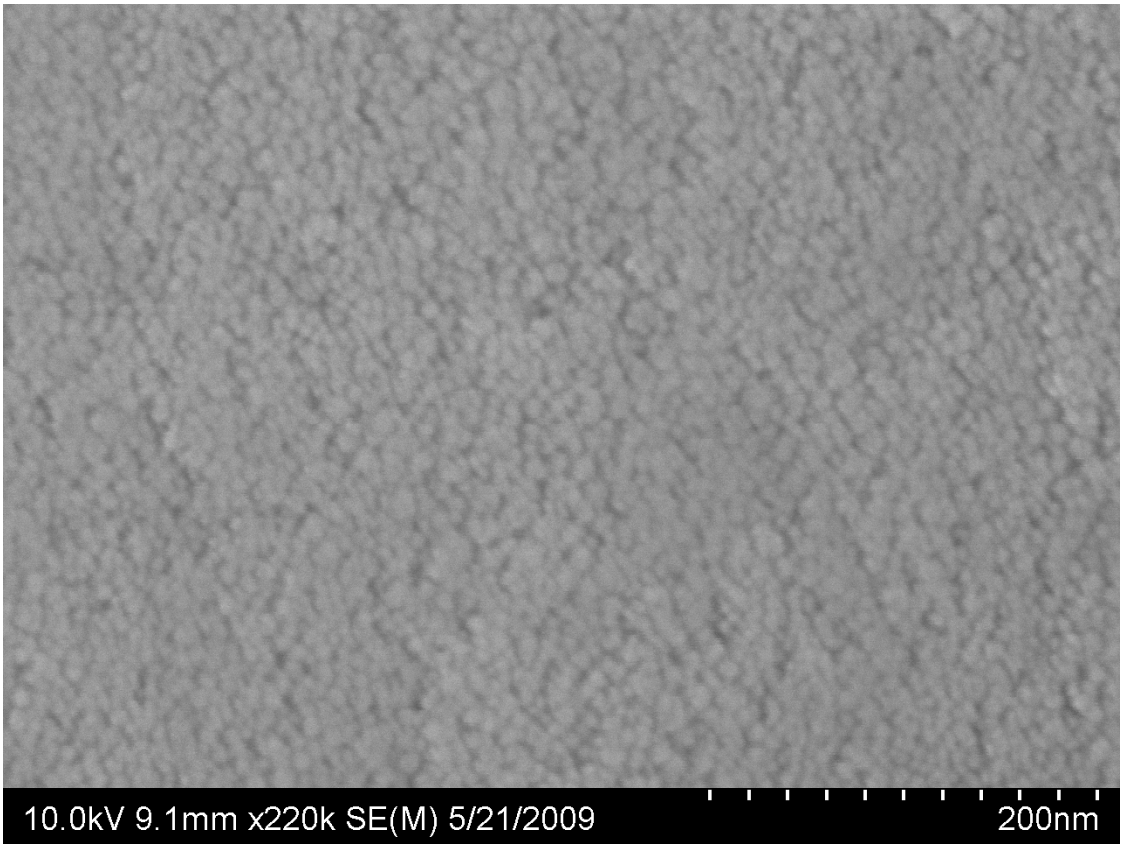

Figure 17 Surface morphology of sample A18 grown at T_s = 200 °C.

The cross section of sample A18 was also analyzed with SEM. In Figure 18 it is clearly seen that the oxide-semiconductor interface is not completely sharp and that a little interface layer of close to 10 nm starts to grow between the Si substrate and the HfO_2 layer. In Figure 18 SEM detects the difference in morphology between the HfO_2 layer and the interface layer formed due to energy provided by the 200 °C substrate temperature.

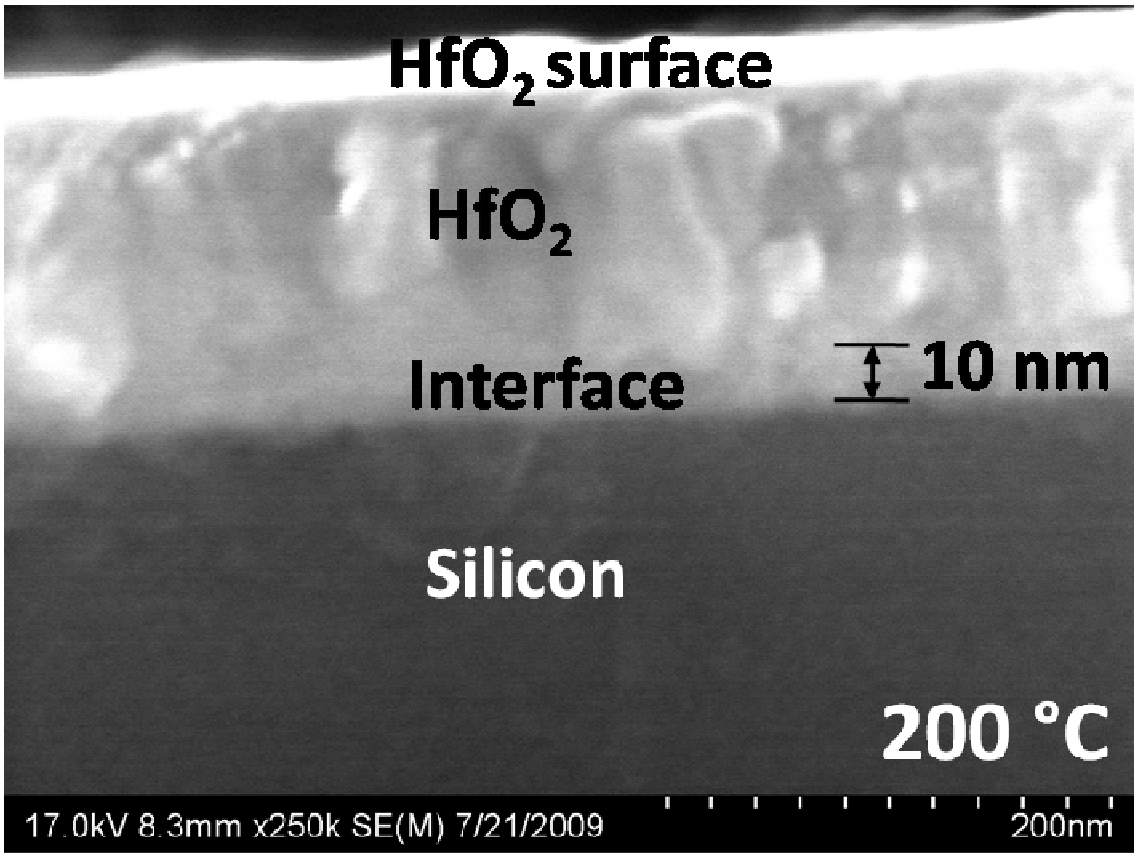

Figure 18 Cross-section view of sample A18 grown at T_s = 200 °C.

4.1.3 HfO_2 films grown at T_s = 300 °C

Sample A16 was grown at T_s = 300 °C and its microstructure was analyzed with GIXRD under the same parameters of fixed incident angle, step size and min/scan as sample A18. Figure 19 shows the GIXRD spectrum corresponding to sample A16. From this figure it is clear that HfO_2 continues crystallizing with the same monoclinic phase as in the sample grown at 200 °C because of the peak resulting in 2θ = 28 °. However in this case, the peak intensity is growing which indicates that the average crystallite size increases. In addition, it is also clear that the degree of preference orientation increases with increasing T_s.

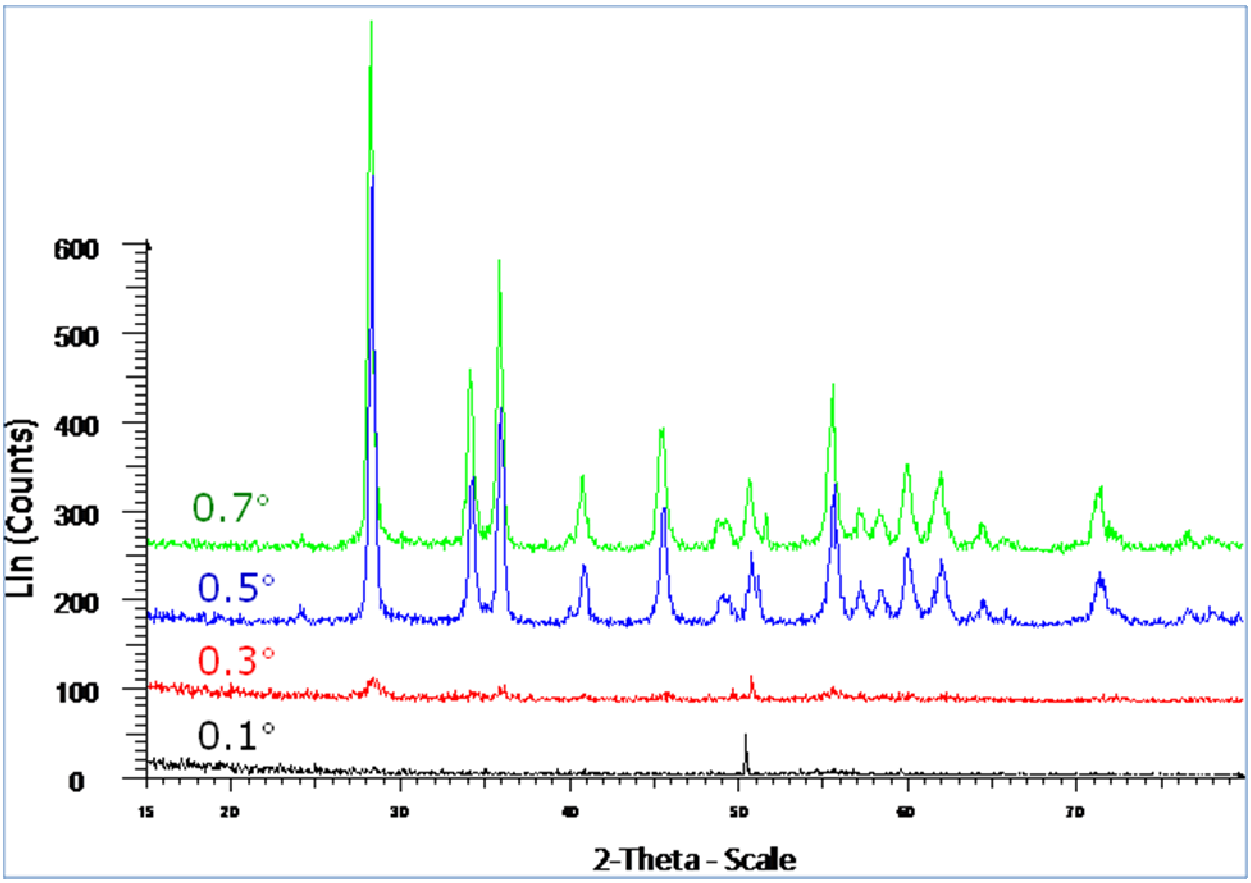

Figure 19 GIXRD data corresponding to sample A16 grown at T_s = 300 °C.

Surface morphology of the sample A16 analyzed with SEM is shown in Figure 20. It is evident that HfO_2 exhibits nano-crystals in its monoclinic phase confirmed by GIXRD data. Sample A16 is less amorphous and resembles sample A18.

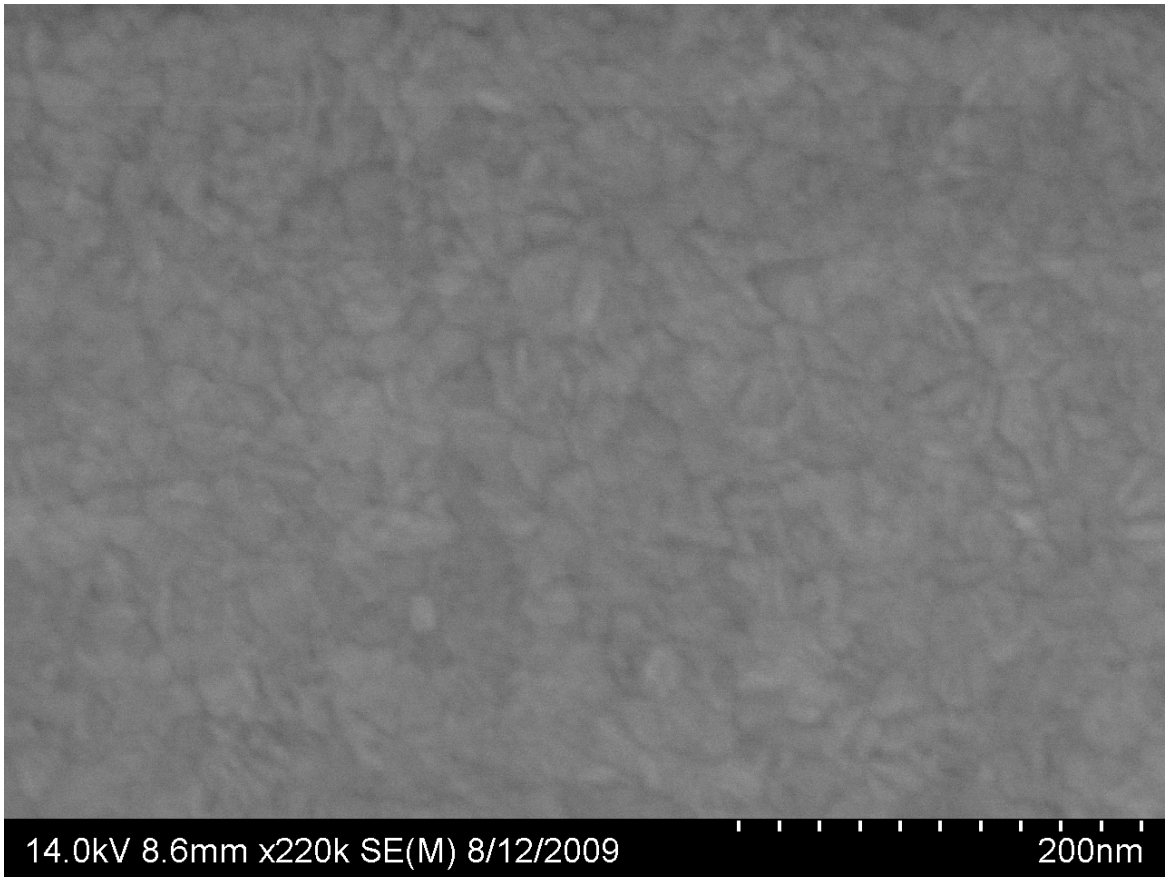

Figure 20 Surface morphology of sample A16 grown at T_s = 300 °C.

4.1.4 HfO_2 films grown at T_s = 400 °C

XRD analysis of HfO_2 thin films grown at T_s = 400 °C was performed on sample A10. XRD data shown in Figure 21 indicates that HfO_2 films grown at 400 °C are polycrystalline and exhibit a monoclinic phase with (-111) orientation. Our results regarding the crystalline structure for this sample grown at T_s = 400 °C agree with the results obtained by Li-ping Feng *et al* [17]. They also show a monoclinic phase HfO_2 with a strong peak in their XRD at 2θ = 28 ° [27].

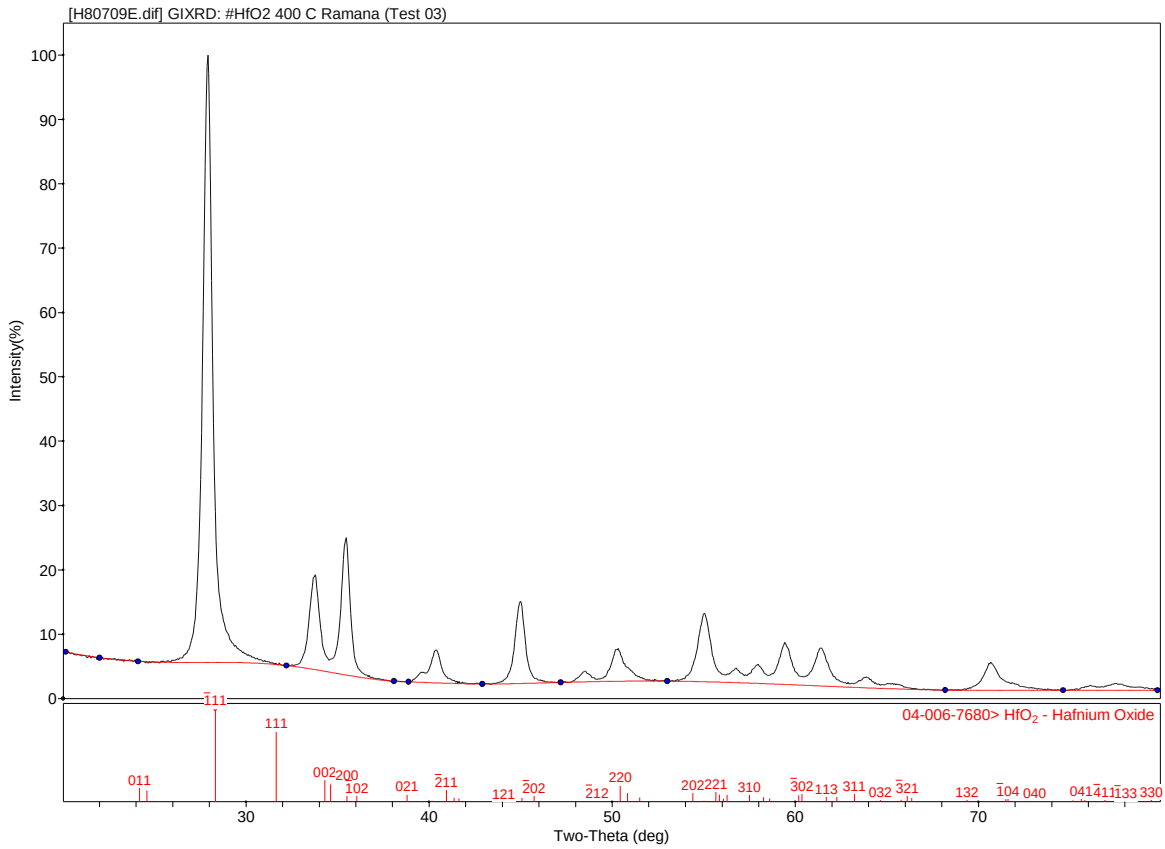

Figure 21 XRD spectrum for sample A10 grown at T_s = 400 °C.

Surface morphology of sample A10 analyzed with SEM is shown in Figure 22. The surface of this sample is crystalline and looks with better order than sample grown at room temperature.

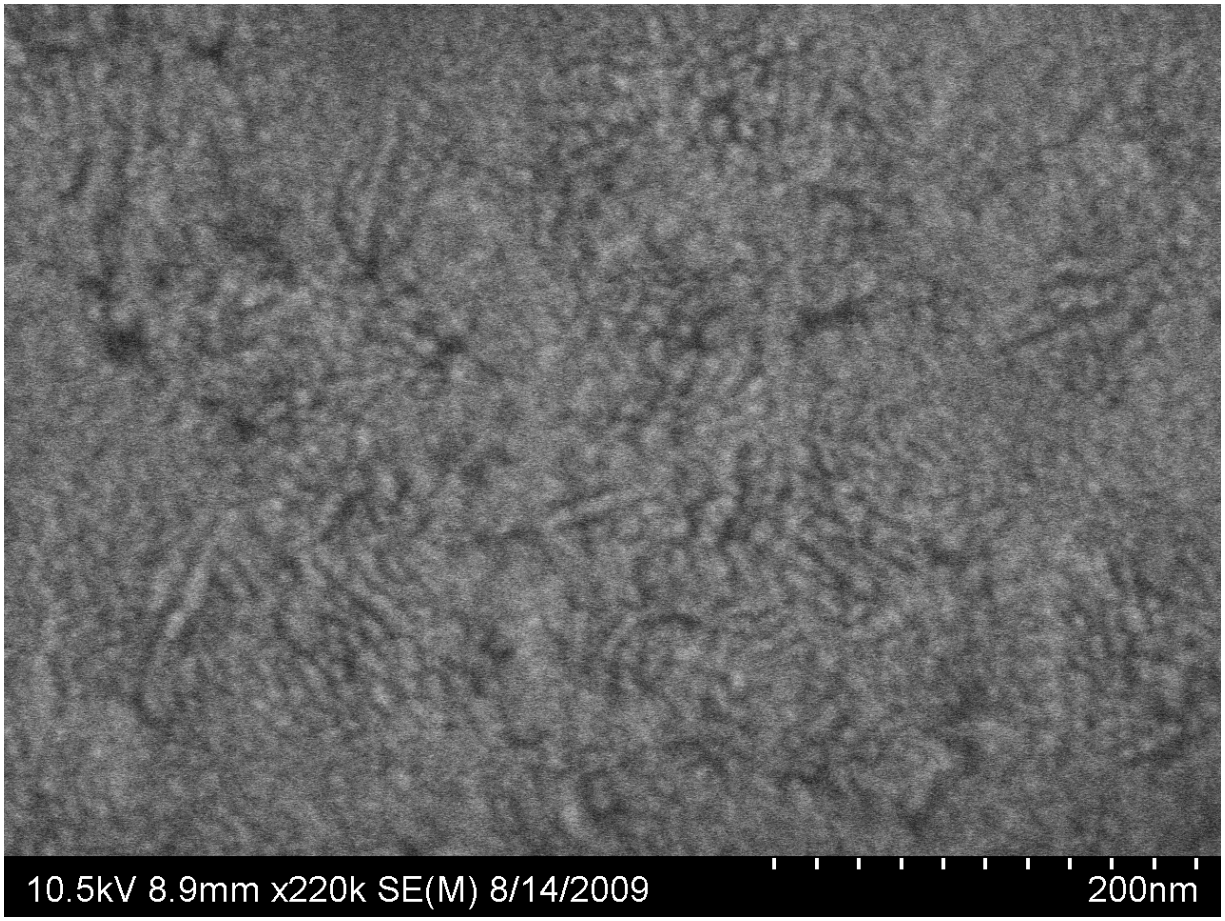

Figure 22 Surface structure of sample A10 grown at T_s = 400 °C.

Interface structure of sample A10 is displayed in Figure 23. It is clearly evident that an interface layer width is much higher at the HfO_2-Si interface. This interface is almost twice thicker as the interface of samples grown at 200 °C.

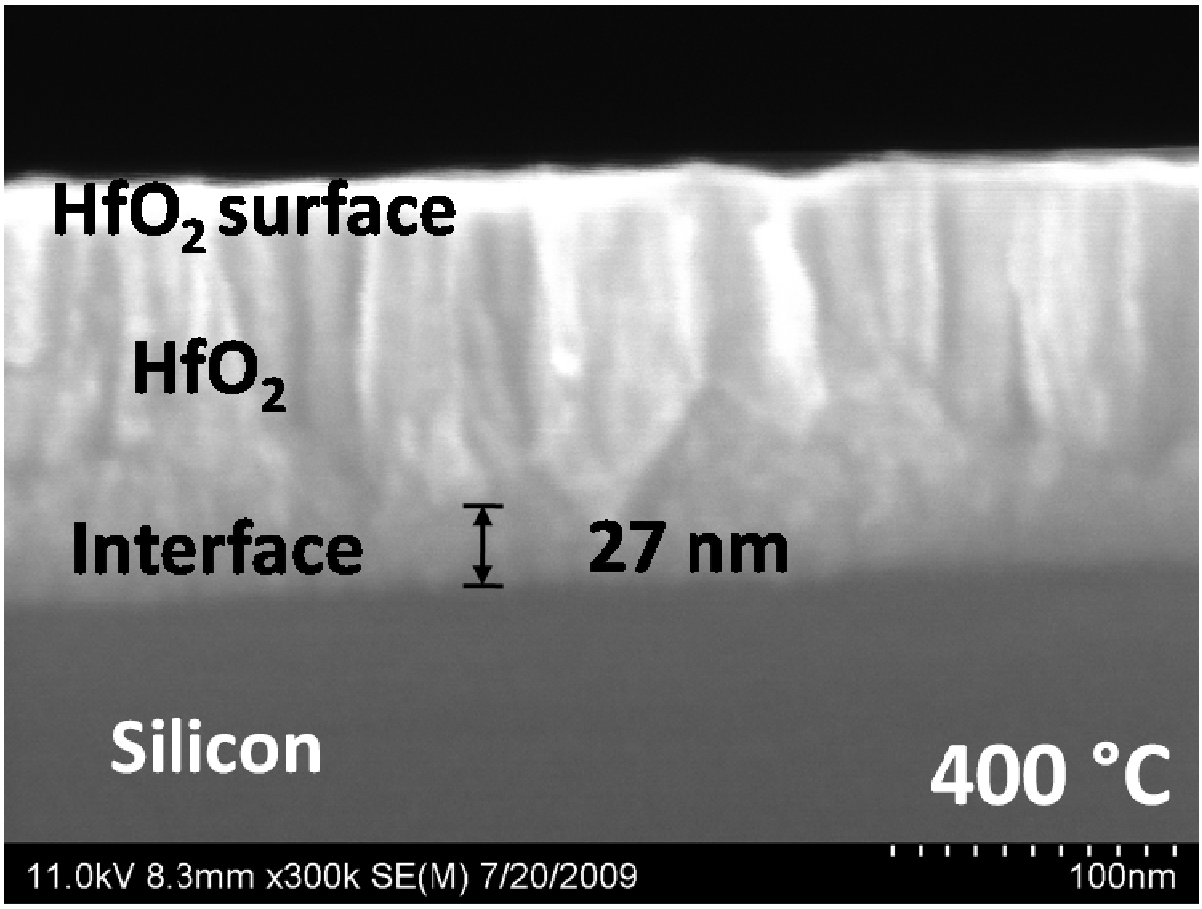

Figure 23 Cross section view of sample A10 grown at T_s = 400 °C.

The cross-section part of sample A10 was analyzed with energy dispersive X-ray spectroscopy (EDS) to find the elemental composition. The sample is positioned carefully in the SEM and the spot mode is selected in order to obtain chemical information on the substrate, film and interface film regions separately. The three layers (silicon substrate, interface layer and hafnium oxide film) are shown in Figure 23. The reasons for this are as follows: (1) the substrate is a pure Si and EDS must show only the Si contribution. (2) Similarly, the film region must be totally from Hf and O if a high-quality HfO_2 film is grown. If the elemental impurities are in the film, (i.e., segregating to the top or along the film for any reason) EDS will show their presence. (3) The most important point is that the nature and composition

of the interface layer can be determined if EDS data can be obtained from a spot within the interface layers.

The EDS spectra are shown in Figure 24. The SEM image of the cross-section (Figure 24a) and EDS curves (Figure 24b - Figure 24d) obtained from various regions are shown. The EDS curves are spot-mode and obtained from the selectively chosen area in the film, IL, and substrate, respectively. The EDS spectrum obtained from the substrate region indicates pure Si since no other elements were detected (Figure 24b). It can be seen in Figure 24c that the only contributions in the EDS spectrum for the film region of the sample are peaks due to Hf and O. The peaks labeled are Hf M and O K lines. The minor contributions from C K level are due to sample handling. On the other hand, it can be seen (Figure 24d) that the EDS curve shows contributions from Hf, O and Si from the IL region. The broad and shoulder appearance of the peak due to Hf M and Si K levels along with O K level suggests that there is a reaction between the film and substrate during HfO_2 film growth at T_s=400 °C. These results clearly suggest that the top layers are completely HfO_2 and the chemical nature of the IL is a mixture of Hf, Si and O.

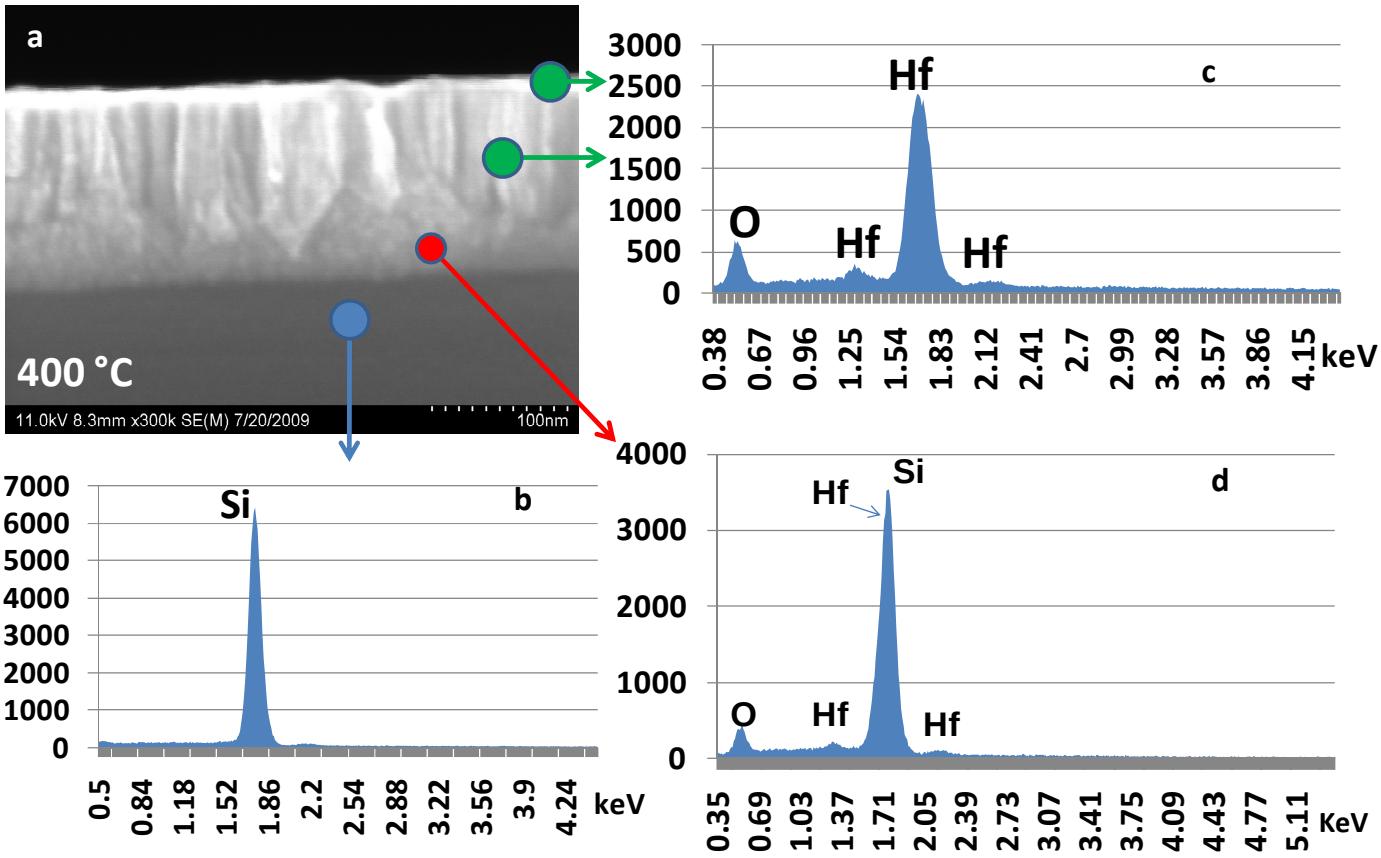

Figure 24 EDS results of the HfO_2-Si interface for HfO_2 films grown at T_s = 400 °C. The spot mode EDS curve obtained for Si-substrate, interface layer, and HfO_2 film are shown and marked as indicated by arrows. It is evident that the interfacial layer contains contributions from Hf, Si, and O atoms which iare an indication of Hf-Si-O mixed compound formation at the interface.

The XPS curve of HfO_2 films deposited at T_s=400 ^oC is shown in Figure 25 as a representative of broad survey spectra obtained. The photoemission peaks due to various elements and specific levels along with binding energy (BE) positions are as indicated in Figure 25.

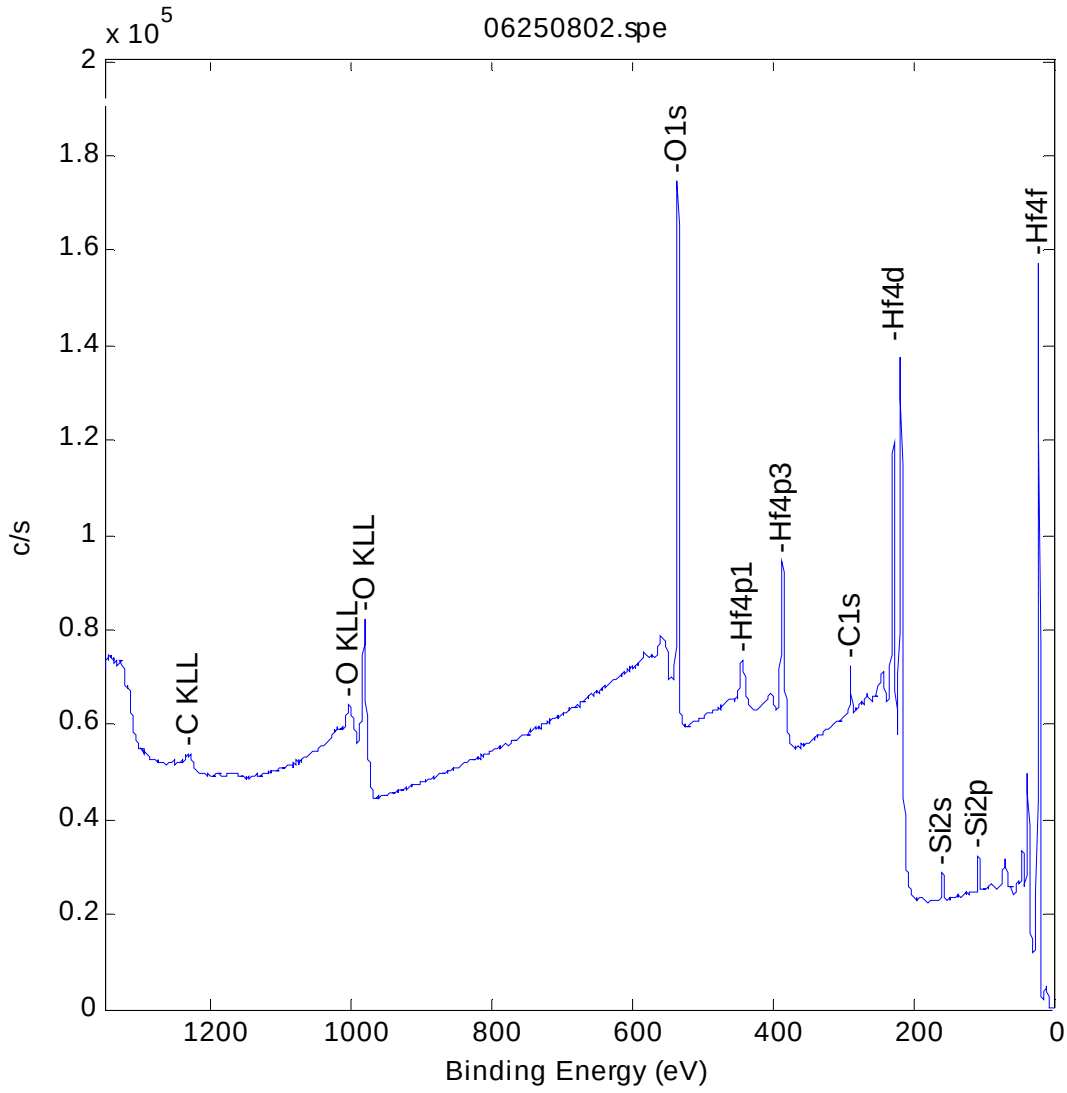

Figure 25 Representative XPS survey spectrum of a HfO_2 film grown at T_s = 400 °C. The elements detected and specific photoemission peaks are labeled at their respective binding energy positions.

The detailed core-level spectra Hf 4f, O 1s and Si 2p for HfO_2 films grown at RT and 400 ^oC are compared in Figure 26 - Figure 28. A sharp doublet corresponding to spin-orbit splitting of $4f_{5/2}$ and $4f_{7/2}$ levels is evident from the core-level spectra of Hf (Figure 26). The BE values of these two peaks are 19.5 eV and 17.1 eV, respectively. The measured BE of Hf $4f_{7/2}$ level at 17.1 eV and spin-orbit splitting energy (ΔE) of 2.4 eV are in good agreement with the literature reports for HfO_2 [31]. The Hf $4f_{7/2}$ core-level peak at a BE of 17.1 eV corresponds to Hf bonded with O to form pure HfO_2 [32].

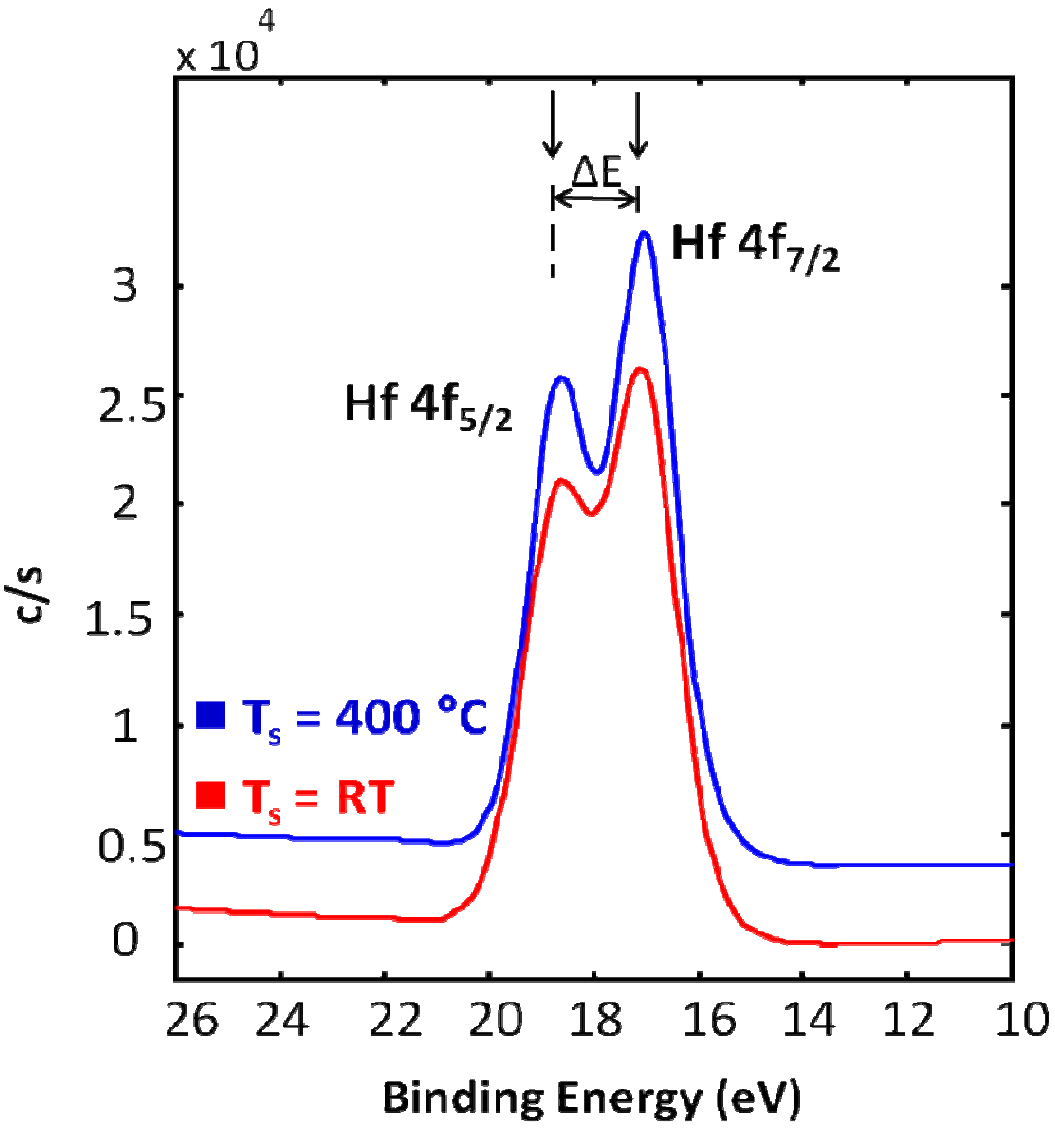

Figure 26 Core-level detailed scan of Hf 4f level. The Hf $4f_{5/2}$ and Hf $4f_{7/2}$ levels are as indicated.

The core-level photoemission spectra of O 1s level in HfO_2 films shown in Figure 27 exhibit a peak at a BE~530.4 eV. This peak is usually attributed to oxygen bonded with Hf [31]. However, a small shoulder at a BE~532 eV starts to appear for the samples grown at T_s>300 °C. The shoulder becomes prominent at T_s=400 ^{o}C. This peak or shoulder contribution at ~532 eV is attributed to the bonding of oxygen to (Hf,Si) to form a silicate [31]. On the other hand, this shoulder also can be attributed to the presence of O-H bonding if water is somehow incorporated. If OH-groups are there then

they must present for all of the HfO_2 films. Appearance of this shoulder, therefore, can only be due to (Hf,Si)-O. As it can be seen from Figure 27, the shoulder-like contribution close to 532 eV is not really a peak but it is a clear manifestation of the chemical composition of the thick IL formed for samples grown at 400 °C compared to a very thin or no IL layer formation for the sample grown at RT.

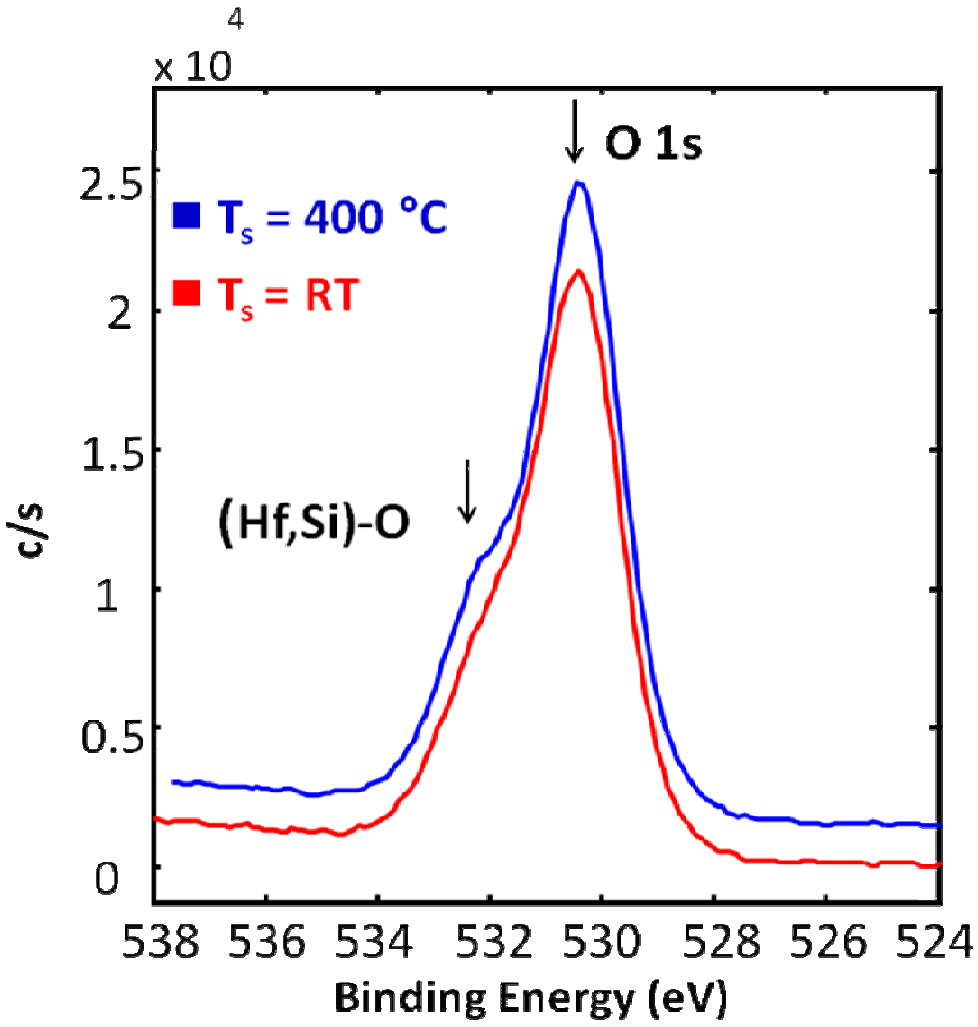

Figure 27 Core-level photoemission spectra of O 1s level. This peak at 530.4 eV is usually attributed to oxygen bonded with Hf.

The core-level photoemission spectra of Si 2p level for HfO_2 films shown in Figure 28 indicate a peak at a BE of 102.4 eV. This peak reveals Si bonded with oxygen [33]. It is evident that the peak

intensity of Si 2p is increasing when the T_s is increased to 400 ^oC. The relatively higher intensity could be due to Si in the IL when compared to almost a buried interface for T_s = RT.

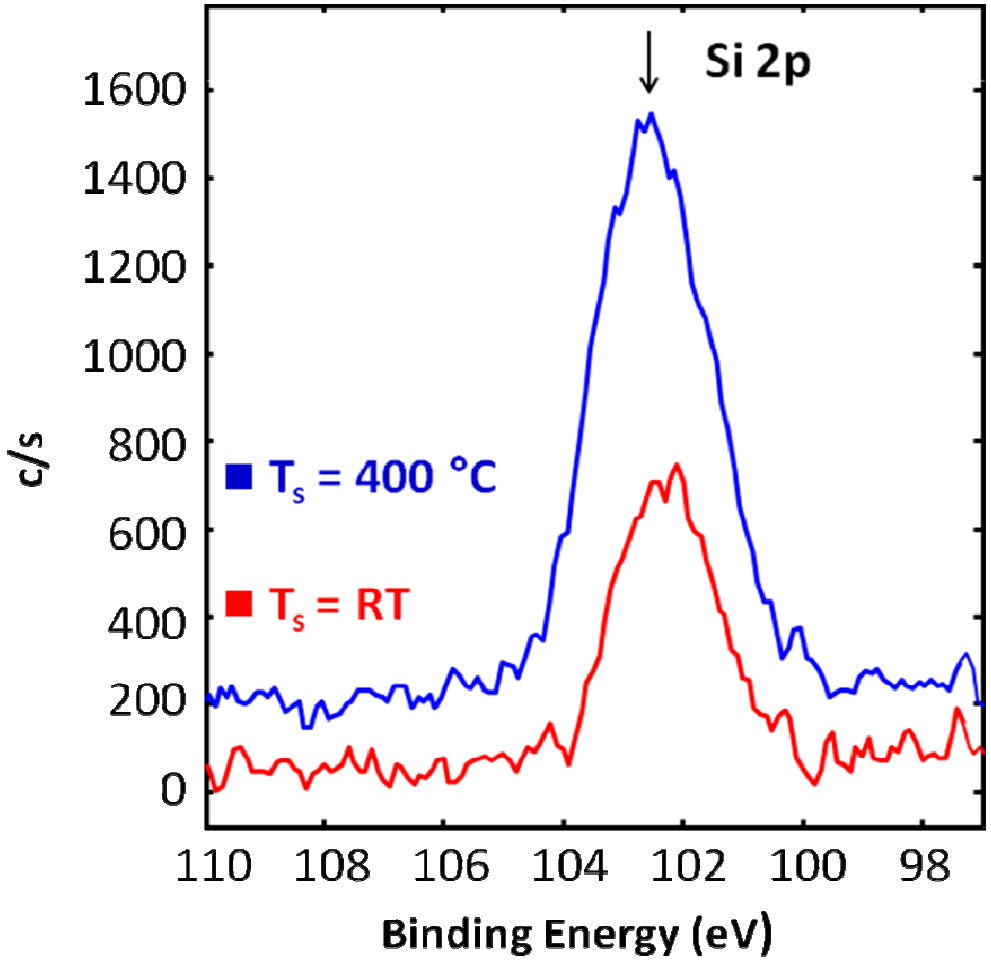

Figure 28 Core-level photoemission spectra of Si 2p level for HfO2 films. Peak at a BE ~ 102.4 eV is due to Si bonded with oxygen.

The XPS results provide a clear scenario of the temperature induced surface segregation combined with chemical mixing if we take both O 1s and Si 2p into account. Clearly, Si is not present in EDS data when the spectra we obtained in the region of HfO_2 film. However, an intensity increase in Si 2p level combined with shoulder for O 1s level suggests that small amount of Si is segregating to the surface at higher temperature (400 °C in this case). Simultaneously, a chemical reaction driven by temperature results in the formation of a (Hf,Si) O compound at the interface. If Si is buried at the interface, the photoelectrons ejected from the surface would not have shown a high intensity.

The effect of T_s is remarkable on the crystal structure and phase of HfO_2 thin films. Both the GIXRD and SEM (Figure 13and Figure 14) results indicate that the HfO_2 thin films grown at $T_s \leq 200\ ^oC$ are amorphous. Usually, if T_s is low such that the period of the atomic jump process of atoms on the substrate surface is very large, then the condensed species may stay stuck to the regions where they are landing thus leading to an amorphous film. The atom mobility on the surface increases with increasing T_s. The small, dense grains spherical in shape observed in SEM along with appearance of diffraction peaks in GIXRD clearly indicate that T_s=200 °C is the critical temperature to promote the growth of nanocrystalline, monoclinic phase HfO_2 films. For the given set of experimental conditions, a temperature of 200 °C is, therefore, favorable to provide sufficient energy for HfO_2 crystallization. This observation in our work is in good agreement with that reported by G. Aygun [30].

The GIXRD and SEM results suggest that a further increase in T_s beyond 200 °C did not result in any changes in the crystal structure; films continue crystallizing with the same monoclinic phase. However, the peak intensity of (-111) reflection is seen to be increasing which is an indicative of two characteristic features. The average crystallite-size increase with increasing T_s is the first. A preferred orientation of the films along (-111) is the second. The later feature is dominant for HfO_2 films grown at $T_s \geq 200\ ^oC$ which can be attributed to increasing degree of preferred orientation with increasing temperature. The preferred (-111) orientation of HfO_2 films can be explained based on the growth process minimizing the internal strain-energy in the film. This is due to the fact that in the crystalline materials anisotropy exists and the strain energy densities will typically be different for different crystallographic direction and the growth will favor those orientations with low strain energy density. Therefore, in the present case, it can be understood that an increase in T_s favors the preferred orientation along (-111) while minimizing the strain-energy in the HfO_2 film.

The HRSEM imaging and EDS chemical analyses (Figure 18, Figure 23 and Figure 24) indicate that the ILs formation takes between HfO_2 film and Si substrate. However, at room temperature, there is no significant reaction of the Si substrate with the deposited HfO_2 film. This result was expected since

no thermal energy is being applied to activate a chemical reaction to form compounds at the Si-HfO_2 interface. In spite of the fact that there is no clear indication of the IL at the HfO_2-Si interface in SEM images, a relatively thinner (perhaps, on the order of ~1-2 nm) IL cannot be ruled out for HfO_2 films since the resolution of the instrument is limited. The most significant feature of the SEM cross-sectional imaging is the quantitative information that can derive for ILs grown as a function of T_s. An analysis of the IL-T_s data obtained from SEM cross-sectional imaging of HfO_2-Si for HfO_2 films is presented in Figure 29. The data shows an excellent fit to an exponential growth function. The IL growth behavior, therefore, can reasonably be approximated to exhibit the temperature dependence similar to diffusion coefficient, which can be expressed as

$$IL = IL_o \exp(-\Delta E/k_B T) \qquad \{2\}$$

where ΔE is the activation energy, k_B is the Boltzmann constant, T is the absolute temperature, and IL_o is a pre-exponential factor that depends on the physical properties of the substrate-deposit. However, a direct comparison of our data with literature is not readily possible at this time since such an analysis is missing for HfO_2 films grown by other methods.

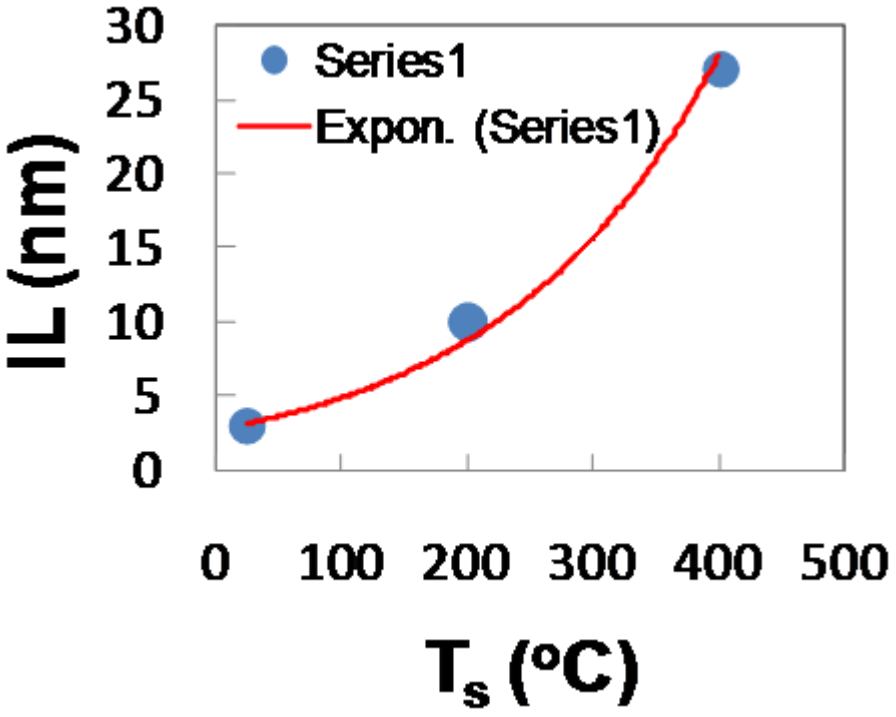

Figure 29 Analysis of IL-T_s data derived from SEM imaging measurements. The experimental data fits to an exponential function as indicated by a solid line. The data and solid line presents a simple model to represent the temperature dependence of interfacial layer growth in sputter-deposited HfO_2 films.

Having established a functional, quantitative relationship between the interfacial layer and temperature for sputter-deposited HfO_2 films, the focus now is the chemical nature of ILs. The imaging and chemical analysis data presented in Figure 24 provides first-hand qualitative information on the chemical nature of ILs. It is clearly seen in the images that the interface is amorphous showing x-ray emissions from Hf, Si and O which indicates that the IL is a Hf-Si-O mixed compound. Based on the phase diagram of Hf-Si-O, and since the temperatures in the present case are not very high, we attribute the IL as a compound of Hf-silicate ($HfSiO_4$). The results are in fact very close to this composition and in agreement with the results of Kirsch et. al. [29] The additional evidence for (Hf,Si)–O compound formation at increasing T_s is seen in XPS.

The measured BE of Hf $4f_{7/2}$ photoemission peak at 17.1 eV, ΔE~2.4 eV and O 1s core-level BE at 530.4 eV characterizes the grown films as stoichimetric HfO_2. All the Hf ions in the grown films exist

in their highest oxidation state of Hf^{4+}. The most important two factors that accounts for the nature of ILs at the HfO_2-Si interface are the following. The shoulder at a BE~532 eV in the core-level scan of O 1s is the first. An increase in the intensity of Si 2p photoemission peak at a BE of 102.4 eV with increasing T_s is the second. The later feature is a clear manifestation of the interfacial reaction of Si with the growing film. This peak or shoulder contribution at ~532 eV is attributed to the bonding of oxygen to (Hf,Si) to form a silicate. A reduced intensity for Si 2p photoemission peak, the complete absence of shoulder component, and no IL detected in SEM cross-section imaging is direct evidence that there is no interfacial reaction or very restricted reaction for HfO_2 films grown at RT. The Si substrate surface buried at the HfO_2-Si interface accounts for the decreased intensity in Si 2p photoemission peak. However, for the HfO_2 film depositions at higher T_s with the same time and thickness, the IL formation takes place. The thickness of ILs extends into several nanometers, as is evident in SEM images and data presented in Figure 29, into the HfO_2 film. As a result, the Si atoms present all along these ILs will enhance the Si 2p peak intensity in the XPS curves. Since the reaction is taking place between the growing HfO_2 film and Si substrate, the bonding in ILs are mainly between Hf, Si and O and, therefore, a shoulder corresponding to (Hf,Si)-O or silicate results into a shoulder. It is seen that the shoulder becomes prominent at T_s=400 ^{o}C. Furthermore, the EDS results also confirm that the contributions from ILs are due to Hf, Si and O atoms and the composition is nearly $HfSiO_4$. Thus, based in both EDS and XPS results, it can be concluded that the chemical nature of ILs in this case is Hf-silicate, which is $HfSiO_4$.

4.1.5 HfO_2 films grown at T_s = 500 °C

Sample A17 was grown at T_s = 500 °C and its crystalline structure was analyzed with GIXRD as shown in Figure 30. The GIXRD spectrum shows that sample A17 has a very ordered structure since the peak at 2θ = 28 ° is very pronounced with respect the rest of the spectrum. This peak corresponds to

the monoclinic phase of HfO_2 with orientation (-111) similar to the samples grown at lower substrate temperatures. The scanning conditions and detector positions to capture GIXRD data were the same used previously for samples A16 and A18.

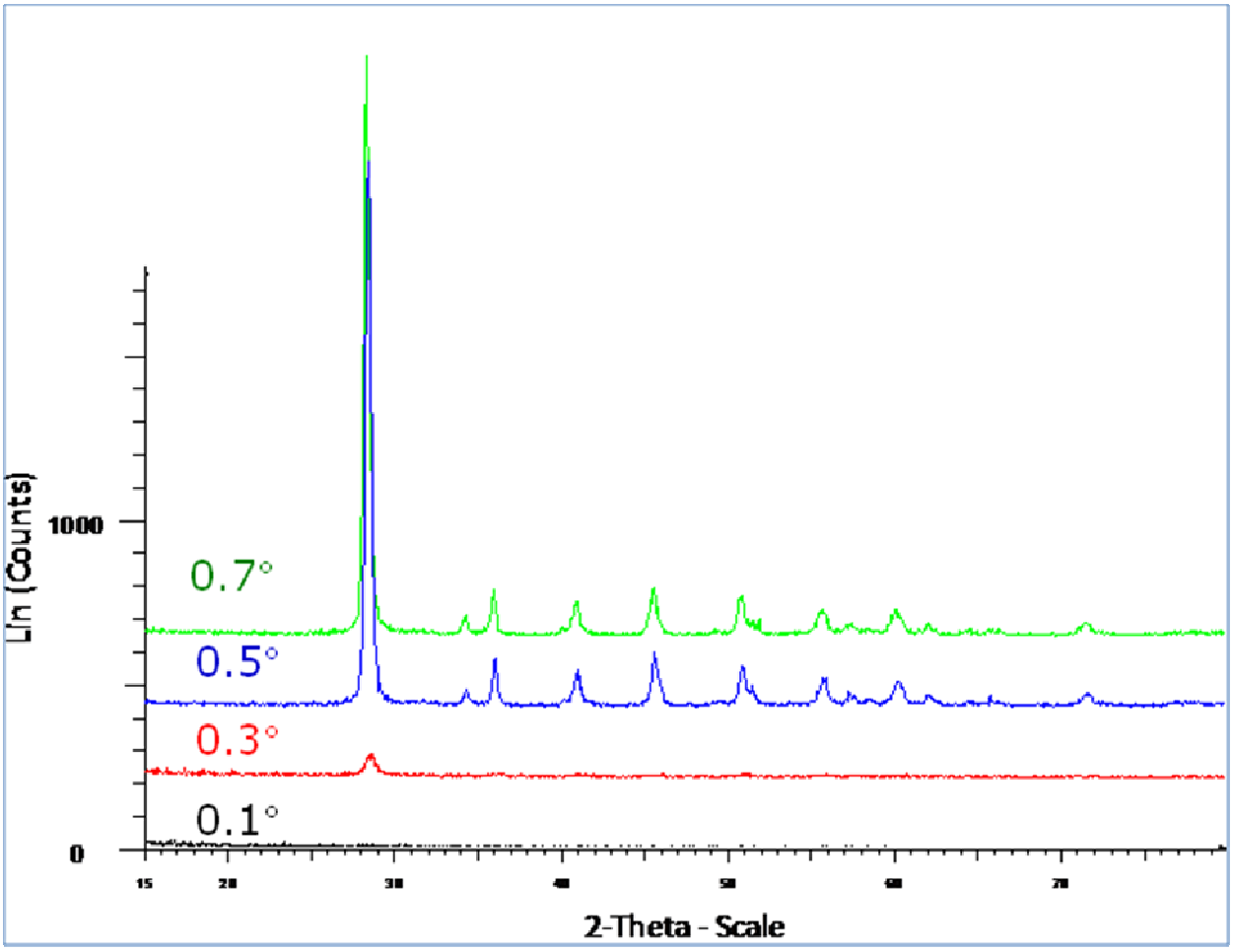

Figure 30 GIXRD spectrum for sample A17 grown at T_s = 500 °C.

Surface morphology was analyzed with SEM as with the previous samples. Figure 31 shows an SEM picture of the HfO_2 surface in which it can be seen that HfO_2 has grown with better order and crystalline structure.

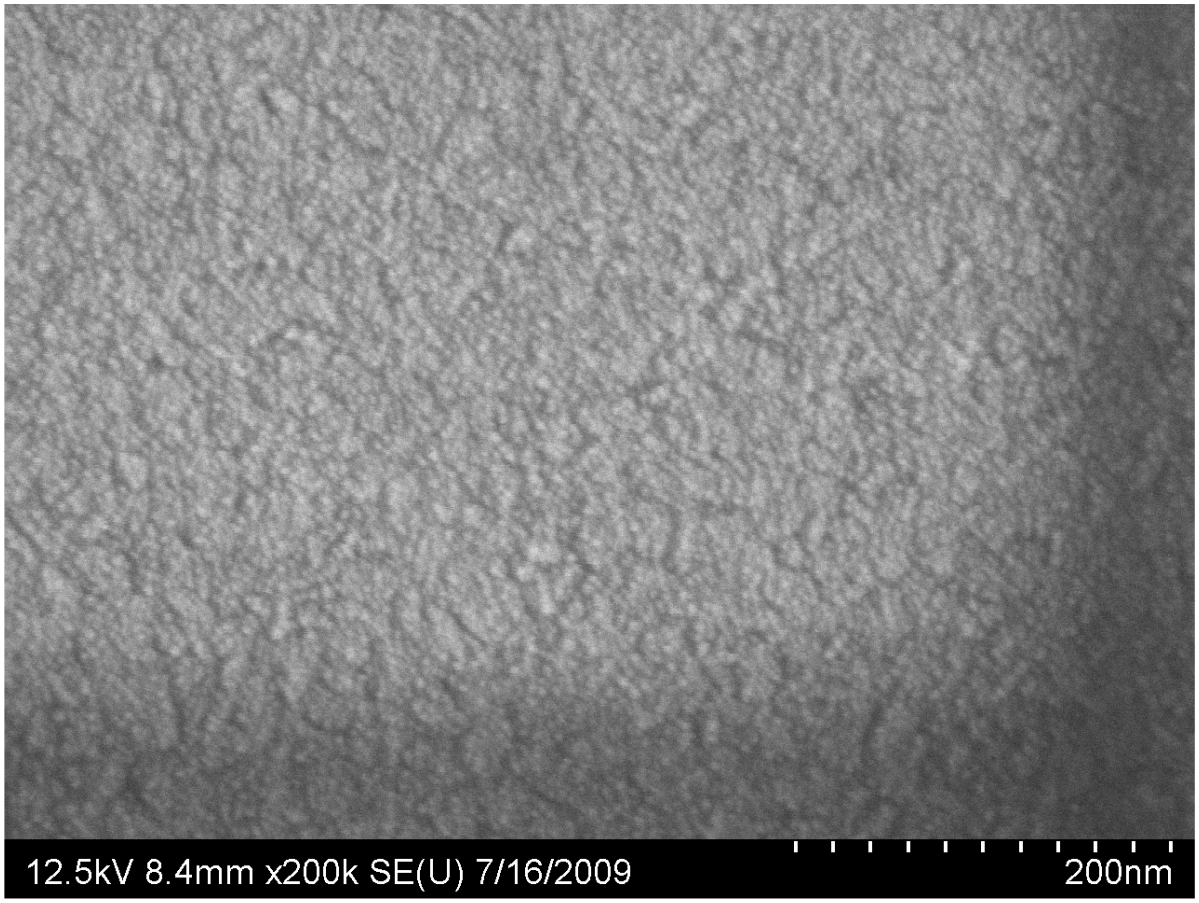

Figure 31 Surface morphology of sample A17 grown at T_s = 500 °C.

A comparison chart of GIXRD data for samples grown at 200 °C, 300 °C and 400 °C is shown in Figure 32. This figure shows the evolution in crystallization of the films deposited under different temperature. Sample A17 has the most pronounced peak (with highest substrate temperature) indicating better ordered films and sample A18 has the smallest peak (with the smallest substrate temperature) among the three compared samples.

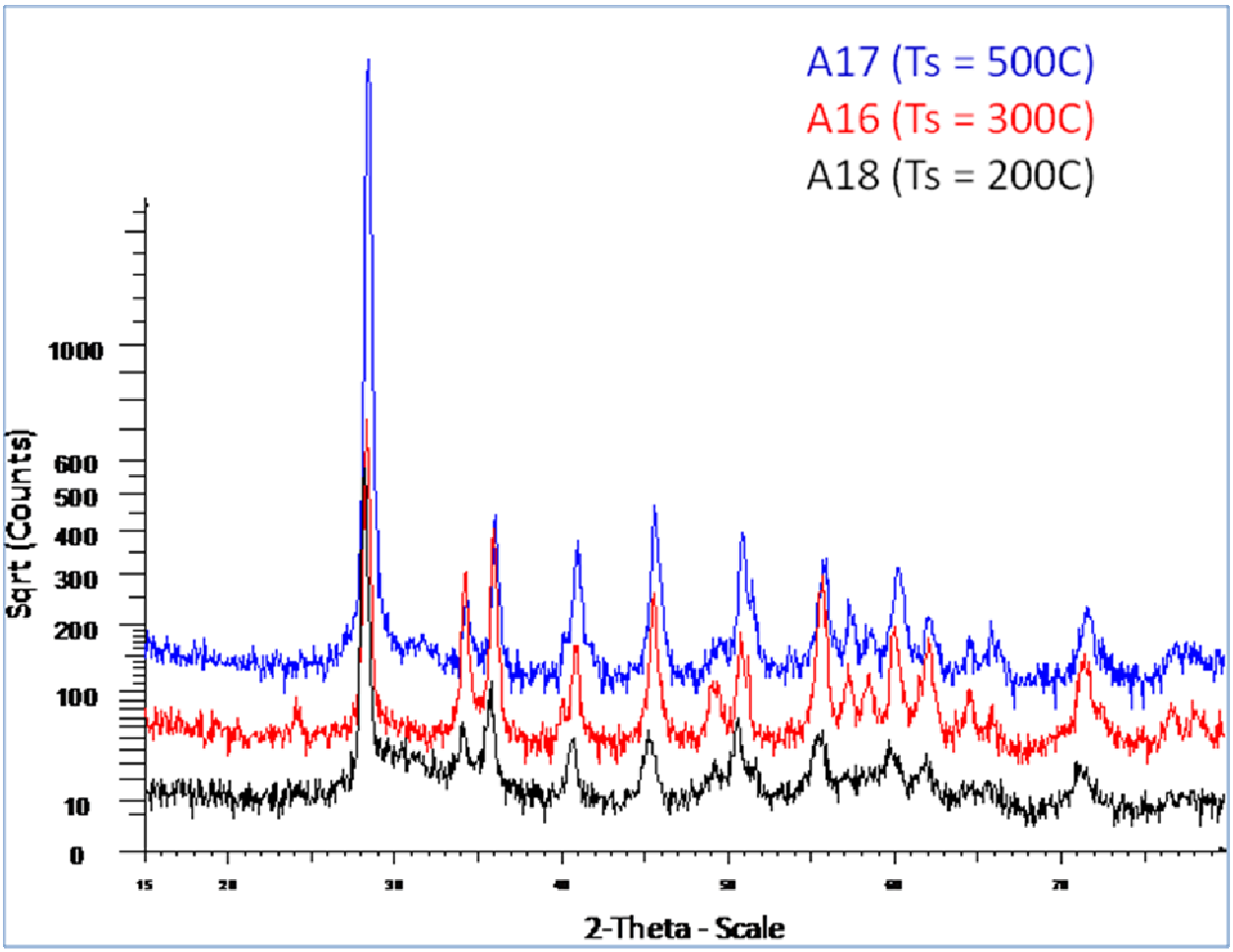

Figure 32 GIXRD comparison for samples A17, A16 and A18 grown at T_s = 500 °C, 300 °C and 200 °C respectively.

A comparison of the interface layers as a function of substrate temperature indicates that the thickness of the interfacial layer grows as the T_s is increased.

4.2 ELECTRICAL ANALYSIS

4.2.1 Electrical analysis of HfO_2 films grown at T_s = 400 °C

HfO_2 thin films with different thicknesses were deposited at T_s = 400 °C. Deposition time was changed in each deposition to achieve HfO_2 films with different thicknesses. Also, the effect of post-deposition annealing on oxide charges was studied for this set of samples. Right after each HfO_2 deposition, film thicknesses were measured with a filmetrics instrument and goodness of fit of 0.99 was achieved for each measurement.

Table **2** shows a brief summary of the thickness achieved for each of the films.

Table 2 Shows the thickness variation for each sample grown at T_s = 400 °C.

Sample name	t_{ox} (nm)
C16	258
C15	160
C18	65
C17	206*

*Plus 10 min. post-deposition annealing.

Right after film thickness measurements, samples were placed under vacuum for top contact deposition. As mentioned previously, top contact deposition was the last step in making MOS capacitors. In order to characterize the MOS capacitors, C-V measurements were made using a Boonton 7200 capacitance meter. This capacitance meter uses a 1 MHz signal to measure capacitance; therefore, only the high frequency response of MOS structures was obtained with this instrument. The Boonton 7200 is capable to measure capacitance in a range of 0 pF -2000 pF; however, the high limit was extended up to 3759 pF by calibrating the instrument with an external capacitor. The capacitance value

obtained from the instrument was divided by the area of the top contact for each of the MOS structures fabricated in order to calculate capacitance density.

It is important to note that the total capacitance (C_T) of the MOS capacitors fabricated in this work depends on three different capacitances connected in series as shown by the following formula:

$$C_T = \frac{1}{\frac{1}{C_{HfO_2}} + \frac{1}{C_{IL}} + \frac{1}{C_{SC}}}$$

Where:

C_{HfO_2} = Capacitance given by the HfO_2 layer.

C_{IL} = Capacitance given by the interface layer.

C_{sc} =Capacitance given by the semiconductor depletion width.

Depending on the bias applied to the MOS capacitor one of the three capacitances (the smaller one) dominates over the other ones. For example, when a positive bias is applied to a p-type MOS capacitor, the majority carriers (holes) of the semiconductor located below the oxide layer are repelled and as a consequence, a depletion width is created with a very low capacitance (C_{sc}). This capacitance dominates at positive voltages giving as a result the inversion region in a C-V plot. On the other hand, when negative bias is applied to a p-type MOS capacitor that has an interface layer between the gate oxide and the semiconductor, the total capacitance is a result of the capacitance series combination between C_{HfO2} and C_{IL}. For this bias condition, the width of the depletion layer in the semiconductor is zero, giving as a result $C_{sc} = \infty$ and as a consequence, $\frac{1}{C_{sc}} = 0$. Since the dielectric constant of the interface layer formed between HfO_2 and Si is usually smaller than the HfO_2 dielectric constant, the overall capacitance of the MOS structure is lowered when an interface layer is present.

C-V curves obtained for HfO_2 films deposited at 400 °C are shown in Figure 33. As it was mentioned above, capacitance in the accumulation region (C_{ox}) is the series combination of C_{HfO2} and C_{IL} (capacitance proportional to the IL shown in SEM data previously). It is clear that the oxide capacitance decreases with increasing oxide thickness, t_{ox}.

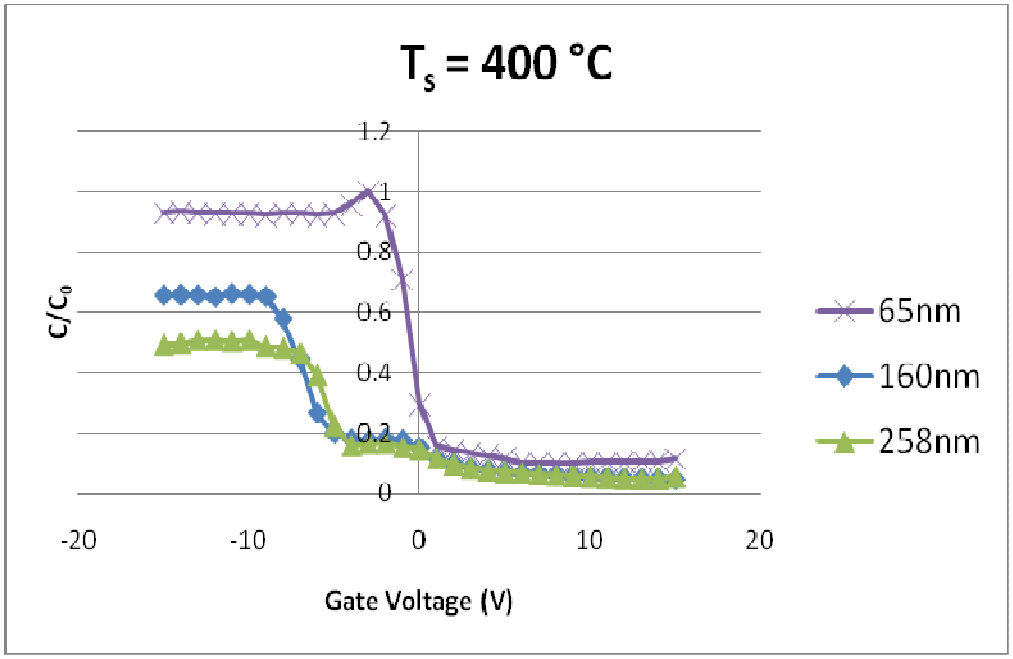

Figure 33 Shows the C-V response of the MOS structures with HfO_2 grown with T_s = 400 °C.

4.2.2 Electrical analysis of HfO_2 films grown at T_s = 300 °C

HfO_2 thin films with different thicknesses were also deposited at T_s = 300 °C. As before, the deposition time was changed in each deposition to achieve HfO_2 films with different thicknesses. Right after each HfO_2 deposition, films thicknesses were measured with a filmetrics instrument and goodness of fit of 0.99 was achieved for each measurement. Table 3 shows a brief summary of the thickness achieved for each of the HfO_2 films deposited at 300 °C. The C-V curves obtained for each of the MOS structures are shown in Figure 34.

Table 3 **Shows three different HfO_2 thicknesses achieved at T_s = 300 °C under different deposition times.**

Sample name	Dep. Time	t_{ox} (nm)
C27	19min.	56
C25	30min.	147
C24	45min.	178

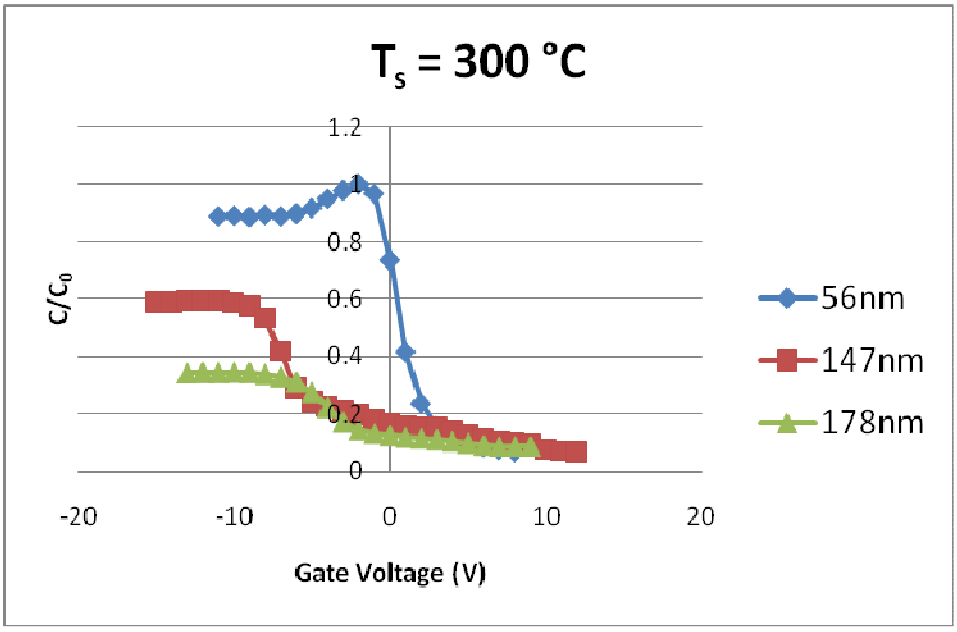

Figure 34 C-V curves of MOS structures with HfO_2 grown at T_s = 300 °C.

From Figure 34 it is clearly seen that capacitance at accumulation varies inversely proportional to the oxide thickness as expected. From the samples grown at T_s = 300 °C the thinner sample (56 nm) exhibits the higher capacitance and the thicker sample (178nm) exhibits the smaller capacitance.

4.2.3 Electrical analysis of HfO_2 films grow at T_s = RT

HfO_2 thin films with different thicknesses were deposited at RT. Deposition time was changed in each deposition to achieve HfO_2 films with different thicknesses. Table 4 shows a brief summary of the thickness achieved for each of the HfO_2 films grown at RT.

Table 4 Shows the different thickness obtained at T_s = RT during different deposition times.

Sample name	Dep. Time	t_{ox} (nm)
C19	7.5min.	65
C23	15min.	114
C22	30min.	213

MOS capacitors were also fabricated with the oxides deposited at RT. The C-V curves obtained are shown in Figure 35.

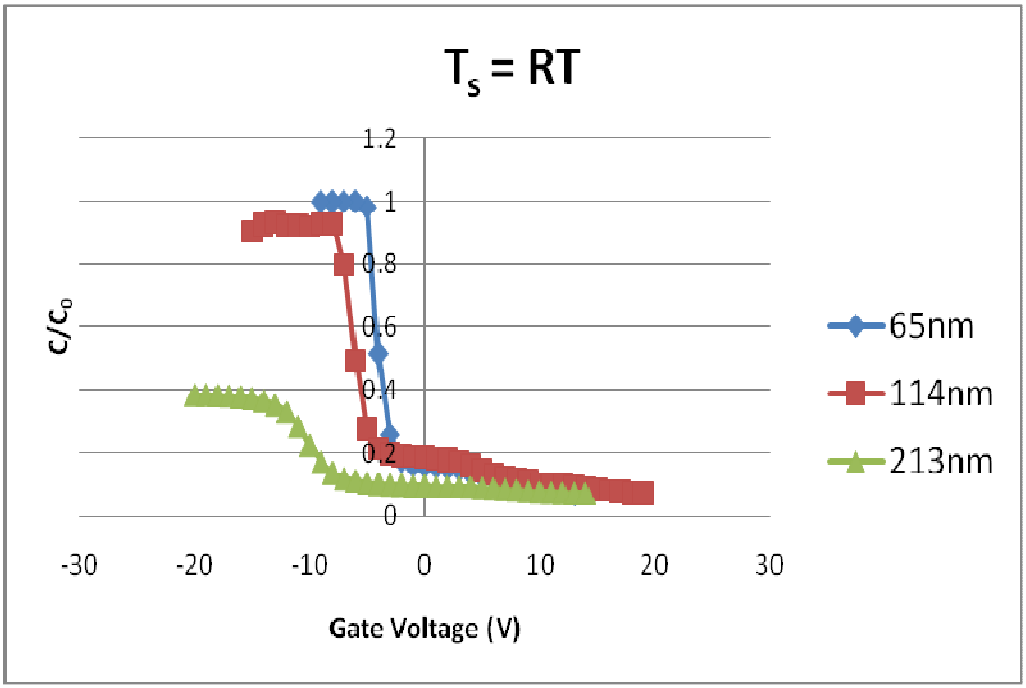

Figure 35 C-V curves form MOS structures with HfO_2 films grown at T_s = RT.

The accumulation capacitance for samples grown at room temperature is also inversely proportional to the oxide thickness as it was exhibited by samples depostied at T_s = 400 °C and 300 °C. From Figure 33, Figure 34, and Figure 35 it is clear that the transition from inversion capacitance to accumulation occurs very gradually. The C-V curves exhibit a parallel shift towards the negative voltages; this means that a higher gate voltage is needed to drive the MOS structures to accumulation region. Another interesting point is that the accumulation capacitance does not have a very stable region in the C-V plots. It is variable rather than flat and constant. All these deviations from the ideal C-V curve are due to oxide positive charges and interface traps [34]. These charges and traps could be arising from the chemical structure of the grown oxide film, film-substrate and film electrode interfaces. The incorporation of forming gas (FG) treatment to the MOS structures fabrication will be explained later as an alternative to reduce the number of oxide charges and interface traps present in the HfO_2 films grown.

4.2.4 Effect of T_s on HfO_2 electrical performance.

The effect of substrate temperature on the electrical properties of the HfO_2 films deposited in this work was also analyzed. Figure 36 shows a comparison of the C-V curves obtained for different substrate temperatures. The thicknesses of these films are comparable within the error of ±5%. In this comparison, any differences in the capacitance can be attributed to the electronic quality of the high-*k* dielectric. Figure 36 shows that the sample deposited at room temperature exhibits the highest accumulation capacitance among the three samples. This is in good agreement with cross-sectional HRSEM data the shows the lack of any interface layer between the deposited HfO_2 films and the Si substrates. An interface layer would have a lower dielectric constant than the dielectric constant of HfO_2. As a result, the overall gate stack capacitance would be lower.

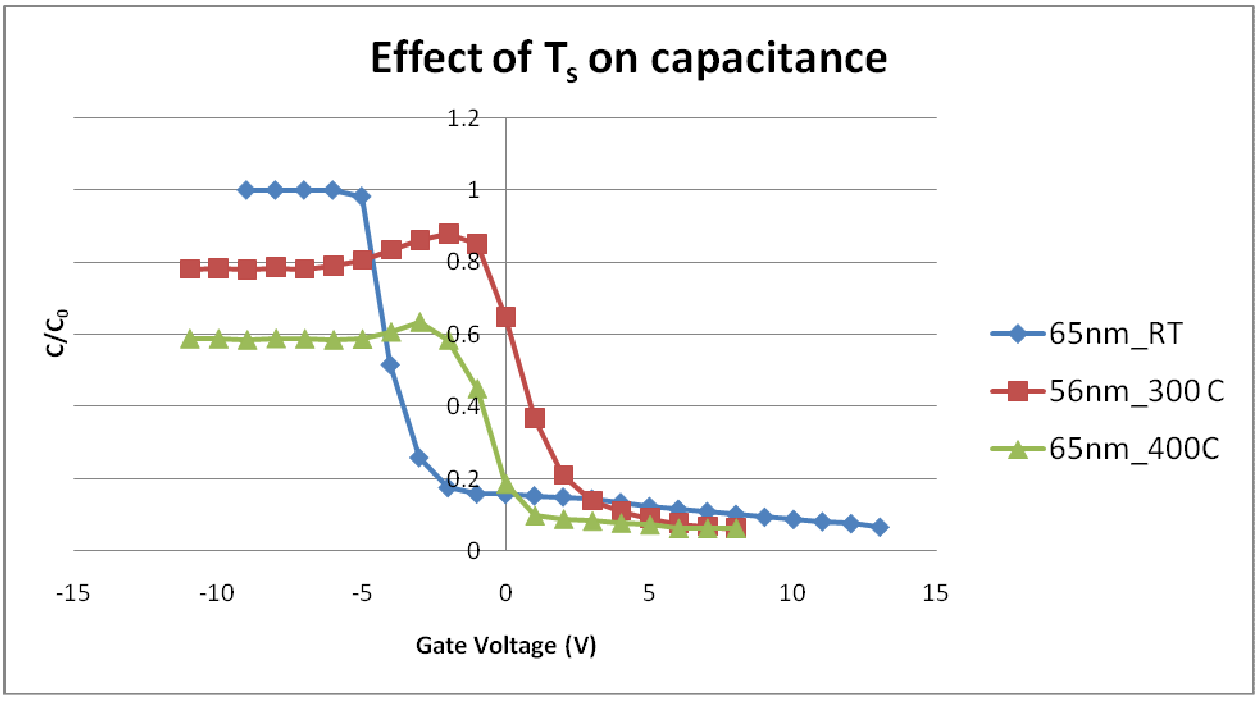

Figure 36 Effect of T_s on the electrical properties of HfO_2 films deposited by RF sputtering.

A different scenario occurs with the sample deposited at T_s = 300 °C. The accumulation capacitance for this sample should be higher than the accumulation capacitance of the other two samples because it has an oxide thickness of 56 nm which is smaller than the other oxides' thickness; however, its capacitance is smaller. The reason for this difference in capacitance is attributed to a lower dielectric constant of the IL formed between the Si substrate and the HfO_2 film at 300 °C. Previous works have shown that when Hf is oxidized to form HfO_2 at different temperatures, the accumulation capacitance is reduced as the oxidation temperature increases due to an increase in the IL thickness [35]. Therefore, the decrease in capacitance for samples deposited at T_s = 300 °C is attributed to the interface layer formed as seen in the HRSEM data. A similar decrease in the accumulation capacitance is seen for the sample deposited at 400 °C. From HRSEM, a substrate temperature of 400 °C produces a very thick interface layer. In summary, a higher substrate temperature yielded a thicker interface layer which resulted in lower overall capacitance. This is attributed to the interfacial layer having a lower dielectric constant compared to HfO_2.

In order to study the quality of the deposited HfO_2 films, the dielectric constant of the gate stacks fabricated was calculated as follows:

- The values of capacitance (capacitance density) at accumulation biasing outputted by the capacitance meter were averaged and used as the oxide capacitance (C_{ox}).

- The value for the dielectric constant (k) was then calculated by solving for k_0 in equation 1:

  $C_0 = \frac{K_0 \varepsilon_0 A_G}{x_0}$

  Then,

  $$K_0 = \left(\frac{C_{ox}}{A_G}\right)\left(\frac{t_{ox}}{\varepsilon_0}\right)$$

The highest dielectric constant obtained in this work is 25 for HfO_2 film deposited at RT. This is an expected result for samples grown at RT since no IL formation (HRSEM analysis) occurs that might degrade the gate stack dielectric constant and as a consequence the gate capacitance.

In order to reduce the oxide charges and the interface traps from the MOS structures, N_2 annealing and H_2 annealing treatments were performed on the HfO_2 films before top contact metallization. The results are presented and discussed in the following section.

4.2.5 Effect of N_2 annealing on HfO_2 electrical properties

MOS structures with HfO_2 grown at T_s = 400 °C were annealed in N_2 and studied their electrical characteristics. The C-V curves are shown in Figure 37, where a comparison of the sample with and without N_2 annealing is presented. The only difference between sample C15 and C17 is that samples C17 received a N_2 annealing treatment with the purpose of reducing the oxide charges an interface traps.

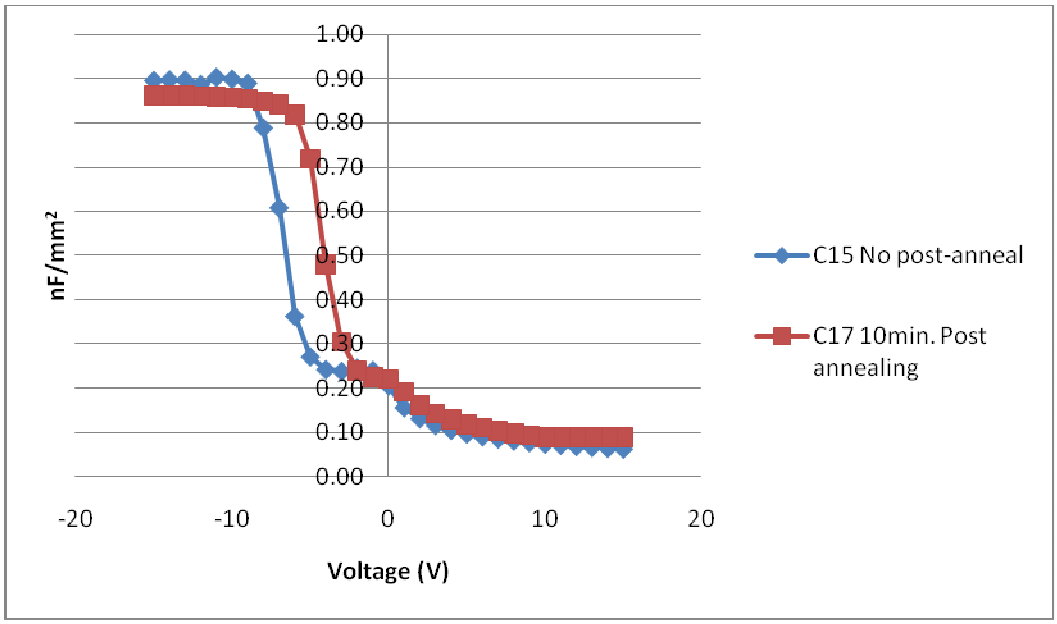

Figure 37 Effect of N_2 annealing on the electrical behavior of MOS structures with HfO_2 films grown at T_s = 400 °C.

Figure 37 shows that the annealed sample demonstrated a parallel shift towards the positive voltage (which imply that lower gate voltage is required to bias the MOS structure into accumulation), indicating a reduction in oxide charge and interface trap density. However, the presence of a shoulder like in both C-V curves is an indication of the high density of oxide charges still present in the oxide films. In an attempt to further reduce the density of oxide charges and the interface traps in the grown HfO_2 films and improve the behavior of the MOS structures, H_2 annealing treatment was performed and the results are explained below.

4.2.6 Effect of H_2 treatment on HfO_2 electrical properties

MOS structures were annealed under FG atmosphere after HfO_2 deposition. C-V curves for samples that went under FG annealing treatment are compared to curves that did not receive the treatment in Figure 38and Figure 39 for T_s = RT and 300 °C, respectively.

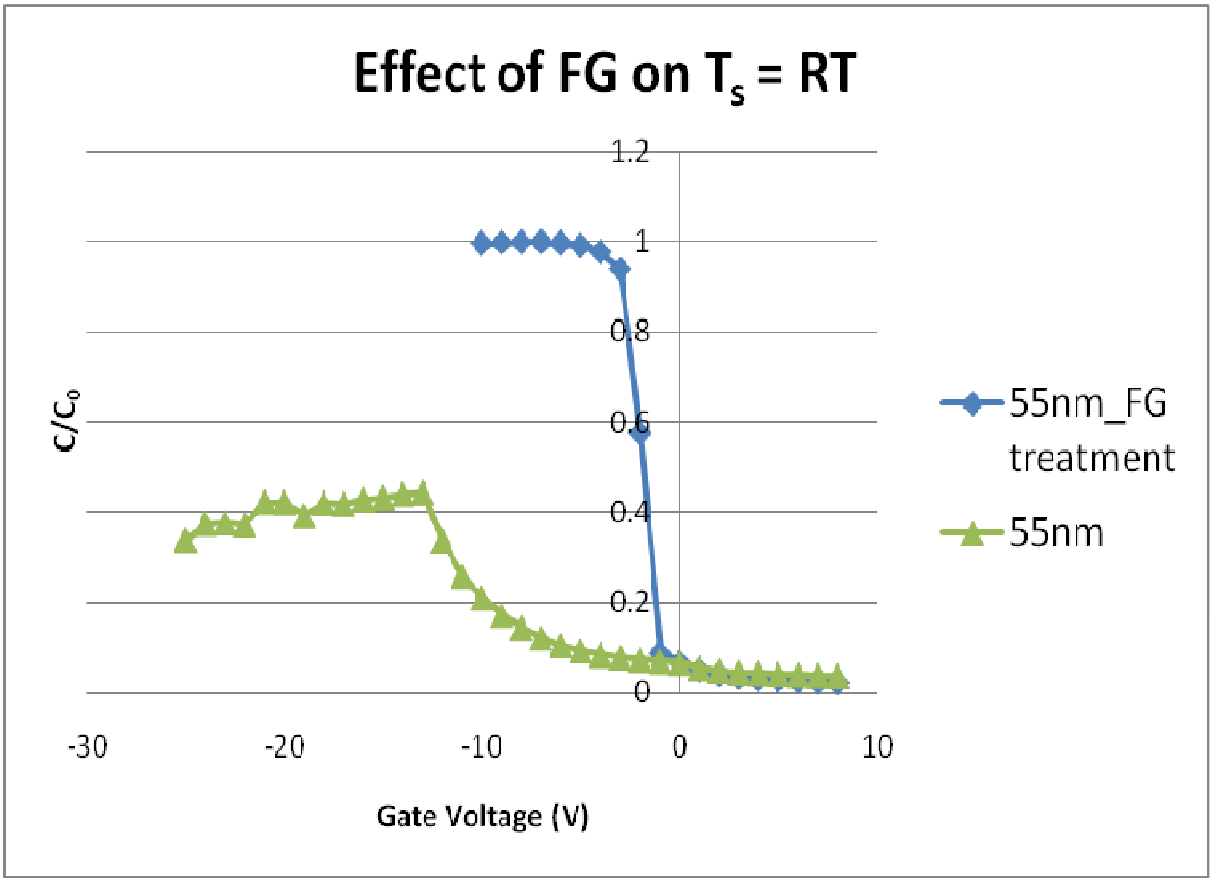

Figure 38 Effect of FG treatment on MOS structures grown at T_s = RT for reduction of oxide charges and interface traps.

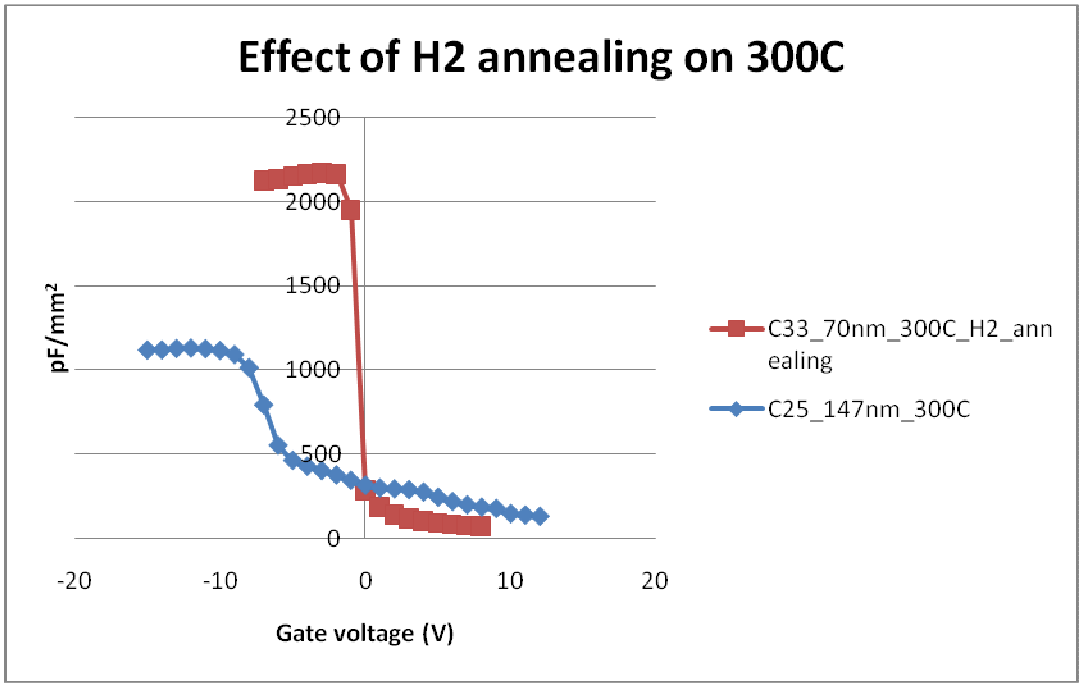

Figure 39 Effect of FG treatment on MOS structures grown at T_s = 300 °C for reduction of oxide charges and interface traps.

From samples deposited at T_s = RT, after depositing HfO_2 on sample C36 it was cut into two halves. One half was annealed in FG prior top contact deposition and the other half was contacted with aluminum right after HfO_2 deposition. The results show that samples that did not go under FG treatment present a stretched out C-V and non uniform accumulation capacitance as a result of oxide charges and interface traps as mentioned previously. On the other hand, samples that went under FG treatment were shifted towards positive voltages. They have an abrupt change in capacitance when going from strong inversion to accumulation, capacitance does not change gradually, C-V curves have good shapes and a uniform and more stable accumulation capacitance was obtained. Sample deposited at T_s = 300 °C with FG treatment is compared to a sample process under the same substrate temperature but with an oxide thickness that is twice as thick. As expected, the accumulation capacitance in the thicker sample is smaller than in the thinner sample; however, the thinner sample that went through FG annealing

treatment have a better C-V shaped for the same reasons explained above. In general, after FG treatment, it is seen that the amount of positive oxide charges and interface traps is lowered.

5. Summary and Conclusions

The results presented in this work offer a good explanation of the micro structural evolution of IL formed between HfO_2 and Si as the substrate temperature increases while deposition of HfO_2 occurs. The effect of substrate temperature on the electrical properties of HfO_2 thin films was also investigated. Micro structural analysis in conjunction with electrical characterization provide a good understanding of the interface layer that is formed when HfO_2 is deposited on silicon using RF sputtering at various temperatures.

HfO_2 thin films were deposited by sputtering onto Si(100) varying the T_s from RT to 500 ^oC. The effect of T_s on the growth, crystal structure, surface morphology and surface/interface structure and composition of the deposited HfO_2 films was studied using GIXRD, HR-SEM, EDS, and electrical measurements. The results show that the effect of T_s is remarkable on the growth, surface and interface structure, morphology and chemical composition of the HfO_2 films. HfO_2 films grown at T_s<200 ^oC were amorphous while films grown at $T_s \geq 200$ ^oC were polycrystalline with monoclinic crystal structure. The onset of crystalline occurs at T_s=200 ^oC. An interface layer (IL) formation occurs due to reaction at the HfO_2-Si interface for HfO_2 films deposited at $T_s \geq 200$ ^oC. The thickness of IL increases to 27 nm with an increase in T_s to 400 ^oC. The exponential temperature-dependence of the ILs growth was evident from the IL-T_s analysis. Hf, Si, and O contributions in EDS measurements indicate the IL is a Hf-silicate ($HfSiO_4$). XPS analysis suggests that a small amount of Si is segregating to the surface of the HfO_2 films at high temperatures, and also, it suggests that a chemical reaction is driven by temperature and results in the formation of a (Hf,Si) O compound at the interface. From electrical measurements, HfO_2 films with dielectric constant as high as 25 were deposited. H_2 annealing treatments to reduce the density of oxide charges and interface traps were successfully performed on MOS structures and HfO_2 films quality was enhanced.

6. Future Work

The results of this work are a very good foundation for future research that requires more sophisticated characterization equipment. The present work can be further investigated if the studies mentioned below are performed.

Leakage current studies could be made in order to study the insulating properties of the HfO_2 films as a function of temperature. It is expected to have higher leakage currents when higher substrate temperatures are used to grow HfO_2 because of the grain boundaries that formed in polycrystalline films that might be used as conduction paths through the oxide film. These studies can be correlated with measurements of bandgap if HfO_2 is deposited on transparent substrates such as quartz. More sophisticated equipments such as a transmission electron microscope (TEM) could be used to measure a possible IL formation of the samples with HfO_2 grown at room temperature and also to study the IL formation of HfO_2 films of 5 nm or less in thickness.

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Curriculum Vita

Brandon Adrian Aguirre was born on January 06 of 1984 in ciudad Juarez Chihuahua Mexico. He started his career at the University of Texas at El Paso (UTEP) in fall 2001. By the fall of 2006 Brandon graduated with a bachelor's degree in electrical engineering with Cum Laude Honors. As undergraduate student, he got a nanotechnology-related summer research internship at Purdue University during the summer of 2005, and the following year he was selected to participate in the Louis Stokes Alliance for Minority Participation (LSAMP) research academy on the summer of 2006 at UTEP. During the fall of the same year, he joined the nano-Materials Integration Laboraory (nanoMIL) in UTEP and continue working in the same laboratory as graduate student. As undergraduate student Brandon was recipient of NASCAR/Wendell Scott Award 2007-2008, General Motors Engineering Excellence Award 2007-2008, 2007 Xerox Hispanic College Liaison Program (HCLP) Scholarship, National Action Council for Minorities in Engineering (NACME) scholarship 2006-2007, and the National Science Foundation Scholarship (NSF) (2004-2007). Also, Brandon obtained the 2nd place as the outstanding student award of the electrical and computing engineering department (fall 2006) and he and his team were awarded the outstanding senior design project on fall 2006. As graduate student, he was selected to participate in the NanoScholar internship program at Semiconductor Manufacturing Technology (SEMATECH) during the summer of 2007, and the following year he worked as a product engineer in a 7-month Co-op program in Texas Instruments. As graduate student, Brandon was awarded the LSAMP Bridge to the doctorate fellowship to continue his education. Brandon was one out of ten students selected across the United States to participate in an International Winter School Program to be celebrated in Indian Institute of Technology (IIT) in Mumbai, India from November 27th to December 13th.

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