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Investigation of Selective Nanohetero-epitaxy Growth on Si(100) Substrates for HgCdTe Infrared Detector Applications

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Dedication

I would like to dedicate this thesis to my parents, Venancio Diaz and Silvia Vences,

for all the priceless support they have giving me throughout my college career

which I would never forget,

To my sister, Itzel Diaz, for all her support and patience whenever I needed,

And

To my boyfriend, Hugo Najera, for all the support and guidance he gave me

whenever I needed.

INVESTIGATION OF CdTe NANOHETERO-EPITAXY GROWTH ON Si(100) SUBSTRATES FOR HgCdTe INFRARED DETECTOR APPLICATIONS

by

ARYZBE DIAZ, B.S.E.E.

THESIS

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Abstract

The selective CdTe Nanohetero-Epitaxy growth on Si(100) substrates has been achieved without the use of a mask in an attempt to reduce the dislocation density at the CdTe/Si interface to $10^5/cm^3$ using the Close-Space Sublimation (CSS) technique, which is a low-cost effective technique for the deposition of polycrystalline CdTe films. Furthermore, CdTe is a compound semiconductor with a direct bandgap of 1.5 eV, which makes it an ideal material for the applications of infrared detectors and solar cells. It has been demonstrated that the selective growth of CdTe on patterned Si(100) substrates results in CdTe grains with smooth surfaces. For this reason, these high quality grains may be used for the subsequent growth of planar MBE CdTe followed by HgCdTe for the applications of Long-Wavelength Infrared (LWIR) detectors and Middle-Wavelength Infrared (MWIR) detectors. Several techniques have been used for the epitaxial growth of CdTe on Si, such as Molecular Beam Epitaxy (MBE), Liquid Phase Epitaxy (LPE), Hot-Well Epitaxy (HWE) and Metalorganic Vapor Phase Epitaxy (MOVPE); however, these techniques are expensive and have low growth rates. For this reason, special interest has been given to the CSS technique for the growth of CdTe such as its low-cost and higher growth rates (>1 μm/h).

In this study, the first set of experiments consisted of the planar epitaxial growth of CdTe on CdTe(111) substrates, resulting in average growth rates between 5 - 10 μm/hr. The film with the most promising film morphology resulted from growth parameters, where T_{sou}=530°C and T_{sub}=350°C. The second set of experiments consisted of the planar epitaxial growth of CdTe on Si(100) substrates, resulting in average growth rates between 6 - 10 μm/hr. The same parameters used to produce the highest quality CdTe films on CdTe(111) were found to be optimum for Si(100) as well. The third set of experiments consisted of the selective epitaxial growth of CdTe on patterned Si(100) substrates, where CdTe selectively was achieved for all substrate and source temperatures analyzed without using a mask. This has never been observed before for CdTe deposited on patterned Si. Characterization

methods such as scanning electron microscopy (SEM) and x-ray diffraction (XRD) were used to observe CdTe film and grain morphology and to analyze the structure and quality of the planar CdTe films. As a result, the characterization of these films confirmed that CSS can be an effective and low-cost technique for the planar and selective epitaxial growth of CdTe films.

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Chapter 1: Introduction

1.1. Importance of Infrared Detectors and Focal Plane Arrays (FPAs)

Mercury Cadmium Telluride (HgCdTe), a compound semiconductor material for the applications of infrared (IR) detectors and Focal Plane Arrays (FPAs), has been developed since its first synthesis in 1958. Direct bandgap (E_g) semiconductors, such as HgCdTe detectors, have a strong optical absorption that allows the detector structure to absorb a very high percentage of the signal for the long-wavelength infrared (LWIR) spectral region between 8-14 μm [1]. Moreover, epitaxial growth of HgCdTe films requires a suitable substrate, and for this reason cadmium telluride (CdTe) has been used as a substrate since it was first available in reasonably large sizes [2]. CdTe substrates were replaced with CdZnTe substrates, due to the fact that CdTe has a lattice mismatch with LWIR and MWIR HgCdTe which causes dislocation densities above the $10^4 cm^{-2}$ range that have an effect on detector performance [1]. There are advantages to using Si substrates including its mechanical strength the elimination of thermal strain issues, and its availability in large area wafers [1,2,10,27].

HgCdTe alloys have been grown on CdTe(211), Si(211), CdTe(111) substrates using the Liquid Phase Epitaxy (LPE) and Molecular Beam Epitaxy (MBE) techniques [1,2]. Other deposition techniques such as Hot-Well Epitaxy (HWE), Isothermal Close Space Sublimation (ICSS), Metalorganic Vapour Phase Epitaxy (MOVPE), and Vapour Phase Epitaxy (VPE) have being used for the epitaxial growth of CdTe. However, these techniques are expensive, more complex to use, and have slow growth rates. For this reason, special interest has been given to the CSS technique for the deposition of CdTe thin films, since this technique is a low-cost effective method, simple to use, and is associated with high growth rates (>1 μm/h) compared to the techniques mention above. The CSS technique is a common method to used for the fabrication of polycrystalline CdTe solar cells; however, recent work has been

done to develop growth parameters that will produce CdTe films of high quality for infrared detector applications [3,4].

1.2. MOTIVATION OF THIS THESIS

HgCdTe has been the most widely used compound semiconductor material for military, civil and commercial infrared application which requires the use of focal plane arrays with high image resolutions and system performance in the long-wavelength infrared (LWIR) and the middle-wavelength infrared (MWIR) regions [1,7]. The advantages of using HgCdTe for these applications are (1) its direct bandgap of 1.6 eV with high absorption coefficient, (2) the ability to obtain both low and high carrier concentrations, (3) high mobility electrons, (4) low dielectric constant, (5) the availability of wide bandgap lattice-matched substrates for epitaxial growth, and (6) its moderate thermal coefficient of expansion [1,2,5]. Focal plane arrays (FPAs) require a detailed knowledge and control of the experimental factors that cause defects in the material including dislocations, twins, stacking faults, surface hillocks and crater defects, precipitates, and defects created by sample preparation methods [5]. Furthermore, the development of these detectors requires high sensitivity, small pixel size, large-area substrates, low defect density and long-term thermal-cycling reliability [5,6].

By the mid-1980s it was demonstrated that the addition of a few percent (typically 4%) of zinc telluride (ZnTe) to CdTe could create a lattice-matched substrate (CdZnTe), which resulted in defect densities in the low $10^4 cm^{-2}$ range [1,2,8]. However, CdZnTe substrates also have several drawbacks such as the lack of large substrate areas, high cost production, and the difference in the thermal expansion coefficient between CdZnTe and Si readout circuits [2,9]. For this reason, employing the nanoheteroepitaxy (NHE) technique makes it possible to grow CdTe on Si with fewer defects. The NHE technique can be achieved by the selective deposition of CdTe on patterned Si(100) substrates using a variety of growth techniques. The use of the CSS technique to do this will reduce the production

cost and fabrication time of CdTe films for infrared applications. The ability to selectively deposit CdTe on patterned Si(100) substrates without the use of a mask has not been observed before using the CSS technique. This will benefit researchers in this field economically and will motivate them to develop more techniques to obtain high quality CdTe films for the subsequent growth of HgCdTe applications.

1.3. CONTRIBUTION OF THIS THESIS

The purpose of this thesis is to develop and apply a method for the fabrication of CdTe films on Si(100) substrates using the CSS technique for the subsequent growth of infrared-detector-HgCdTe. Furthermore, this thesis focuses on the selective nano-heteroepitaxial (NHE) growth of CdTe on patterned Si(100) substrates for the subsequent growth of planar CdTe and HgCdTe in order to reduce dislocations at the CdTe/HgCdTe interface below $10^5 cm^{-2}$. The Si(100) substrates are patterned using the optical lithography method. The dry etching method is used in order to create pillars at the nanoscale. The selective CdTe growth is achieved by depositing a single crystal CdTe grain on top of each pillar using the closed-space sublimation (CSS) technique. This was successfully accomplished for a variety of source and substrate temperatures and deposition times for the first time on Si(100) without the use of a mask using the CSS technique. The scanning electron microscope (SEM) was used to prove that the CSS technique is an excellent method for the fabrication of CdTe on patterned and planar Si substrates.

Chapter 2: Literature Review

2.1. CdTe and HgCdTe Properties

Cadmium telluride (CdTe), is a direct gap semiconductor with a room temperature bandgap energy of 1.5 eV. CdTe is recognized for the electrical and physical properties required for an infrared detector substrate [1,11]. Furthermore, CdTe is a transparent material out to 30 μm, with high atomic number and good charge-transport property which makes it an effective detector material of γ and χ-radiation [4].

At present, mercury cadmium telluride (HgCdTe) is the most widely material used for infrared (IR) photodetectors [2]. HgCdTe can be used for detectors operated at various modes such as photoconductors, photodiodes, or metal-insulator-semiconductor (MIS) detectors [2]. Several properties of HgCdTe makes it a perfect semiconductor material to react with infrared (IR) radiation. These properties include [1]:

1. Adjustable bandgap from 0.7 to 25 μm.
2. Direct bandgap with high absorption coefficient.
3. Moderate dielectric constant/index of refraction.
4. Moderate thermal coefficient expansion.
5. Availability of wide bandgap lattice-matched substrates for epitaxial growth.

Moreover, the specific advantages of HgCdTe are its ability to obtain both low and high carrier concentrations, high mobility of electrons and low dielectric constant. Consequently, the extremely small change of lattice constant with composition makes it possible to grow high quality layered and graded gap structures [2].

2.2. CdTe Applications

2.2.1. Solar cells

Cadmium telluride (CdTe) has been recognized as a promising photovoltaic material for solar cells due to its near-optimum bandgap of ~1.5 eV and its high optical absorption. It is possible to fabricate CdTe cells with efficiencies of more than 15% and commercial-scale modules with efficiencies of more than 10% [15,34,36]. The performance and fabrication of thin-film solar cells was limited by the conventional SnO_2/CdS/CdTe device structure for more than 30 years. The device structure was modified to a CTO/ZTO/CdS/CdTe structure which helped to improve the efficiency [36]. The National Renewable Energy Laboratory (NREL) has demonstrated the fabrication of CdS/CdTe polycrystalline thin-film solar cells with a total area efficiency of 16.5%. In comparison, NREL has achieved an efficiency of 19.9% for solar cells fabricated with copper indium gallium selenide (CIGS) [35]. SunPower Laboratories have demonstrated the highest commercially an efficiency (22%) solar cell on silicon (Si) wafers, and the University of New South Wales has achieved an efficiency of 25% on monocrystalline silicon. Figure 2.1 illustrates the research on solar cells efficiency that the NERL laboratories have done over the past 30 years.

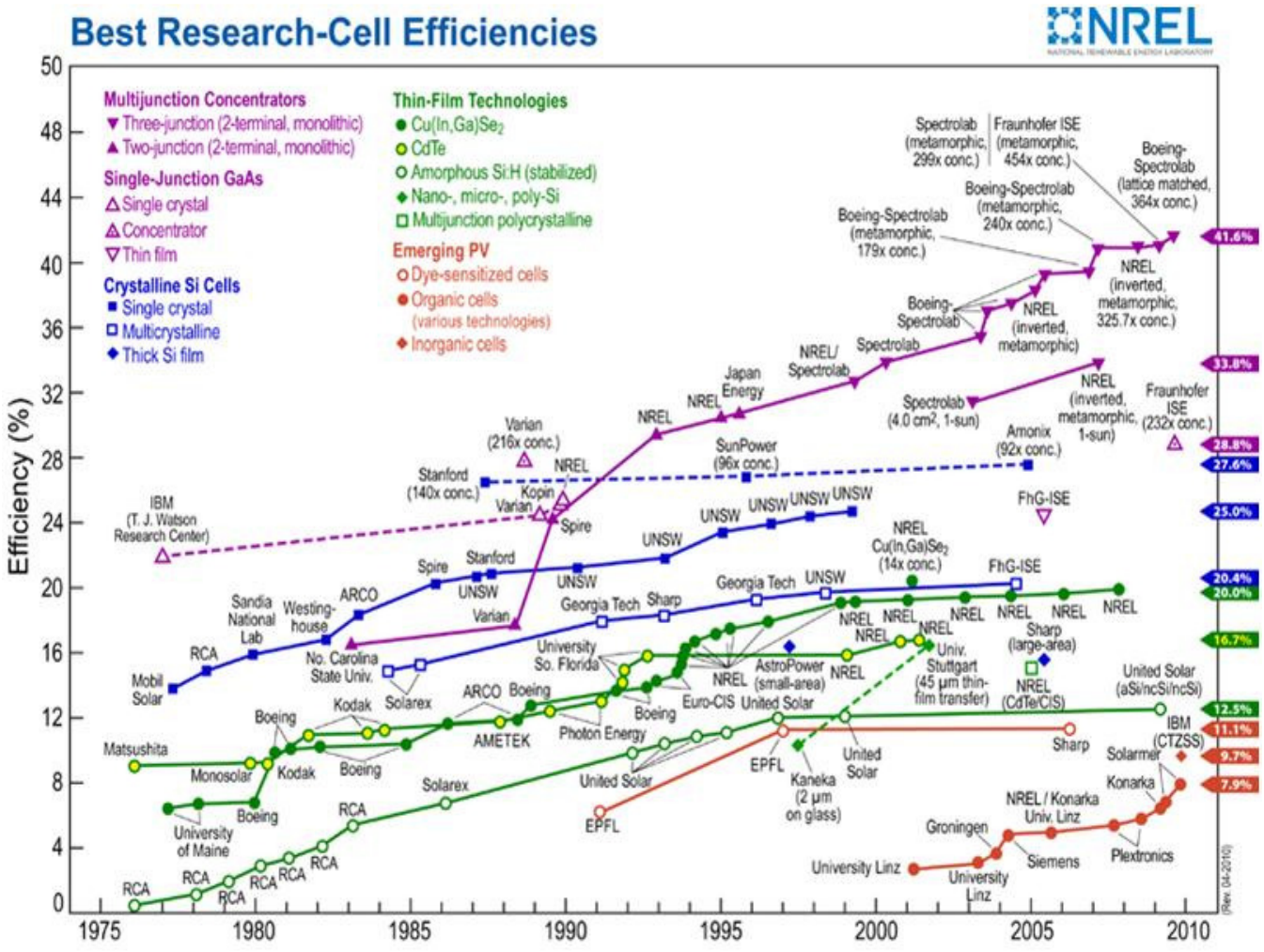


Figure 2.1. NREL best research solar cell efficiencies [35].

Much of the solar cell research has focused in polycrystalline film solar cells due to their high efficiency and low-cost fabrication cost [15]. Unfortunately, the main drawback on the fabrication of CdS/CdTe thin film solar cells is the high density of defects due to the large lattice mismatch (~10%) and thermal mismatch between CdS and CdTe, which decreases the performance of the cell. For this reason, the ordered polycrystalline approach by Zubia *et al.* [15] has being proposed to reduce defect densities in lattice mismatched materials. This approach consists of the selective deposition on a patterned selective area by the CSS technique to produce an ordered array of high quality crystals in order to increase solar cell performance.

2.2.2. Infrared Detectors

The epitaxial growth of mercury cadmium telluride (HgCdTe) has dramatically improved over the past 10-15 years resulting in the ability to realize large-area, high performance infrared focal plane arrays (FPA's) in the medium-wavelength infrared (MWIR) spectral range from 3-5 μm, and the long-wavelength infrared (LWIR) spectral range from 8-12 μm [28,29]. Infrared detection in HgCdTe begins with the excitation of an electron from the valence band into the conduction band, where the minimum photon energy required is equal to the bandgap [1]. Moreover, the bandgap of HgCdTe is a function of the alloy composition ratio "x" of CdTe to HgTe, and the temperature of the material, where the relationship between the element and the bandgap is given by the following expression [2]:

$$E_g = -0.302 + 1.93x - 0.81x^2 + 0.832x^3 + 5.35(1 - 2x)10^{-4}T \qquad \text{Eq. (2.1)}$$

where the temperature is in units of Kelvin. The relationship between the wavelength (λ) and the bandgap energy (E_g) is given by the following expression [31]:

$$\lambda_c = \frac{1.24}{E_g} \qquad \text{Eq. (2.2)}$$

Figure 2.2 shows the dependence of Eq. (2.1) for composition of alloys, x=0.2, x=0.3, and x=0.4, where higher values of "x" can result in wavelengths as short as 0.7 μm.

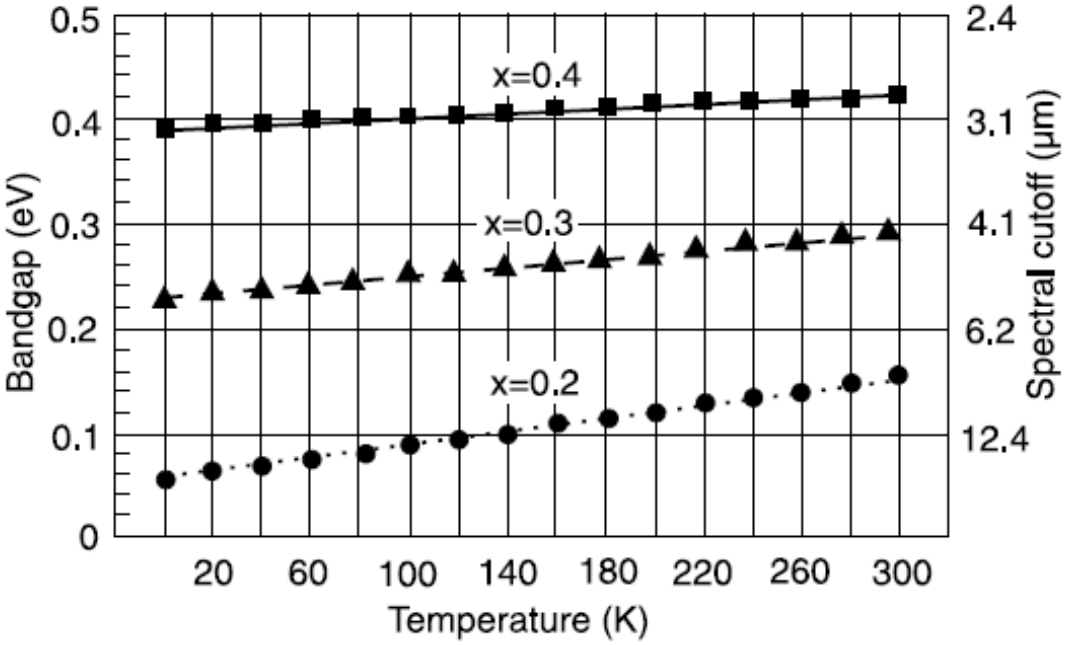


Figure 2.2. Bandgap and corresponding spectral cutoff for representative alloy compositions of $Hg_{1-x}Cd_xTe$ as a function of temperature as calculated from Eq. (2.1) [2].

HgCdTe semiconductors have a strong optical absorption as the photon energy increases above E_g, which allows HgCdTe infrared detector structures to absorb a very high percentage of the signal while being relatively thin, on the order of 10-20 μm. Consequently, minimizing the detector thickness helps to minimize the volume of the material which can generate noise, such as thermal excess carriers in the diffusion-limited operating mode [2].

However, the epitaxial growth of HgCdTe has being a major problem due to the high vapour pressure of Hg present during growth, which makes it difficult to control the stoichiometry and composition of the growth material [1,2]. The difficulties of growing HgCdTe material have lead to the development of alternative infrared detectors materials such as the PbSnTe material system. PbSnTe is easy to grow and high quality infrared detectors have been produced that were able to detected signals within the 8-12 μm spectral region. Unfortunately, the development of PbSnTe had to be stopped for

two factors, (1) the high dielectric constant of PbSnTe compared to HgCdTe and (2) the large temperature coefficient of expansion (TCE) mismatch with Si [1].

For many years, bulk growth of HgCdTe was initially used for many types of infrared detectors, but the growth produced relatively thin rods of HgCdTe material and non-uniform distribution of composition. Another disadvantage of using bulk growth was the need to thin the bulk wafers, and the requirement of further fabrication steps such as polishing the wafers, mounting them on suitable substrates and polishing to the final device thickness [1,2]. By the 1990s, bulk growth was replaced by various epitaxial techniques, such as liquid phase epitaxy (LPE), vapour phase epitaxy (VPE), metalorganic chemical vapour deposition (MOCVD), and molecular beam epitaxy (MBE). Among these epitaxial growth techniques, MBE and MOCVD have the benefit to modify the growth conditions dynamically during the growth in order to tailor bandgaps, add and remove dopants, prepare surfaces and interfaces, add passivType equation here.ations, perform anneals and grow on selected areas of the substrate. Table 2.1 provides a comparison of the various epitaxial HgCdTe techniques.

Table 2.1. Comparison of the various methods used to grow HgCdTe [2].

	Bulk			Liquid phase epitaxy		Vapour phase epitaxy	
	SSR	Travelling heater method					
		HCT melt	Te melt	Hg melt	Te melt	MOCVD	MBE
Temperature (°C)	950	950	500	350–550	400–550	275–400	160–200
Pressure (Torr)	150 000	150 000	760–8000	760–11400	760–8000	300–760	10^{-3}–10^{-4}
Growth rate (μm/hr)	250	250	80	30–60	5–60	2–10	1–5
Dimensions *w* (cm)	0.8–1.2 dia	0.8–1.2 dia	2.5 dia	5	5	7.5 dia	7.5 dia
l (cm)	–	–	–	6	5	4	4
t (cm)	15	15	15	0.0002–0.0030	0.0005–0.012	0.0005–0.001	0.0005–0.001
Dislocations (cm^{-2})	$<10^5$	–	$<10^5$	$<10^5$	$<10^5$–10^7	5×10^5–10^7	5×10^4–10^6
Purity (cm^{-3})	$<5\times10^{14}$	$<5\times10^{14}$	$<5\times10^{14}$	$<5\times10^{14}$	$<5\times10^{14}$	$<1\times10^{15}$	$<1\times10^{15}$
n-Type doping (cm^{-3})	N/A	N/A	N/A	1×10^{14}–1×10^{18}	1×10^{14}–1×10^{16}	5×10^{14}–5×10^{18}	5×10^{14}–1×10^{19}
p-Type doping (cm^{-3})	N/A	N/A	N/A	1×10^{15}–1×10^{18}	1×10^{15}–5×10^{16}	5×10^{15}–5×10^{17}	1×10^{16}–5×10^{18}
X-ray rocking curve (arc sec)	–	–	20–60	<20	<20	50–90	20–30
Compositional uniformity (Δx)	<0.002	<0.004	<0.005	<0.002	<0.002	±0.01–0.0005	±0.01–0.0006

The epitaxial growth of HgCdTe requires a suitable substrate. CdTe was used initially because it was available in large sizes and as a result of its physical properties such as its transparency out to 30 μm, potential doping of the epitaxial film, and it is more structurally stable than HgCdTe crystals. However, the main disadvantage of using CdTe as a substrate is the lattice mismatch with LWIR and MWIR HgCdTe. It was found that the crystal perfection of HgCdTe and surface morphology of the epitaxial layers was significantly influenced by the substrate epitaxial layer lattice mismatch. For this reason, by the 1980s, it was found that adding a few percent (4%) of ZnTe to CdTe could create a

lattice-matched substrate to HgCdTe [1,2,32]. Figure 2.3 demonstrates a comparison of the bandgap and lattice constant variation with the alloy composition of $Hg_{1-x}Cd_xTe$ and CdZnTe substrates.

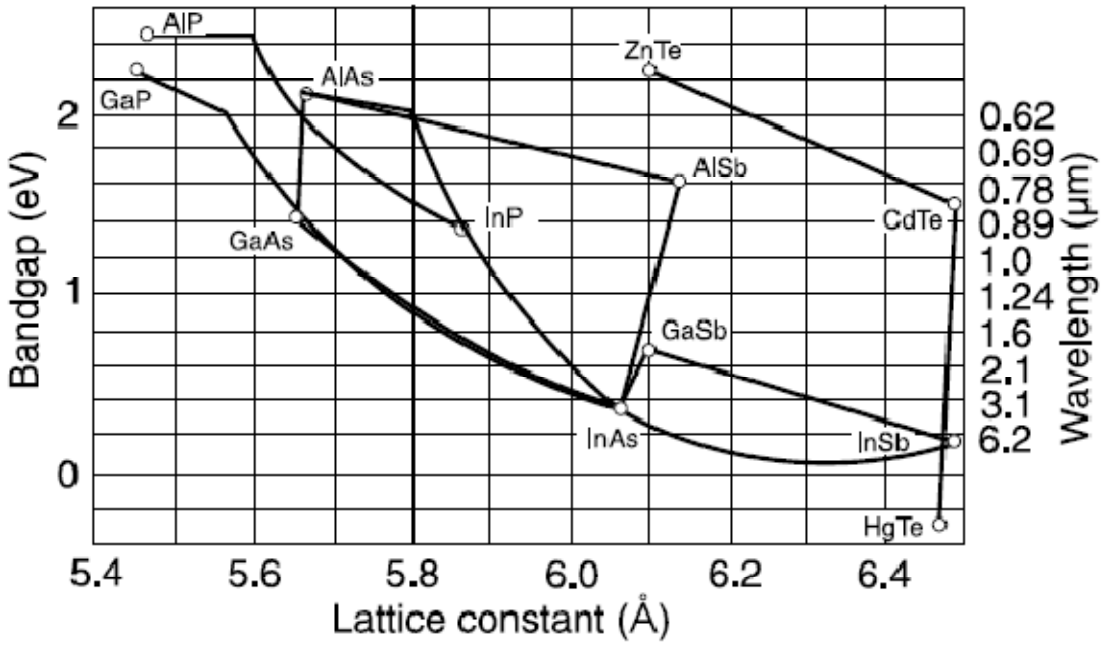


Figure 2.3. Comparison of the bandgap vs. lattice constant variation with alloy composition of $Hg_{1-x}Cd_xTe$ and CdZnTe substrates, with the lattice constant variety of III-IV compounds (after Ref. 10). $Cd_{0.96}Zn_{0.04}Te$ is a good match for a wide range of MWIR to LWIR HgCdTe alloys [2].

Unfortunately, CdZnTe substrates have several disadvantages such as the lack of large areas, cost, and the thermal expansion mismatch between the detector and the read-out circuit (ROIC) which affects the performance of the detector [2,5,8,9].

For this reason, scientists and engineers have being focusing on the epitaxial growth of mercury cadmium telluride (HgCdTe) alloys on Si(100) and Si(211) substrates due to the excellent mechanical properties, the availability of large area wafers at a low cost, and the well established fabrication of silicon-based integrated circuits [1,2,5,8,10,13,20,27,28,30]. In addition, if high quality HgCdTe can be grown on Si, the HgCdTe infrared detector and the signal processing electronics of the focal plane array can be integrated on the same wafer [26]. Unfortunately, the large lattice mismatch (~19%) between

CdTe and Si prevents the fabrication of high quality of CdTe films on Si substrates. CdTe grown on Si substrates result in films with high dislocation densities in the mid-$10^5 cm^{-2}$ range which affects the detector's performance [33]. In order for a semiconductor to operate as a radiation detector it must have a large bandgap and low carrier density to minimize current noise. In addition, a radiation detector must have higher carrier mobilities to produce pulses with fast rise time, a high atomic number element for good stopping power of high energy radiation, and a long carrier lifetime to allow efficient charge collection [30]. Therefore, as the dislocations densities decrease in the film, the quality and performance of infrared detectors fabricated on HgCdTe epilayers will be improved [21]. Previous research has been done to reduce these dislocations by growing CdTe layers on Si and GaAs substrates using the molecular beam epitaxy (MBE) technique [1,2,7,8,9,27,29]. However, research has proved that using a layer of ZnTe as a buffer layer between CdTe and Si reduces defects arising from the 19% lattice mismatch [13]. The epitaxial lateral overgrowth (ELO), which is a technique to help reduce dislocation densities in layers grown on substrates with a large lattice mismatch, has been applied to the growth of CdTe on Si and GaAs substrates using the MBE and metalorganic vapour phase epitaxy (MOVPE) technique. For the ELO growth of CdTe and HgCdTe on Si substrates to be successful, the first requirement is that the growth should be selective [20]. For this reason**,** selective grown of CdTe on nanopatterned silicon on insulator (SOI) substrates by MBE has been developed in order to grow high quality CdTe films for the subsequent growth of HgCdTe films [10,21,22]. Moreover, CdTe epitaxial layers have being grown on patterned Si(100) and GaAs(100) substrates using SiO_2, Si_3N_4, or CaF_2 masks, where the selective growth of CdTe layers shows strong anisotropy depending on the orientation of the pattern on the mask, as wells as the orientation of the substrate [26]. Further work has to be done to reduce the dislocation density during the selective hetero-epitaxial growth of CdTe resulting from the lattice mismatch with the Si substrates. To do this, the pattern on the substrate should be reduced to the nanoscale in order to determine if the ZnTe buffer layer can be eliminated. It will be part of this work to

determine if this is possible and if the CSS technique is a viable method for fabricating CdTe films in this manner.

2.3. VARIOUS METHODS OF CDTE EPITAXIAL GROWTH

For many years, the epitaxial growth of CdTe has been performed by different techniques such as metal-organic phase epitaxy (MOVPE), molecular beam epitaxy (MBE), and isothermal close spaced sublimation (ICSS). However, there are several disadvantages in using these techniques for the growth of CdTe films such as slow growth rates, nonuniformity films, and parameters are not easy to control, which makes it difficult to achieve a high quality CdTe film. In addition, these systems require a high cost. For this reason, an alternative technique has being used in this study, the close-spaced sublimation (CSS) technique to develop high quality selective CdTe films for the subsequent growth of HgCdTe. In this section, each epitaxial growth technique will be explained in detail, as well a mention of its advantages and disadvantages for growing CdTe films.

2.3.1. Molecular Beam Epitaxy (MBE) Method

The Molecular Beam Epitaxy (MBE) technique has been recognized as a promising technique for the fabrication of HgCdTe focal plane arrays (FPAs). This technique operates under an ultrahigh vacuum (UHV) and atomic-layer by atomic-layer crystal growth technique based on reaction of molecular or atomic beams with a heated single crystal substrate [37-39]. Furthermore, the source is heated to a desired temperature until it evaporates, resulting in a thermal beam of molecules or atoms that will travel inside the chamber to concentrate on the substrate. Consequently, to achieve high quality epitaxial growth, the sublimation should occur slowly in order for the molecules or atoms to accommodate uniformly on the substrate's surface. The MBE technique distinguishes itself from other evaporation crystal growth methods by its precise control of beam fluxes, control of growth conditions,

and the UHV environments which ensures high purity. Figure 2.4 illustrates a schematic of a common MBE reactor.

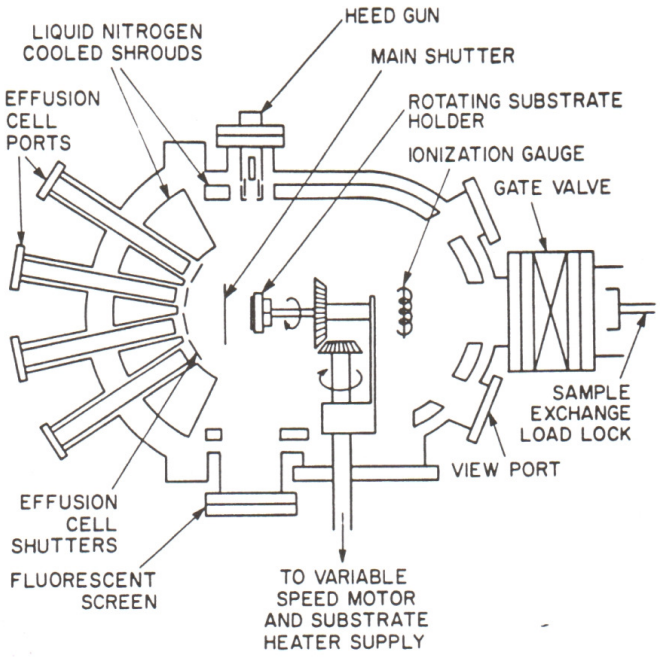


Figure 2.4. Schematic of a typical MBE growth chamber [38].

2.3.2. Metal-organic Vapour Phase Epitaxy (MOVPE) Method

The metal-organic vapour phase epitaxy (MOVPE) technique was developed in the late 1960s, and it has become an important industrial technique for the production of thin solid layers for optoelectronic devices. MOVPE also known as organometallic vapor phase epitaxy (OMVPE), metalorganic chemical vapor deposition (MOCVD), or nometallic chemical vapor deposition (OMCVD) relies on chemical sources (in this case liquid chemicals) at room temperature which are transported inside the reactor by a carrier gas. This technique has been especially designed as a growth technology for large scale fabrication multilayer heterostructure devices [38,39]. During the past years, MOVPE has been the epitaxial growth method of single crystal CdTe and HgCdTe films, because it allows high growth rates at low temperatures [11,12].

2.3.3. Isothermal Closed-Space Sublimation (ICSS) Method

Another effective epitaxial growth technique for semiconductor materials is the isothermal closed-spaced sublimation (ICSS) method. This method is a low cost technique for the epitaxial growth of very thin films of II-IV compounds such as CdSe thin films [45]. Consequently, this technique is similar to the CSS method, but the sources in the ICSS are elemental sources instead of compound sources, and the temperature between the source and substrate is kept constant. In other words, the growth is isothermal and depends on the difference in vapor pressure between the source and substrate. This technique has proved to have good control of the film thickness and works at low temperatures. The operation of the ICSS begins with the sublimation of one source element at a time. Once the substrate is fully covered by the material from the first source, the difference in vapor pressures will disappear because the growing film will be in equilibrium with the vapor of the pure element. Next, the substrate is shifted to the second element source, closing a cycle once equilibrium is reached at the second stage. There have been various studies that demonstrated the growth of CdZnTe, CdSe, and ZnTe/GaAs epitaxial layers by the ICSS technique [42-45]. Figure 2.5 is a schematic of the growth system using Cd and Te elemental sources and H_2 flux.

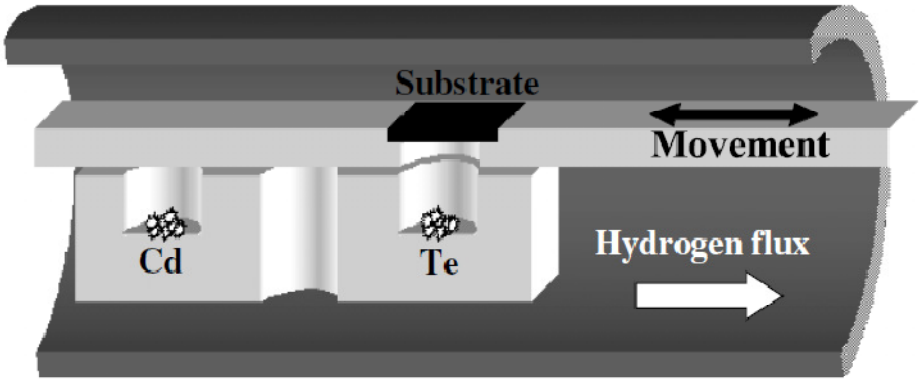


Figure 2.5. Isothermal closed space sublimation reactor used to grow CdTe layers [44].

2.3.4. Closed-Space Sublimation (CSS) Method

The closed-space sublimation (CSS) technique is an effective and low cost system suitable for the epitaxial growth of materials with relatively high vapor pressure. It is a system where the deposition and growth rate depends on four parameters: (1) source temperature, (2) substrate temperature, (3) separation between the source and substrate, and (4) the system pressure [3]. The separation between the source and the substrate should be close enough (approximately ~ 1 mm) in order to allow a wide range of deposition rates, from 0.01 to 4860 μm/hr [6,18]. The close distance between the substrate and the source, where the sublimation occurs, allows the deposition growth rates to be much faster than other epitaxial growth techniques. For this reason, an advantage of the CSS system is the ability to change the separation between the source and the substrate to analyze different deposition growth rates in order to obtain high quality films.

Moreover, the system consists of a vacuum chamber where two graphite blocks are placed inside a quartz tube. The source is placed on top of the bottom graphite block and the glass spacers are positioned between the source and the substrate. Figure 2.6 illustrates the schematic of the CSS reactor and the set up of the graphite blocks, source, substrate and spacers in the liner. The graphite blocks are heated by two halogen lamps, which are facing towards the graphite blocks outside the liner. The temperature of each graphite block is monitored and controlled by two thermocouples, which measures the temperature in Kelvin (K) units and sends the signal to a eurotherm. Labview 7.1 software compares the thermocouple temperature reading to the desired temperature for the source and substrate graphite blocks independently and the power to the lamps is adjusted using a proportional integral derivative (PID). The epitaxial growth is done in a flow of gas, helium or oxygen, with some systems working at different pressures.

The CSS technique has been used for the growth of CdTe polycrystalline films, mainly for solar cells applications. However, limited work has being done to produce planar and patterned CdTe

epitaxial growth. For this reason, the work done in this study relies on the CSS technique to produce patterned CdTe films on Si(100) substrates without the use of a mask for subsequent planar CdTe growth by MBE for HgCdTe infrared detector applications.

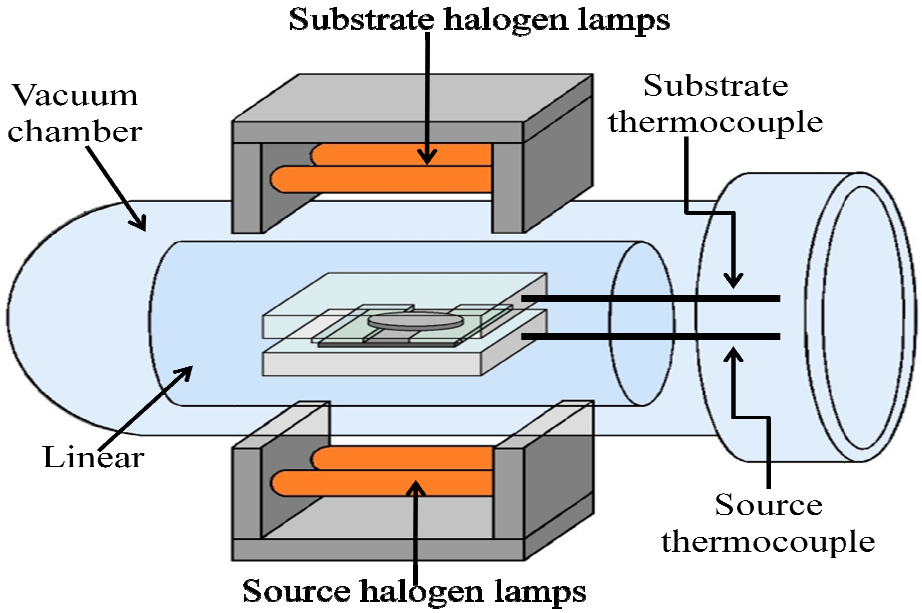


Figure 2.6. Schematic of CSS reactor.

2.4. SIMILAR SELECTIVE CDTE GROWTH BY DIFFERENT METHODS

Partial work has been done on the selective CdTe epitaxial growth on Si substrates to produce thin films for the application of infrared detectors using the CSS. Selective CdTe epitaxial growth on patterned CdTe/Si(211) substrates using a mask layer and depositing the selective CdTe by the CSS technique has been achieved by Quinones *et al.* [13]. Zubia *et al.* performed similar work involving the selective area deposition of CdTe on patterned Si /CdS/ITO/glass, Si /CdS(0001) and /CdS/ITO/glass substrates using the CSS technique [15]. The latter group compared the deposition of planar CdTe to selective CdTe on CdS substrates using Si and masks to reduce the defect density in the CdTe films for the better performance of CdTe/CdS solar cells.

Similar work was demonstrated by Zubia *et al.* [15] and related work by Rodriguez [14], where the selective area deposition of CdTe showed to be an effective technique to improve the CdTe grain uniformity and therefore the efficiency of CdTe/CdS solar cells [14]. Planar CdTe epitaxial growth on CdS(0001), CdTe(111), and GaAs(100) substrates using the CSS reactor has been demonstrated, and nanoheteroepitaxy was recently proposed as a technique to utilize strain relief mechanisms active at the nanoscale to reduce the defect density in lattice mismatched materials and increase the performance of solar cells and infrared detectors [4,15-19].

There is proof of selective growth of CdTe on Si, GaAs and silicon-on-insulator (SOI) substrates using the MOVPE and MBE deposition techniques [10,20-22]. According to R. Zhang *et al.* and R. Sporken *et al.*, the epitaxial lateral overgrowth (EOL) is a new technique to grow low defect density films on lattice-mismatched substrates such as CdTe and HgCdTe films on Si substrates [20,22]. The first requirement to achieve nanoheteroepitaxy is selective growth. Selective growth of CdTe on Si and GaAs substrates using SiN_x and SiO_2 by MOVPE was demonstrated by Zhang and Bhat [20]. Similar work was performed by R. Bommena *et al.* using the MBE deposition method [10,21]. Bommena *et al.* achieved selective growth of CdTe on SOI substrates to grow low defect density CdTe films for the subsequent growth of HgCdTe, where the CdTe films improve the performance of infrared detectors fabricated on the HgCdTe epilayers.

According to the literature mentioned above, there is no work done similarly to the one presented in this thesis in which selective CdTe nanoheteroepitaxy is grown on Si(100) substrates using the CSS technique.

2.4.1. Selective CdTe Growth via CSS Technique

As stated before, S. Quinones *et al.* has achieved selective CdTe single crystal growth on Si(211) substrates using the CSS technique. Si(211) substrates with a CdTe film grown by MBE were patterned

at the micron scale using a Si_3N_4 mask layer and optical lithography, which resulted in 1µm window exposing the CdTe underneath. A thin layer (~10nm) of ZnTe was use as a buffer layer between the CdTe and Si(211) substrate in order to reduce defects at the interface arising from the 19% lattice mismatch between the two materials [13]**.** In order to achieve the desired selectivity, four experiments were conducted which consisted of changing source and substrate temperatures, resulting in different types of selectivity. This work demonstrated that it is possible to achieve CdTe selective deposition of individual 1 µm CdTe grains for substrate temperatures of 450ºC and source temperatures of 530ºC using the CSS technique. Figure 2.7 is an SEM image of the selective growth.

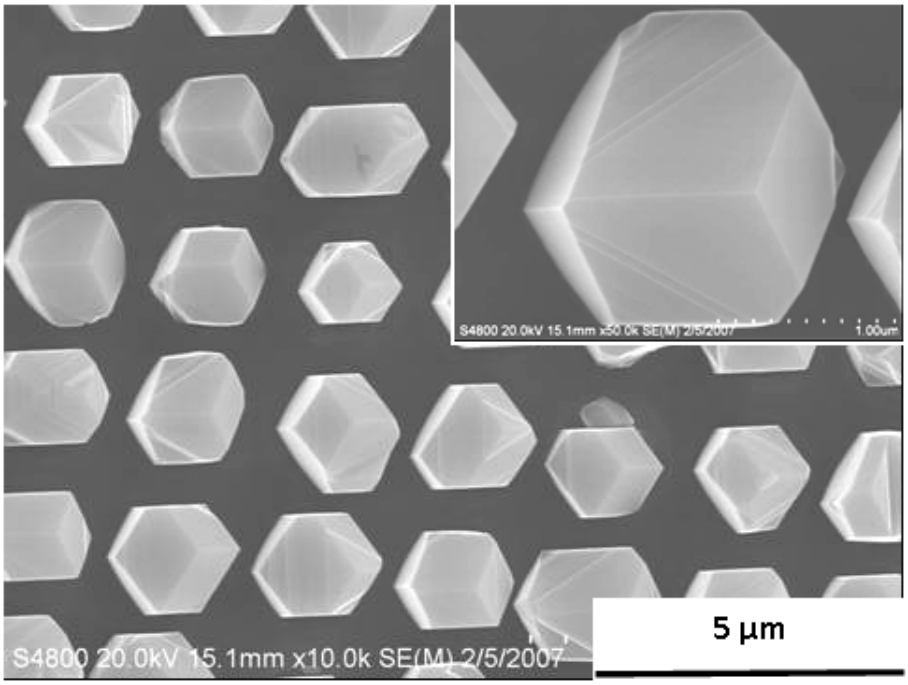


Figure 2.7. Selective deposition of CdTe grains by S. Quinones *et al.* [13].

The quality of these CdTe grains was analyzed using the transmission electron microscope (TEM) which validated the crystalline nature of the grains with the presence of twins (Fig. 2.8) [13]. A high magnification TEM image is included in Fig. 2.8(b) showing the crystallinity of the CdTe grain showing

(111) planes. Fig. 2.8(c) is a STEM cross-sectional image demonstrating two adjacent CdTe grains and the patterned structure.

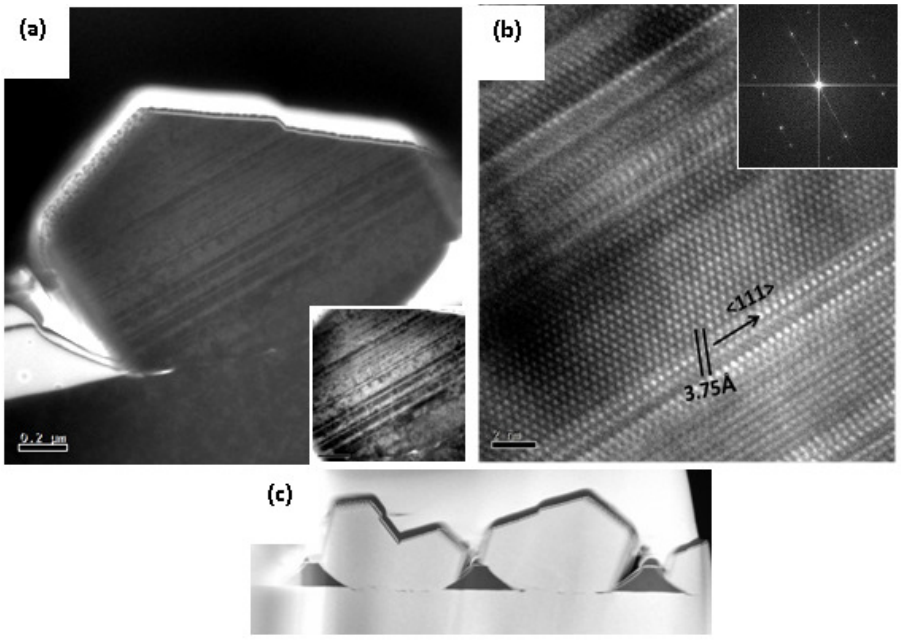


Figure 2.8. TEM results for selective CdTe grains [13].

According to the results obtained by Quinones *et al.*, at low substrate temperatures (350ºC) no selective CdTe deposition was achieved. CdTe was deposited on all surfaces since there was enough surface energy for the CdTe to migrate [13]. It is believed that by decreasing the windows size to the nanoscale (~100 nm), defects such as the twins shown in Fig. 2.8 can be eliminated.

D. Zubia *et al.* and his research group proposed an ordered polycrystalline approach for high performance CdTe/CdS solar cells to overcome the problems related with random polycrystalline thin films, which are grain boundaries and inhomogeneity [15]. His approach consisted of two main steps: (1) the deposition of a patterned growth mask, and (2) the selective-area deposition of the ordered polycrystals, which was investigated using CdTe and CdS. The basic concept of ordered polycrystalline arrays in comparison to random polycrystalline thin films is shown in Fig. 2.9.

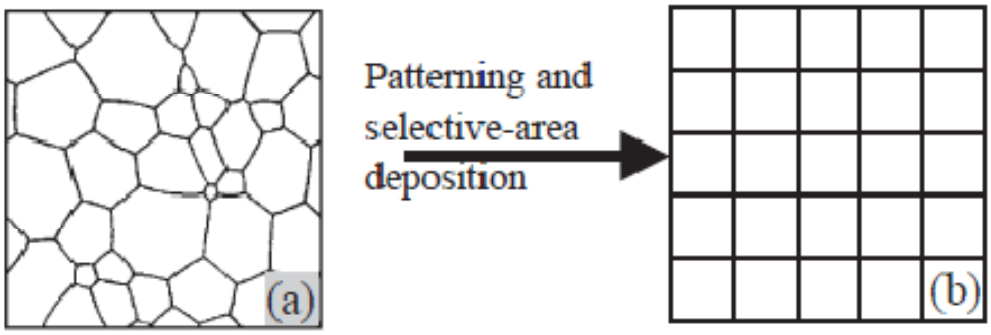


Figure 2.9. (a) The crystal sizes and shapes of films obtained from conventional deposition processes are random, (b) pattering and selective-area deposition is utilized to obtain crystals with ordered crystal grains and boundaries [15].

Zubia *et al.* [15] achieved selective-area deposition of CdTe on patterned SiO_2/CdS/ITO/glass, SiO_2/CdS(0001), and Si_3N_4/CdS/ITO/glass substrates via close-spaced sublimation. The SEM and AFM characterization of selective growth of CdTe on CdS at different temperatures proved that the SiO_2 and Si_3N_4 are effective growth masks and that the temperature is a dominant parameter for selectivity. Furthermore, positive selectivity, meaning that CdTe was deposited on the CdS but not on the SiO_2, was achieved at lower temperatures (Fig. 2.10(a) and 2.11). Zero selectivity where CdTe was deposited on both the CdS and SiO_2 surfaces was achieved at higher temperatures (Fig. 2.10(b)). At high temperatures the selectivity was negative that is, the CdTe was deposited on the SiO_2 but not on the CdS surface (Fig. 2.10(c)). Zubia *et al.* [15] confirmed that the ordered polycrystalline technique has a potential for improving the crystal quality and order of polycrystalline CdTe thin films and the approach appears to be fairly general and could be applied to other materials.

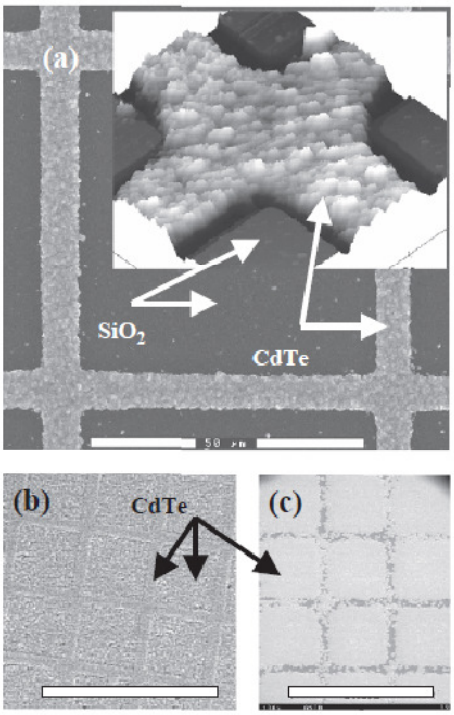


Figure 2.10. Comparison of selective growth of CdTe on CdS versus SiO_2 at temperatures of (a) T_{source}= 575°C, T_{sub}= 550°C, (b) T_{source}= 615°C, T_{sub}= 580°C and (c) T_{source}= 635°C, T_{sub}= 600°C. As the temperature is increased, the selectivity transitions from (a) positive to, (b) zero to (c) negative selectivity. The scale bars indicate (a) 50 µm, (b) 100 µm, and (c) 250 µm. All images are plan view SEM images except for the inset of (a) which is an AFM image [15].

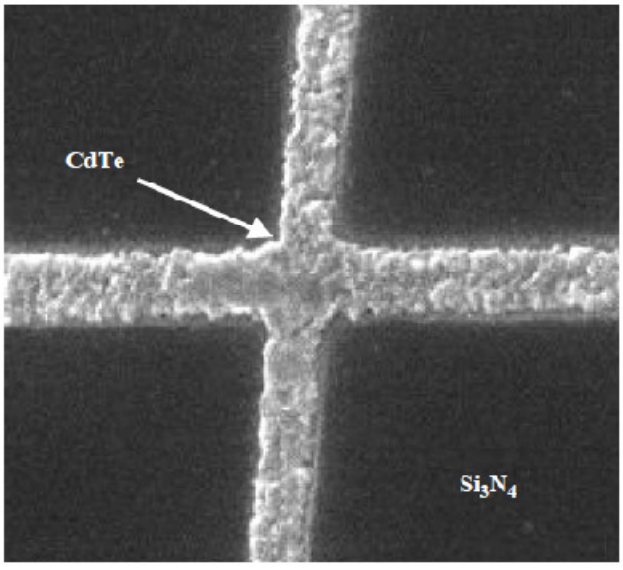


Figure 2.11. Positive selective growth of CdTe on CdS using a Si_3N_4 mask [15].

2.4.2. Selective CdTe Growth via MBE Technique

The strain reduction in selectively grown CdTe by molecular beam epitaxy (MBE) on nanopatterned silicon on insulator (SOI) substrates was reported by R. Bommena *et al* [10,21]. He states that silicon (Si) substrates are an attractive choice for the subsequent growth of HgCdTe infrared detectors because these substrates are available in large areas and quantities at a low cost, and have excellent mechanical properties. However, the drawback of using silicon substrates is the large lattice mismatch of 19% at the interface of CdTe and Si [10,21]. Having a high lattice mismatch between the growing material (CdTe) and the substrate material (Si), results in dislocations being created at the interface to accommodate stress during epitaxial growth [10,21]. Bommena proposed nanoheteroepitaxy (NHE) of CdTe on patterned Si substrates to reduce interfacial dislocation densities. The NHE theory states that stress relief mechanisms are available in three dimensions when the substrate dimensions are reduced to the nanoscale compared to a two-dimensional (2-D) stress relaxation mechanism in macroscopic planar substrates. Furthermore, for material systems with lattice mismatch up to 4.3%, defect-free material can be grown if the substrate dimensions are reduced to 40-50 nm. Strain partitioning between the substrate and the epilayer will lead to a reduction of the strain energy in the material system [10].

In Bommena's work, pattering was performed by the interferometric lithography method using a positive photoresist, which resulted in pillars at the nanoscale. Photoresist pillars were obtained with feature dimensions between 200 nm and 350 nm as shown in Fig. 2.12. The diameter of the silicon islands after the etching process was in the range of 150 nm to 250 nm with pitch between 360 nm and 1000 nm. Reactive ion etching with CHF_3 and O_2 gases was used to create the 2 dimensional nanopillars (Fig. 2.13) [10].

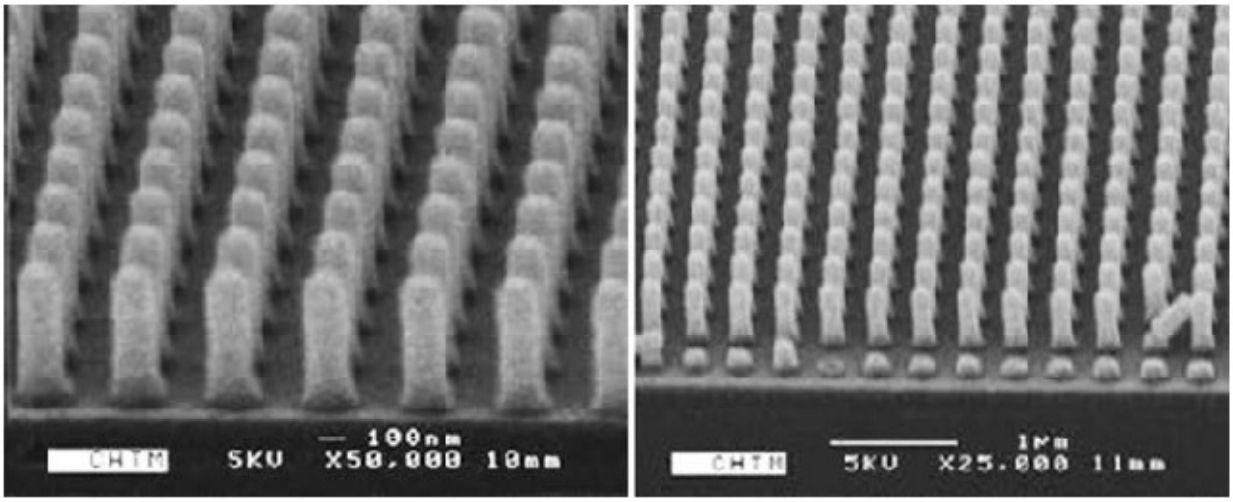


Figure 2.12. SEM images of nanoscale photoresist pillars on SOI substrates fabricated with interferometric lithography [10].

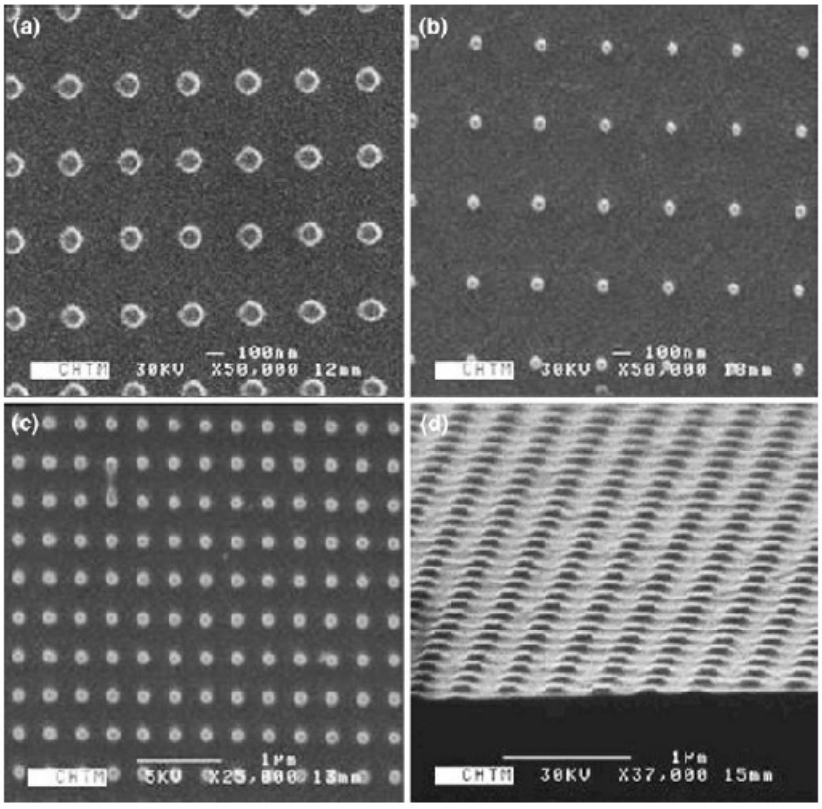


Figure 2.13. (a) ~150 nm silicon nanopillars on a 360 nm pitch, (b) ~200 nm silicon nanopillars on a 500 nm pitch, (c) ~250n nm silicon nanopillars on a 1000 nm pitch, and (d) cross-sectional SEM view of silicon nanopillars on a 500 nm pitch [10].

Once the nanopillars were obtained, CdTe was nucleated on top of the nanopillars at 310ºC using the MBE technique for the first time. Nucleation layers were desorbed at 600ºC and the epilayers were grown at 330ºC, and for 900 s and 3600 s [10]. Since the bond energy between silicon and Te is higher compared to that of silicon dioxide and Te, all the polycrystalline material deposited on the silicon dioxide mask is desorbed during desorption at 600ºC, while a few Te atoms remained on the Si surface of the nanopillars [10]. Therefore, selective CdTe growth on top of the nanopillars was achieved at 330ºC. Figure 2.14 shows the results obtained for the selective CdTe growth on SOI wafers via MBE. In Fig. 2.14(a) no selective CdTe growth occurred because the CdTe epilayer grew without desorption of the nucleation layer. Figure 2.14(b-d) illustrates the selective CdTe growth after the desorption of the initial CdTe layer from the SiO_2 surface.

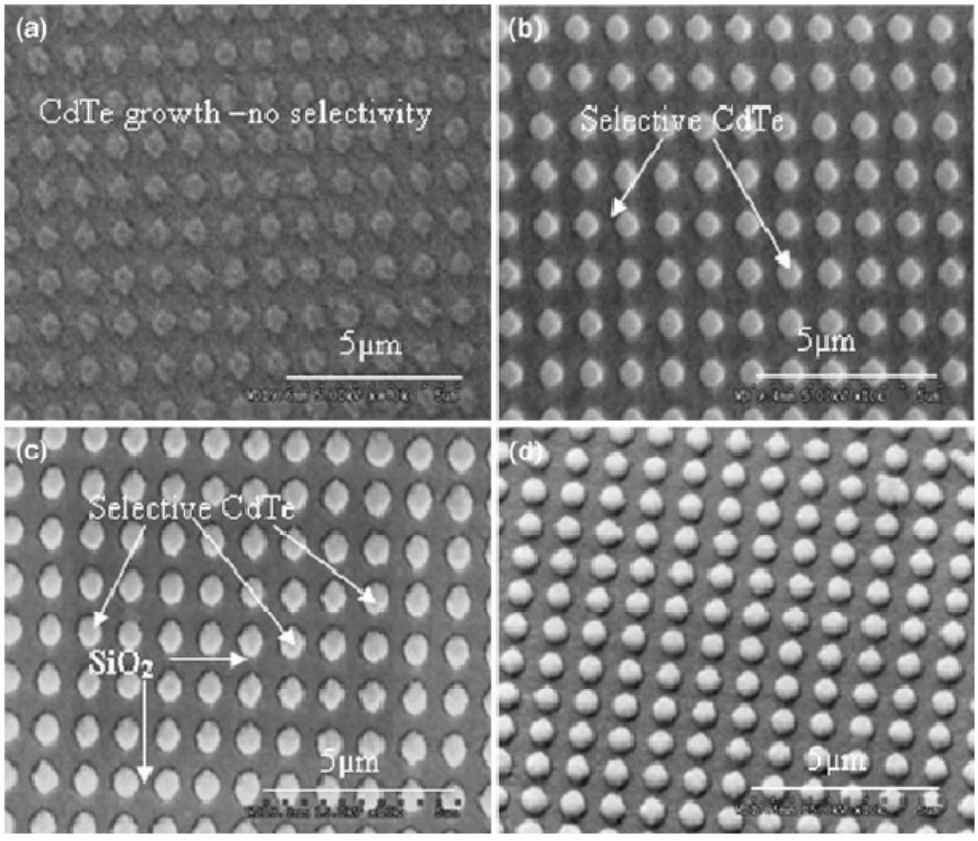


Figure 2.14. (a) CdTe growth from conventional growth process. (b) selective CdTe growth after 900 s of growth, (c) selective CdTe after 3600 s of growth, and (d) angular view SEM of selective CdTe after 3600 s [10].

Overall, Bommena successfully achieved the selective growth of CdTe on SOI(100) substrates via MBE. However, Raman strain characterization demonstrated similar strain for the epitaxial CdTe on planar and nanopatterned substrates. Bommena recommends reducing the lateral dimensions of the silicon nanopillars (>100 nm) to exploit the strain relaxation in three dimensions as predicted by nanoheteroepitaxy (NHE) [10].

The selective growth of CdTe on Si(111) substrates using a hard mask (SiO_2), and a Si(111) substrate covered with by a patterned CdTe seed layer was investigated by R. Sporken *et al.* [22]. Sporken and his research group show that selective growth can be achieved on a patterned CdTe seed layer on Si(111) by implementing the epitaxial lateral overgrowth (ELOG) method. For the ELOG to be possible, selective nucleation must be achieved in addition to a high ratio between lateral and vertical growth rate [22]. In the study by Sporken *et al.*, two experiments were performed using two different types of substrates. The first experiment consisted of the selective epitaxial growth of CdTe on Si(111) substrates using a SiO_2 mask. The substrates were patterned by the optical lithography method. However, selective growth was not successful using a SiO_2 mask.

The second experiment consisted of the selective growth of CdTe on Si(111) substrates covered with a thin (thickness ~0.5 μm) patterned CdTe seed layer using the MBE method at a temperature of 300ºC. The substrates were patterned using the optical lithography technique in order to create parallel stripes. The scanning electron microscope (SEM) image in Fig. 2.15 shows the growth of CdTe on the striped pattern only, and not between the stripes.

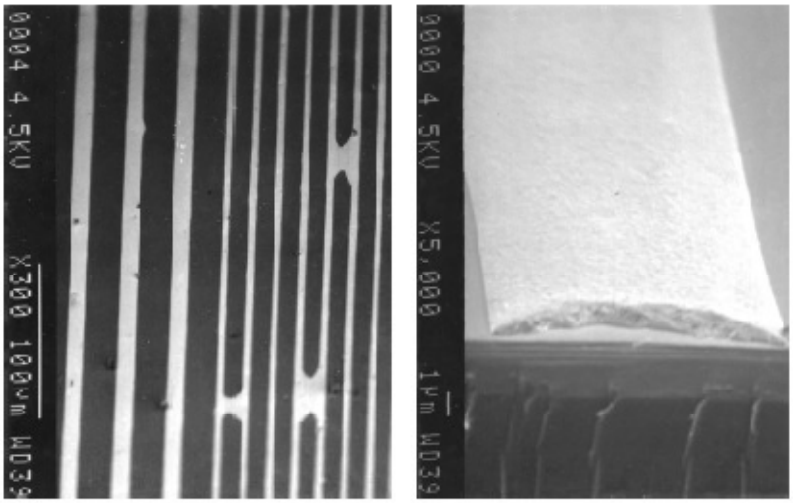


Figure 2.15. Scanning electron microscope image of a) the surface of a CdTe layer grown by MBE on patterned CdTe seed layer on Si (111) and b) the cross-section of the same sample [22].

2.4.3. Selective CdTe Growth via MOVPE Technique

The selective growth of CdTe on Si and GaAs substrates by metalorganic vapor phase epitaxy (MOVPE) was demonstrated by R. Zhang and I. Bhat using a Si_3N_4 mask, where they used the epitaxial lateral growth (EOL) technique in order to grow low defect density thin films on lattice mismatched substrates [20]. In the work by Zhang and Bhat, two different experiments were investigated by applying the ELO technique in order to grow low defect density CdTe and to determine the effects of growth conditions on the selective growth of CdTe. According to Zhang and Bhat the selective growth is mainly influenced by the growth temperature, pressure, substrate and mask materials. Selectivity can be improved by increasing the growth temperature and by decreasing the growth pressure. The first experiment consisted of selective CdTe growth on patterned Si substrates using a SiO_2 mask layer, where the substrate was patterned using the standard photolithography technique in order to create parallel stripes at the micron scale. Consequently, CdTe was grown on Si and SiO_2 surfaces at

temperatures lower than 450°C and pressures higher than 50 Torr as shown in Fig. 2.16(a). For temperatures higher than 450ºC, CdTe grew on the SiO_2 but not on the Si surface (Fig. 2.16(b)).

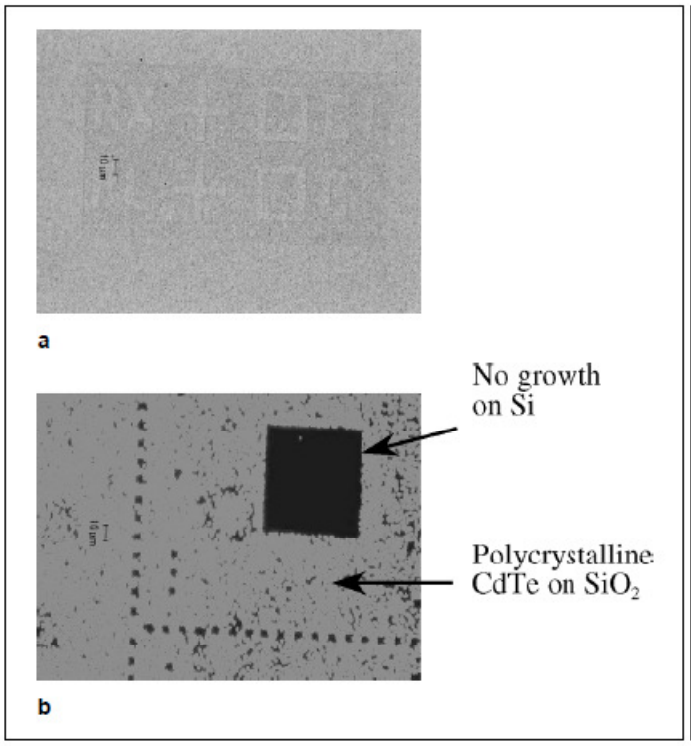


Figure 2.16. Selective growth of CdTe on Si substrate with different mask layers. (a) Growth of CdTe on both Si and SiO_2 when T < 450°C and P > 50 Torr, (b) Polycrystalline CdTe growth on masked SiO_2region, but no growth on Si surface when T > 450°C and P < 50 Torr [20].

Perfect selective growth of CdTe was achieved by Zhang, and Bhat on GaAs and Si substrates using a Si_3N_4 mask layer. The growth temperatures were higher than 525°C and the growth rate was as high as 7-8 µm per hour in order to achieve perfect selectivity on the patterned substrate. Figure 2.17 shows an image of the selective growth of CdTe on both GaAs(100) and CdTe(211)B/Si substrates.

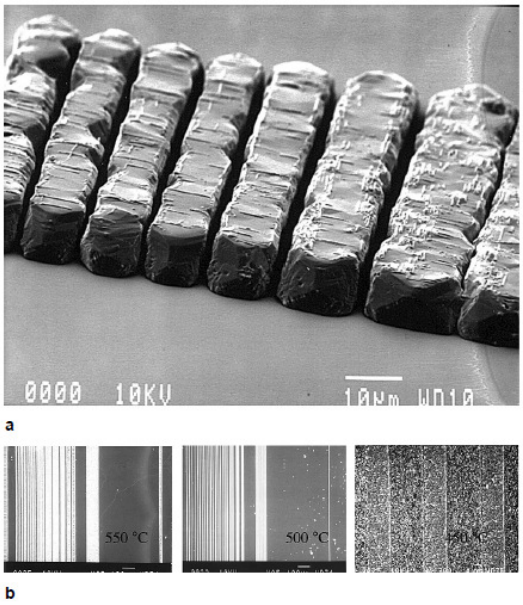


Figure 2.17. Selectivity of the growth of CdTe at different temperatures on (a) GaAs(100) substrate with Si_3N_4 mask layers, (b) CdTe(211)B/Si substrate with Si_3N_4 mask layers [20].

According to Zhang's and Bhat's study, the growth of anisotropic films will improve the morphology of these films. Moreover, anisotropy of the growth rates along different orientations and changing the direction of the mask openings play a significant role in the selective epitaxial growth of CdTe [20,26]. The temperature, pressure, and partial pressures of the precursors affect the vertical and lateral growth rates differently. The vertical growth rates of CdTe films increases significantly with the increase of the growth temperatures and the lateral growth of CdTe depends not only on the differences of the growth rates of the crystallographic planes, but also on the surface diffusion of the precursor atoms on the surface of the mask [20, 26].

Overall, Zhang and his research group confirmed that selective growth can be improved by the use of proper mask materials and by optimizing the growth conditions in order to achieve anisotropic film growth, which will improve the film morphology, as well as the selective CdTe growth of CdTe on Si or the masked region.

In addition to the study mentioned above, Zhang and Bhat investigated the anisotropic growth of metalorganic vapor phase epitaxy (MOVPE) CdTe growth on GaAs(100) and Si(100) substrates using SiO_2, Si_3N_4 or CaF_2 masks [26]. The selective growth of CdTe layer shows strong anisotropy dependence on the orientation of the window pattern mask, as well as on the orientation of the starting substrates. Furthermore, in the experiment where CdTe was grown on Si substrates using a 100 nm SiO_2 mask, the CdTe grew on the Si and SiO_2 surfaces. It is easy for CdTe to nucleate on the SiO_2 mask, since Cd and Te adhere strongly to SiO_2 by forming oxides, and the growth temperature is low enough that these oxides are stable [26]. The second experiment consisted of the selective epitaxial growth of CdTe on GaAs substrates using a 100 nm Si_3N_4 mask. Perfect selectivity was achieved at temperatures as high as 550°C and pressures as low as 25 Torr. Figure 2.18 and 2.19 show SEM images proving the selective growth on patterned 5 µm X 5 µm squares. Figure 2.19 illustrates a difference in CdTe selective growth quality as a function of pattern orientation.

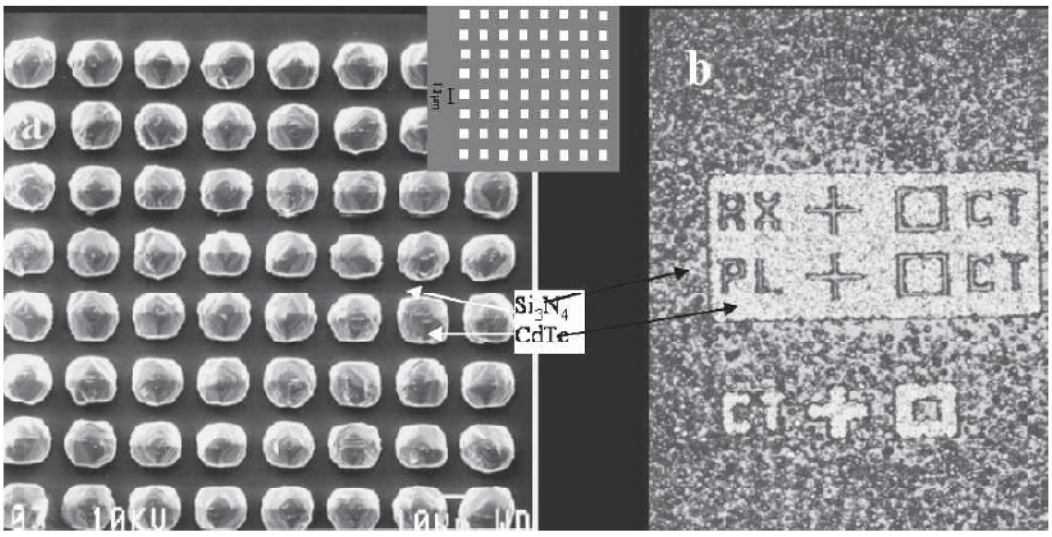


Figure 2.18. CdTe growth on GaAs substrate using Si_3N_4 mask: (a) SEM top view of good selective growth with the inset showing the mask pattern used; (b) optical micrograph of partial selective growth [26].

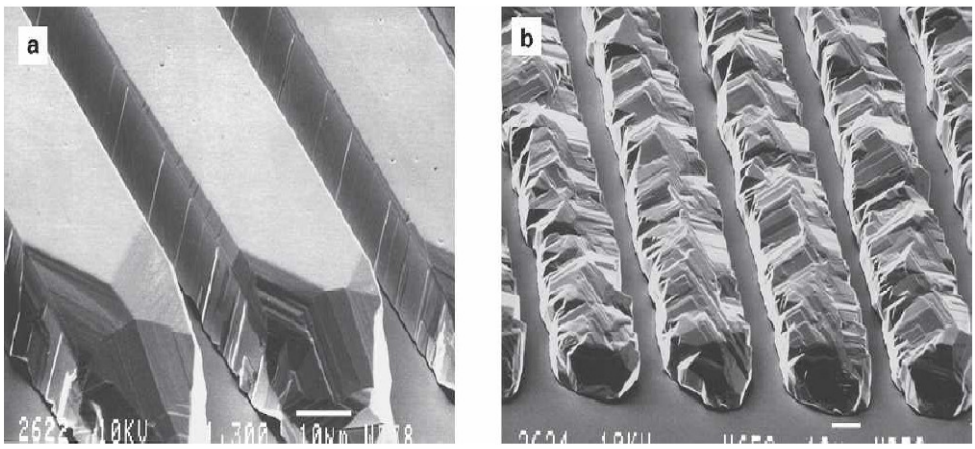


Figure 2.19. SEM top surface of CdTe grown on GaAs (100) substrate: (a) window stripes are along <1 -1 0>; (b) window stripes are perpendicular to the <1 -1 0> direction. Window widths are 5 μm in both cases [26].

The use of a CaF_2 mask also proved to be successful for selective CdTe growth. The CaF_2 layer was first deposited on Si (100) substrate by MBE and then patterned using standard photolithography. The selective growth was achieved via the MOVPE technique at temperatures as low as 450ºC, which is lower than the growth temperature required to achieve selective growth using a Si_3N_4 mask (Fig. 2.18 and 2.19). The optical micrographs of this selective growth are demonstrated in Fig. 2.20, where the feature size of the pattern is as small as 1 μm and as large as 100 μm. These results prove that it is difficult for CdTe to nucleate on the CaF_2 surface due to the low surface free energy of CaF_2, which makes it possible to achieve perfect selective growth of CdTe on Si substrates using a CaF_2 mask at lower growth temperatures [26].

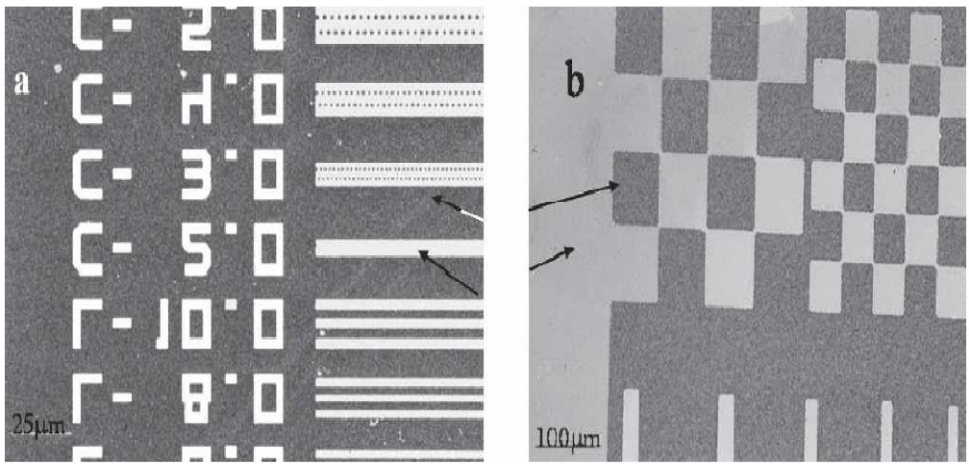


Figure 2.20. (a) CdTe growth on Si substrate using CaF_2 mask. (b) Optical micrograph of good selective growth on a large area [26].

Chapter 3: Experimental Procedure

This chapter includes an explanation about each processing step used to deposit CdTe on CdTe(111), Si(100), and patterned Si(100) substrates using the CSS technique. The ultimate goal of this study is to achieve the selective growth of CdTe on the patterned Si(100) substrates, where the Si substrates are patterned using the optical lithography process. According to previous studies, it is known that dislocations at the CdTe/Si interface can be reduced for selective growth at the nanoscale as a result of dislocation migration to the side walls [21].

In order to accomplish the research goal, the following processing steps were performed in an attempt to obtain high quality CdTe films:

- Photolithography Method.
- Etching Process.
- Lift-off Process.
- Deposition of planar CdTe on CdTe(111) and Si(100) substrates using the CSS.
- Deposition of selective CdTe on patterned Si(100) substrates using the CSS.

The CdTe films were characterized during the of series processing steps using the following characterization tools:

1. Profilometry.
2. Scanning Electron Microscopy (SEM).
3. X-Ray Diffraction (XRD).
4. Transmission Electron Microscopy (TEM).

Each set of experiments as well as the operation of the CSS reactor are explain in detail throughput this section.

3.1. PHOTOLITHOGRAPHY METHOD

In order to pattern the Si(100) substrates, the photolithography method was used to achieve our goal. Photolithography is a process in which a pattern is transferred from a mask to a film on the silicon substrate using ultraviolet light and a light sensitive organic material called photoresist. The first step consists of coating the wafer photoresist which changes its solubility when exposed to appropriate radiation [25]. An important characteristic of the photoresist is that its immunity to chemical etching can be modified by exposure to UV light and heating to higher temperatures. There are two types of photoresist, positive and negative photoresist (Fig. 3.1). A positive photoresist is when the portion of the photoresist that is exposed to light become soluble to the photoresist developer and the portion of the photoresist that is unexposed remains insoluble to the photoresist developer. Likewise, a negative photoresist works in the opposite manner, where the portion of the photoresist that is exposed to light becomes insoluble to the photoresist developer and the unexposed portion of the photoresist is dissolved by the photoresist developer.

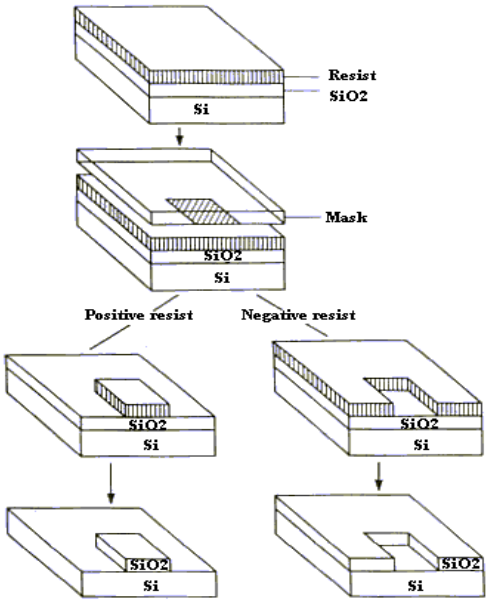


Figure 3.1. Positive and Negative Photoresist [25].

For the purpose of this study, positive photoresists (S1813) and (AZ5214) were used to pattern the Si substrates. However, the (AZ5214) photoresist was reversed to negative photoresist by performing a flood exposure of the pattern.

3.1.1. Sample Preparation for Photolithography Process

In order to achieve a high quality pattern transfer of the Si(100) substrates, it is required to complete a cleaning procedure to the substrate in order to remove any oxide on the substrate's surface before depositing the photoresist on the substrate. The cleaning process consists of the following steps: (1) the substrates were immersed in a basic 5:1:1 ($H_2O:NH_4OH:H_2O_2$) pirahna solution in order to remove all organic contamination on the Si surface, and rinsed with DI water and dried with N_2 gas, and (2) the surface oxide was removed by immersion in a Buffer Oxide Etch (BOE) solution for 1 minute then rinsed with DI water and dried with N_2 gas. This cleaning procedure was followed in this order since the sample preparation is a parameter associated with the successful growth of high quality films.

3.1.2. Parameters for Photoresist (S1813) and (AZ5214) Application

In order to achieve the desired pattern on the Si substrates, the following parameters were varied: (1) spinning speed, (2) pre-exposure bake, (3) exposure time, and (4) developer time. Figure 3.2 includes a flow chart of the photolithography process steps for the negative and positive photoresist, which begins with the dehydration of the substrate on the hot plate at 180ºC for 5 minutes. All the process steps associated with the photolithography procedure for positive and negative photoresist are the same, with the exception of the exposure and developer times. Several experiments were conducted in order to determine optimum parameters for a high quality pattern. After the sample was cleaned as mentioned in section 3.1.1, the positive photoresist (S1813)/(AZ5214) was applied on the sample.

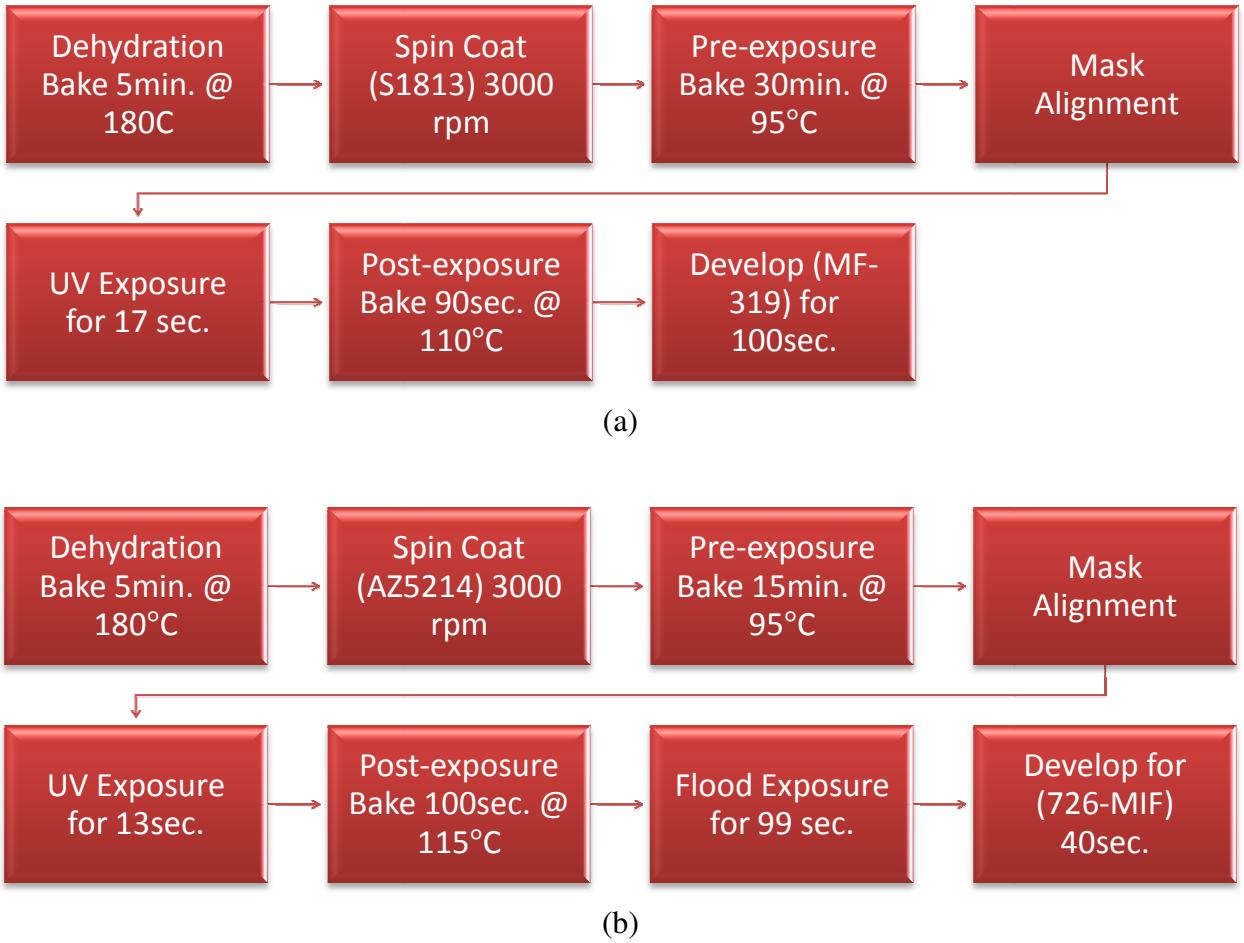


Figure 3.2. Photolithography Process Flow Chart for (a) positive photoresist and (b) for negative photoresist.

After the dehydration step, the substrate is coated with positive/negative photoresist using a spin coater with a speed set to 3000 rpm to produce a uniform thin 1 μm layer (Figure 3.3).

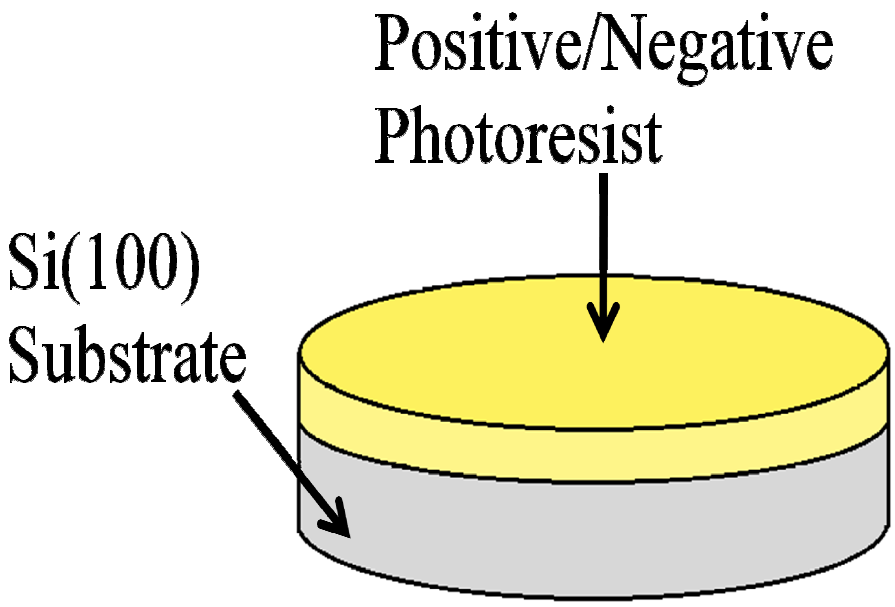


Figure 3.3. Application of photoresist (positive (S1813)/negative (AZ5214)) on substrate.

Subsequently, the substrate was introduced into the oven for a "pre-exposure" bake at 95ºC for 30 minutes for the positive (S1813) photoresist and 15 minutes for the negative (AZ5214) photoresist. This step evaporates the solvents of the photoresist. The dehydration, pre-expose bake, and spinning time parameters were developed by Lopez *et al.* [23]. After the pre-exposure bake, substrates with the positive (S1813) photoresist are exposed to a photomask of ultraviolet (UV) light for 17 seconds using a mask aligner under hard contact mode setup with a total energy dose of 100 mJ/ (Figure 3.4)**.** Substrates with the negative (AZ5214) photoresist are exposed to (UV) light for 13 seconds, followed by a flood exposure of 99 seconds using the mask aligner. The flood exposure is performed in order to reverse the positive photoresist into a negative image of the pattern.

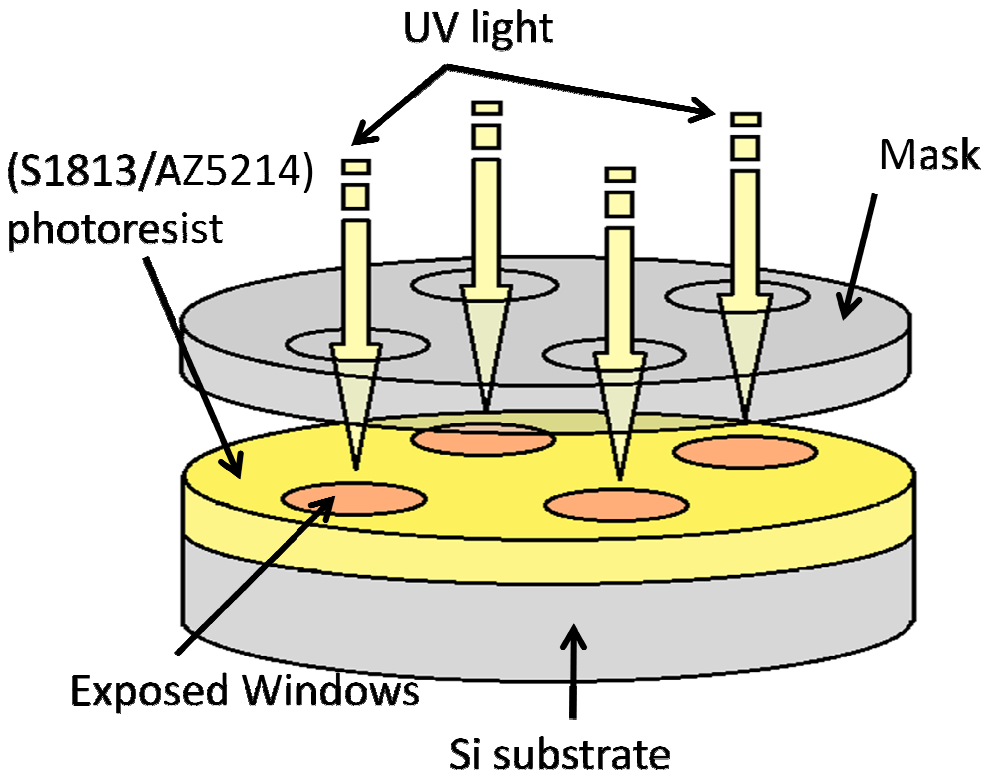
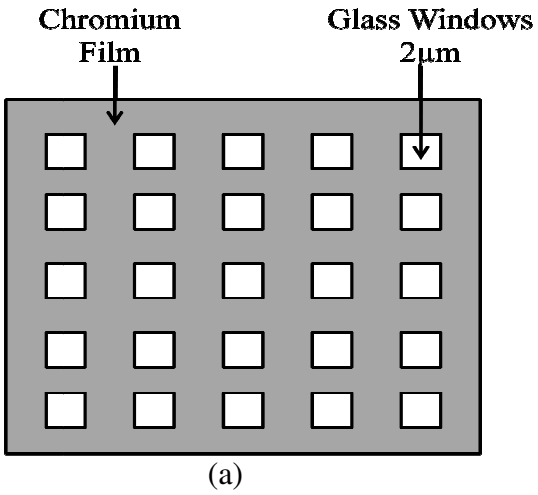
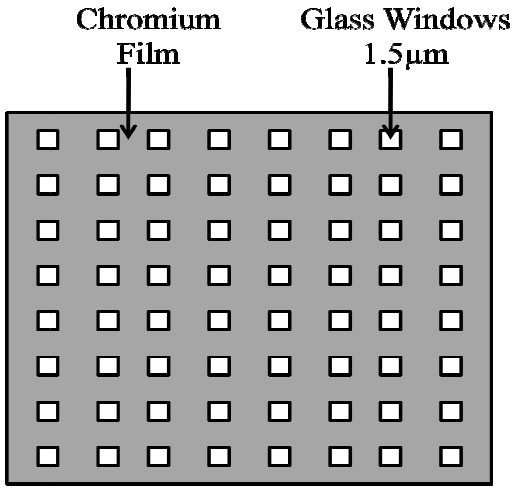


Figure 3.4. Process of UV exposure using positive (S1813) photoresist.

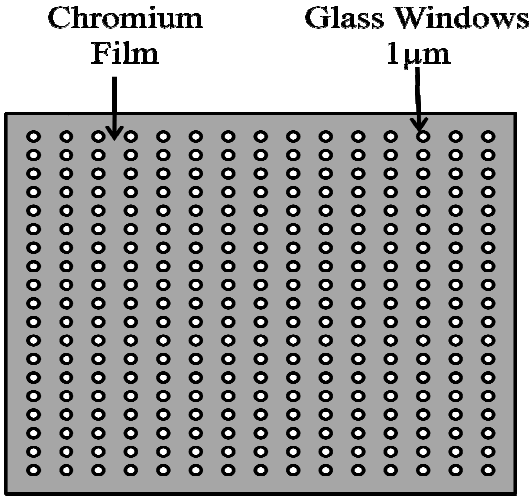
The pattern transfer is performed using a photomask containing four different patterns, which consists of square window arrays with feature sizes in the range of 1-2 microns in increments of 0.5 microns. However, for the purpose of this study only three patterns were used. Figure 3.5 is a schematic of the different feature sizes of the mask; however it is noticeable that the actual shape of the features changes from square to circular as the feature size of the windows decreases. The reason is that the low resolution causes the smaller features to be affected by diffraction when the mask is made.



(a)



(b)



(c)

Figure 3.5. Images of the photomask at different feature sizes (a) 2 µm, (b) 1.5 µm, (c) 1 µm. (Images are not to scale)

As illustrated in Figure 3.5, the gray part of the mask is the chromium film coated glass, which prevents UV light from transmitting through, and the windows where the UV light is transmitted. After the UV exposure, a post exposure bake using a hot plate is performed for 90 seconds at 110ºC for the positive (S1813) photoresist and 100 seconds at 115ºC for the negative (AZ5214) photoresist. This step is performed in order to reduce the standing wave phenomena caused by destructive and constructive interference patterns of the incident light [24]. The final step of the photolithography process is to develop the photoresist, where the unexposed area of the positive photoresist was dissolved and the unexposed area of the negative photoresist was dissolved. Figure 3.6 and 3.7 illustrates the pattern on the substrate after the developer step, for each type of photoresist.

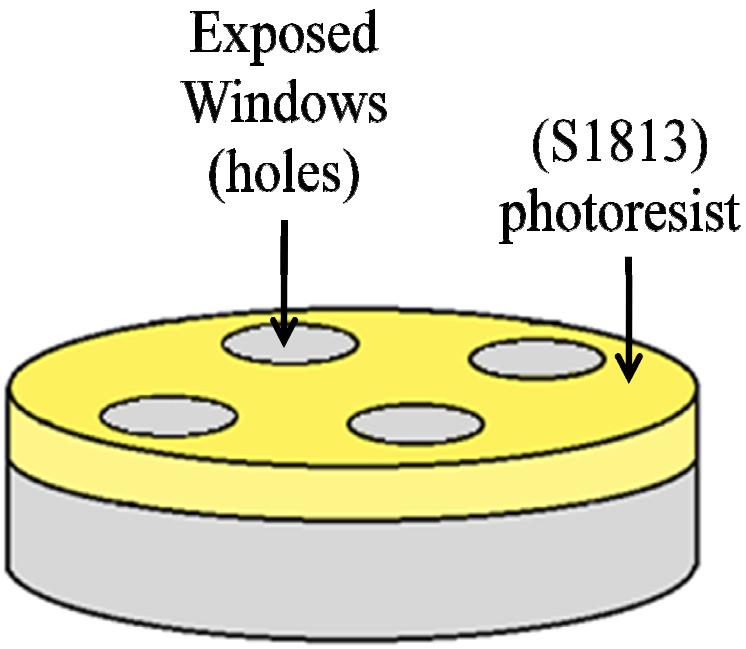


Figure 3.6. Patterned Si substrate with positive (S1813) photoresist.

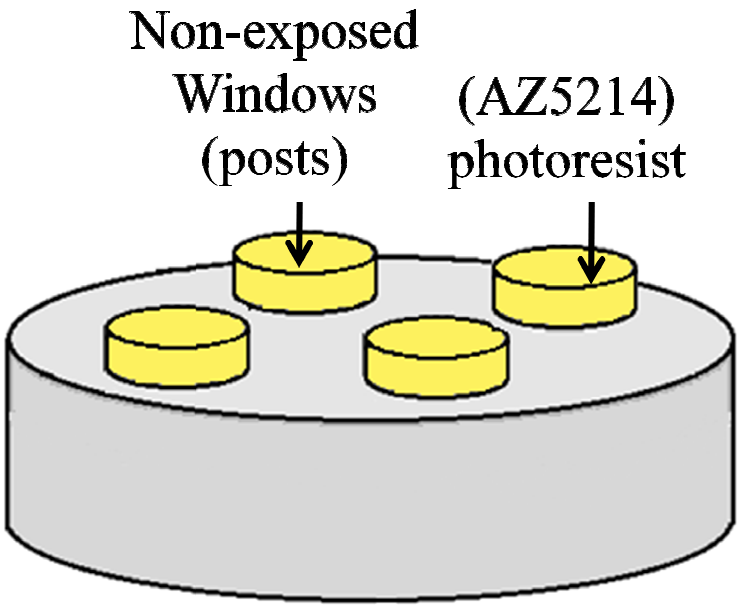


Figure 3.7. Patterned Si substrate with negative (AZ5214) photoresist.

Two different developer solutions were used to form the patterns. The MF-319 developer was used for the positive (S1813) photoresist and the 726MIF developer was used for the negative (AZ5214) photoresist. After the developer step, the pattern shown in Fig. 3.6 and 3.7 was confirmed under the microscope. Nevertheless, in order to obtain these high quality patterns on the Si substrate, several experiments needed to be done to determine the optimal parameters that would result in a high quality pattern. These experiments consisted of changing the exposure and developer times for each type of photoresist and observe the differences on the pattern quality. Table 3.1 and 3.2 shows a summary of the experiments that were performed and the results, where it can be seen that the best exposure time for the positive (S1813) photoresist is 17 seconds and the best developer time is 95 seconds. In addition, the best exposure time for the negative (AZ5214) photoresist is 13 seconds with a 99 seconds flood exposure. The optimum developer time for these samples is 40 seconds.

Table 3.1. Summary of experiments for (S1813) Photoresist.

Positive -S1813 Photoresist (PR)			
Sample	Exposure Time (sec.)	Developer Time (sec.)	Results
1-PPR	14	30	Blurry Pattern
2-PPR	16	75	Some PR left
3-PPR	18	90	A lot PR left
4-PPR	20	115	Not visible
5-PPR	17	90	Visible with little PR left
6-PPR	16	60	Some PR left
7-PPR	17	100	Over develop
8-PPR	17	95	Perfect

Table 3.2. Summary of experiments for (AZ5214) Photoresist.

Negative -AZ5214 Photoresist (PR)				
Sample	Exposure Time (sec.)	Flood Exposure Time (sec.)	Developer Time (sec.)	Results
1-NPR	14	28	25	Some PR left
2-NPR	16	32	30	Blurry
3-NPR	18	36	35	Some PR left
4-NPR	20	40	35	Not visible
5-NPR	17	34	15	Some PR left
6-NPR	13	26	10	Some PR left
7-NPR	13	52	20	Over develop
8-NPR	13	104	60	Over develop
9-NPR	13	102	50	Not visible
10-NPR	13	99	40	Perfect

3.2. DRY ETCHING PROCESS

Etching is the process of using a strong liquid or gas to remove or undercut into a surface. The process in which a strong acid is used to remove or undercut into a surface is called wet etching. When using an ionized gas the process is called dry etching. For the purpose of this study, the dry etching process was used to create pillars (positive photoresist) and pillars (negative photoresist) on the pattern substrate as illustrated in Figs. 3.8 and 3.9 respectively.

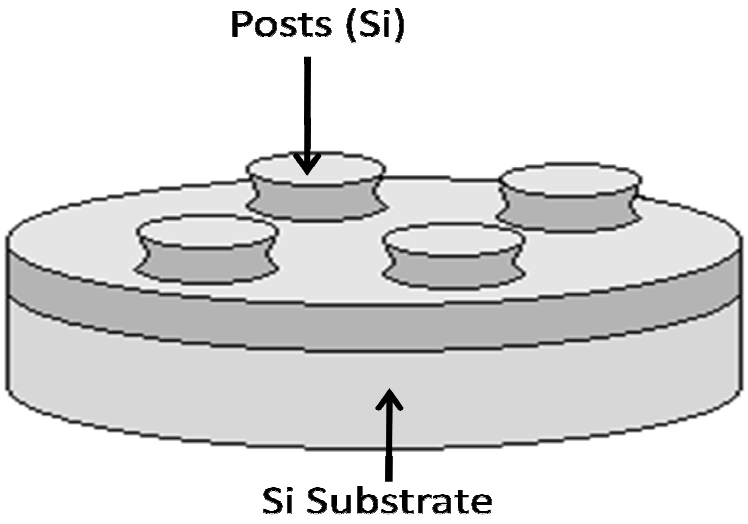


Figure 3.8. Patterned substrate after etching procedure using (S1813) photoresist.

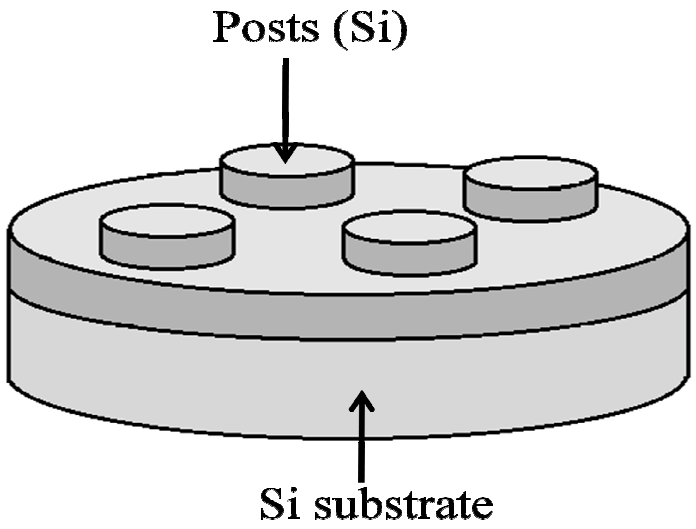


Figure 3.9. Patterned substrate after etching procedure using (AZ5214) photoresist.

Furthermore, there are two types of etching techniques, anisotropic and isotropic etching. Anisotropic etching is the process where the etching occurs preferentially in one direction, whereas isotropic etching occurs equally in all directions. For the purpose of this study, the two etching techniques were taken into consideration since the size of the pillar needed to be reduced in diameter at the same time that the pillar was being created. An Oxford Plasmalab etcher was used as part of this study. A sulfur hexafluoride (SF_6) gas was used to achieve isotropic etch on silicon (Si). The etching process was studied and optimized in order to obtain a high quality pattern on the substrate. Several parameters were examined such as the flow of gas (SCCM), RF power (Watts), gas pressure (Torr) and the time of the etching process (min.). Moreover, the gas pressure and the RF power are the parameters that need to be adjusted to result in isotropic or anisotropic etching of the substrate. Table 3.3 includes an outline of the experiments that were performed in order to obtain the optimized parameters for the etching process. The smallest pillars obtained were 450 nm in diameter and were a result of the negative photoresist process.

Table 3.3. Summary of experiments for dry etch of Silicon using SF6 gas.

Dry etching for Silicon-PlasmaLab					
Sample	Gas Flow (sccm)	RF Power (watts)	Gas Pressure (Torr)	Etching Time (min.)	Results -Post Size
1-PPR	25	75	0.03	3	Need to etch more
2-PPR	25	75	0.03	3.3	Need to etch more
3-PPR	25	100	0.03	4	Need to etch more
4-PPR	30	120	0.06	5	1 µm
5-PPR	30	170	0.07	9.30	600 nm
6-PPR	30	130	0.05	3.45	1.5 µm
2-NPR	30	160	0.05	4	1.5 µm
3-NPR	30	170	0.07	3.45	1 µm
5-NPR	30	180	0.1	3.45	450 nm
6-NPR	30	170	0.09	3	500 nm

**NPR=Negative Photoresist and PPR=Positive Photoresist.*

3.3. PHOTORESIST LIFT-OFF PROCEDURE

Photoresist remains on the substrate after the etching process and is removed using a lift-off procedure. The lift-off procedure is a process where the substrate is immersed into a chemical solution to remove all the photoresist remaining on the substrate. The chemical solution used in this experiment was pirahna (H_2SO_4:H_2O_2) with a ratio of 5:1. The substrate was immersed in the solution for 10 minutes at 130ºC.

3.4. OPERATION AND PARAMETERS OF CSS REACTOR

Figure 3.10 is a schematic of the substrate and source set-up inside the CSS reactor. The source is placed on top of the first graphite block, aligned in the center. The glass spacers are placed on top of the source separated by approximately 1 inch. The substrate is placed on top of the spacers, and the second graphite block is placed on top of the substrate. Once the source and substrate set-up is complete, and the graphite blocks are inserted into the thermocouples, the liner and vacuum chamber are placed around the sample set-up as illustrated Fig. 3.11. Two 1000 W halogen lamps are located outside the reactor and are used to provide thermal energy to the source and substrate graphite blocks. The temperature of each graphite block is monitored and controlled by two thermocouples, which measures the temperature in Kelvin (K) units and sends the signal to a eurotherm. Labview 7.1 software compares the thermocouple temperature reading to the desired temperature for the source and substrate graphite blocks independently and the power to the lamps is adjusted using a proportional integral derivative (PID). The reactor has the advantage of flowing helium and oxygen gas inside the chamber and the pressure is controlled by the MKS mass flow controllers. For the purpose of this experiment, only the helium gas was used. The software displays a table, where the user inputs the parameters to create a growth recipe. The separation between the source and substrate was kept at 1 mm for each experiment

using 1 mm glass spacers. The close distance between the source and substrate allows for very fast deposition rates, from 0.01to 4680 µm/hr [3,6,18].

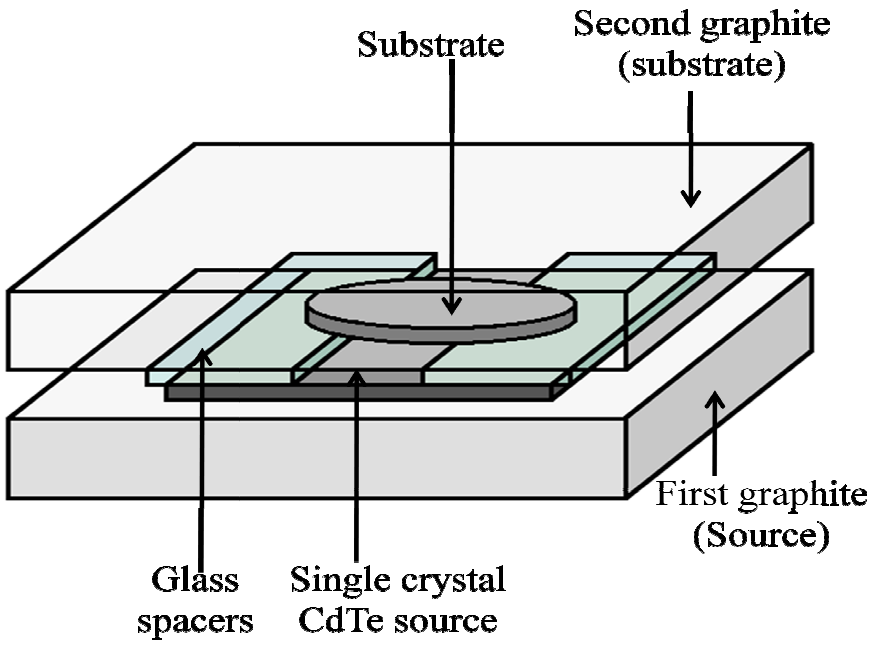


Figure 3.10. Schematic of source and substrate set up in CSS.

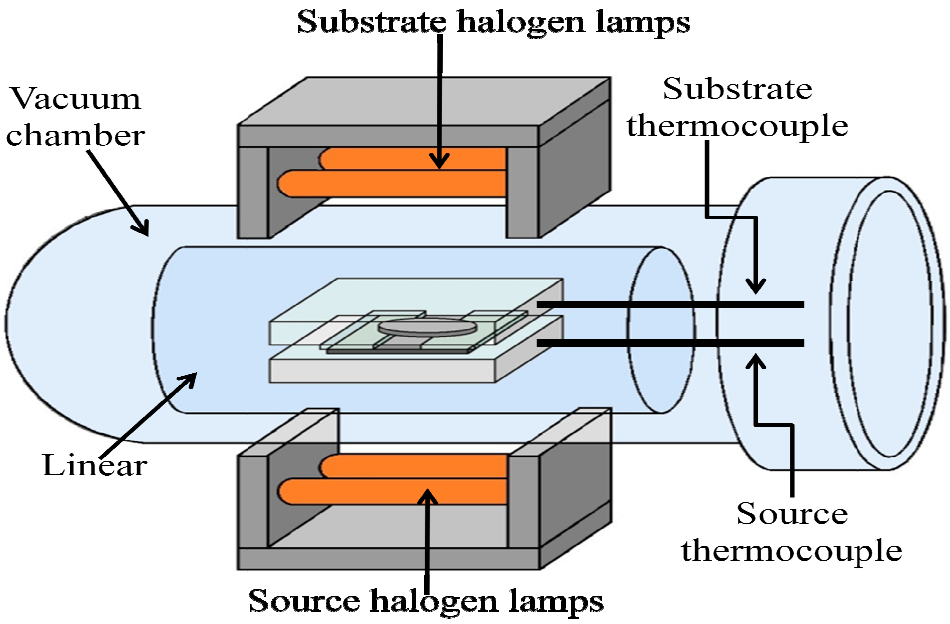


Figure 3.11. CSS reactor.

Using the CSS reactor, it is possible to control the following parameters using the software mentioned above:

- Step time (sec.)
- Helium flow (SLPM)
- Oxygen flow (SLPM)
- Substrate temperature (ºC)
- Source temperature (ºC)
- Pressure inside vacuum chamber (Torr)

For this study, only the source temperature, substrate temperature, deposition time and annealing time were varied, all other parameters were held constant.

3.5. DEPOSITION OF PLANAR CDTE ON SI (100) AND CDTE(111) VIA CSS.

The conditions used for the deposition of planar CdTe on Si(100) substrates was based on the thesis work performed by A. Escobedo [3]. The work done by Escobedo focused on the optimization of the parameters listed in section 3.4 for the deposition of CdTe on CdTe(111) substrates by the CSS technique. In this work, several experiments were conducted to determine the optimum parameters for the deposition of CdTe on Si(100) substrates. The basic procedure, developed by Escobedo was used and only the source temperature, substrate temperature, and deposition time were varied. In this section, the experiments performed are explained in detail starting with the sample cleaning procedure.

3.5.1. Sample Cleaning Procedure for Si(100) and CdTe(111)

The successful growth of high quality CdTe films begins with the sample preparation procedure. The sample is first cleaned, in order to remove particles and organics from the surface. After cleaning

the surface, the wafer is etched immediately before deposition, so that the native oxide is removed prior to insertion of the sample into the CSS reactor. The Si(100) substrates were obtained from University Wafer Company, where they were treated with a chemical polish. The sample cleaning procedure consists of immersing the substrate in a pirahna solution ($H_2O:NH_4OH:H_2O_2$) with a ratio of 5:1:1 for 5 minutes then rinsing with Di water and drying with nitrogen gas. Next, the sample is etched in 100 mL of Buffer Oxide Etch (BOE) for 1 minute and then it is rinsed with DI water and dried with nitrogen gas. After the samples are dried with nitrogen, they are immediately placed on the graphite blocks of the CSS reactor as illustrated in Fig. 3.10.

Several attempts were made to reproduce Escobedo's work of high quality CdTe film growth on CdTe(111) substrates. The CdTe(111) substrates were cleaned in a similar manner as the Si(100) substrates. First, the samples are immersed in an ultrasonic acetone bath for 5 minutes, follow by an ultrasonic methanol bath for 5 minutes and in DI water for 5 minutes. The samples are then rinsed and dried with nitrogen gas. Lastly, the samples are etched for 10 seconds in 0.25 mL of Br_2 and 100 mL of dried methanol. The samples are rinsed and dried with nitrogen gas. After the samples are dried with nitrogen, they are immediately placed on the graphite blocks of the CSS reactor as illustrated in Fig. 3.10.

3.5.2. Deposition Technique

The CSS parameters used to deposit CdTe on the Si(100) substrates were based on the work of Escobedo, who studied the growth of CdTe on CdTe(111) substrates via CSS. However, several experiments were required in order to improve the quality of the CdTe on Si(100) substrates. The planar deposition of CdTe consisted of 3 steps: (1) a pre-heat step, (2) deposition step, and (3) an in-situ annealing step. The annealing step was added to the recipe by Escobedo [3] in order to improve the quality of the film, where this step helps to eliminate grain boundaries. Moreover, the pre-heat and

annealing steps were added to the recipe to avoid pinholes in the CdTe film, which result in higher dislocation densities. These steps were also incorporated into the recipe by Escobedo [3]. The only parameters that were modified for the current work were the source and substrate temperatures, the deposition times, and the annealing times. Table 3.4 includes details about the CdTe growth on Si(100) substrates performed in this work. CdTe was also deposited on CdTe(111) in order to try to duplicate Escobedo's work, but was not successful. Table 3.5 includes similar information for the CdTe growth on CdTe(111) substrates.

Table 3.4. Summary of samples performed for the planar CdTe epitaxial growth on Si(100) substrates.

Sample Name	Source Temperature (ºC)	Substrate Temperature (ºC)		Deposition Time	Annealing Time
	Set Point	Set Point	Actual		
S350530	530	350	395	1 hr.	30 min.
S2350530	530	350	395	2 hr.	1 hr.
S325530	530	325	418	2 hr.	1 hr.
S300530	530	300	417	2 hr.	1 hr.
S350520	520	350	395	1 hr.	30 min.
S450550	550	450	450	2 hr.	1 hr.

Table 3.5. Summary of samples performed for the planar CdTe epitaxial growth on CdTe(111) substrates.

Sample Name	Source Temperature (ºC)	Substrate Temperature (ºC)		Deposition Time	Annealing Time
	Set Point	Set Point	Actual		
SP400530	530	400	404	2 hr.	1 hr.
SP350530	530	350	411	2 hr.	1 hr.
SP350520	520	350	403	2 hr.	1 hr.
SP350510	510	510	396	2 hr.	1 hr.

As mentioned previously, a single crystal CdTe(111) source with twins was used as a sublimation source. Prior to the CdTe deposition, the source was annealed for 30 minutes at 600ºC, in

order to produce more repeatable growth rates. Moreover, the substrate temperature was increased in steps of 25ºC from 300ºC to 350ºC, and the source temperature was kept at 530ºC. However, for one sample the source temperature was decreased to 520ºC to observe any effects on the film quality. For the last experiment performed in this part of the study, the source temperature was set to 550ºC and the substrate temperature to 450ºC. The source temperature had an effect on the substrate temperature due to closeness between the source and the substrate, and therefore, the set substrate temperatures and actual substrate temperatures are reported. The deposition of CdTe with a pre-heat and in-situ annealing steps consists of ten steps, where the first three steps are associated with the purging process of the chamber as shown in Table 3.6, and the other seven steps are the pre-heat, deposition and annealing steps as shown in Table 3.7.

Table 3.6. Purging process for CSS chamber.

	Purging Steps					
Time (sec.)	60	60	60	60	60	60
He Flow (SLPM)	0	4	0	4	0	4
O_2 Flow (SLPM)	0	0	0	0	0	0
Sub. Temp. (ºC)	0	0	0	0	0	0
Sou. Temp. (ºC)	0	0	0	0	0	0
Pressure (Torr)	0.1	100	0.1	100	0.1	100

Table 3.7. Recipe parameters for CdTe deposition with pre-heat and in-situ annealing steps.

	Pre-heat (1)	Pre-heat (2)	Dep. Ramp (1)	Dep. Ramp (2)	Deposition	In-situ anneal	Cooling
Time (sec.)	190	1200	180	280	7200	3600	120
He Flow (SLPM)	0.1	0.1	0.1	0.1	0.1	0.1	0
O_2 Flow (SLPM)	0	0	0	0	0	0	0
Sub. Temp. (ºC)	250	250	350	350	350*	428	0
Sou. Temp. (ºC)	0	0	400	530	530*	0	0
Pressure (Torr)	5	5	5	5	5	5	0.1

**Different experiments were performed by varying the substrate and source temperatures as shown in table 3.4.*

During the purging of the CSS reactor, the reactor is evacuated and then purged to 100 Torr of helium flow at 4 SLPM for 60 seconds (Table 3.6). Next, the pre-heat step is performed by setting the substrate temperature to 250ºC for 20 minutes under helium at 5 Torr. During the pre-heat step, the source temperature is set to zero but reaches ~206ºC due to the closeness of the substrate to the source. The first deposition ramp increases the substrate temperature to the set value and increases the source temperature to 400ºC. The second deposition ramp increases the source temperature to its set value. The implementation of these two deposition ramps to the CdTe growth was performed in order to obtain a better control and stabilization when increasing the source and substrate temperatures. After reaching the desired source and substrate temperatures, the deposition process was performed for 1 or 2 hours. The actual substrate temperature increased to values between 400ºC and 428ºC as a result of heat flow from the source. After the deposition step, annealing was performed for half the deposition time by setting the substrate temperature to values between 350ºC and 400ºC and the source temperature to 0ºC. (See Table 4.1)

3.6. DEPOSITION OF SELECTIVE CDTE ON SI(100) VIA CSS

The deposition of selective CdTe on Si(100) substrates was performed after obtaining the best source and substrate temperature parameters for the growth of high quality planar CdTe films. These parameters were used as a guide for the selective growth of CdTe films. As mentioned in the literature review section, it is believed that growing CdTe selectively will reduce dislocations at the interface between CdTe and Si. Once the micron to nano-scale pillars were created on the Si substrates, the next step was to deposit CdTe grains on top of the pillars via CSS. A CdTe(111) single crystal with twins was used as a sublimation source for this study. Furthermore, prior to the CdTe deposition the source was annealed for 30 minutes at 600ºC, in order to produce repeatable growth rates.

3.6.1. Sample Cleaning Procedure

The Si(100) substrates were cleaned again prior to selective growth in the same manner as described in section 3.3 for the lithography procedure. The cleaning procedure of the sample consisted of two steps. First, the sample was immersed in pirahna solution (H_2SO_4:H_2O_2) with a ratio of 5:1 for 10 minutes at 130ºC. Then, the sample was immersed in BOE for 10 seconds to remove the native oxide on the surface. Finally, the sample was rinsed with DI water and dried with nitrogen gas. Immediately after the sample was cleaned, it was introduced into the CSS reactor as shown in Figure 3.10 and 3.11.

3.6.2. Deposition Technique

Several experiments were performed to achieve selective growth of CdTe on patterned Si(100) substrates. The deposition steps used for this study were based on the results by Escobedo [3], where he deposited CdTe on patterned Si(211) substrates using a Si_3N_4 mask layer. In this study, similar deposition parameters were optimized, but the CdTe grains grew selectively on the Si pillars without the use of a mask. Tables 3.8 includes a summary of the experiments performed for selective CdTe growth and include the source and substrate temperatures, deposition time, warm-up step parameters, and the pattern size.

Table 3.8. Summary of experiments performed for the selective CdTe epitaxial growth.

Sample	Tsub (ºC)	Tsou (ºC)	Warm-up steps	Deposition Time (min.)	Pattern Size
S2-PPR	450	530	No	15	1.5 µm
S2-NPR	450	530	No	15	1 µm
S1-NPR	440	530	Yes	15	1 µm
S3-NPR	450	550	Yes	5	1 µm
S4-NPR	450	540	Yes	5	1 µm
S5-NPR	450	530	Yes	5	450 nm
S5(2)-NPR	450	530	Yes	5	450 nm
S6-NPR	450	530	Yes	5	500 nm
S8-NPR	450	550	Yes	15	500 nm
S9-NPR	450	540	Yes	15	500 nm
S10-NPR	450	560	Yes	5	1 µm

**Note: NPR=Negative photoresist and PPR=Positive photoresist*

For all source and substrate temperatures, as wells as the deposition times, selective CdTe growth was observed to varying degrees of uniformity. The source temperature was varied between 520ºC to 560ºC in order to determine its effect on grain size. The deposition time varied between 5 minutes to 15 minutes in order to determine if deposition time had an effect on CdTe pattern uniformity. The selective CdTe deposition consists of seven reactor steps, where the first three steps (1)-(3) are related to the purging process. The remaining steps are (4) the warm-up step, (5) the deposition ramp step, (6) the deposition step, and (7) the cooling step (Table 3.9). However, the first sets of experiments were performed without the warm-up and deposition ramp steps to observe the effect of the film quality without including these two steps in the deposition process.

Table 3.9. Typical recipe for the selective CdTe epitaxial growth on Si (100) substrates.

	Purging Steps						Warm-up	Dep. Ramp	Deposition	Cooling
Time (sec.)	60	60	60	60	60	60	300	240	300*	180
He Flow (SLPM)	0	4	0	4	0	4	0.1	0.1	0.1	0
O_2 Flow (SLPM)	0	0	0	0	0	0	0	0	0	0
Sub. Temp. (ºC)	0	0	0	0	0	0	250	450	450	0
Sou. Temp. (ºC)	0	0	0	0	0	0	0	550	550*	0
Pressure (Torr)	0.1	100	0.1	100	0.1	100	5	5	5	0.1

**Different experiments were performed by changing the source temperature from 520ºC to 540ºC in step of 10□C, as wells as the deposition times as shown in table 3.7.*

The warm-up and deposition ramp steps were designed in order to improve the quality of the CdTe grains deposit on the substrate. Furthermore, the warm-up step was achieved by heating the substrate temperature to 250ºC for ~5 minutes, follow by a deposition ramp step where the substrate temperature was set to 450ºC and the source temperature to 530ºC for ~3 minutes. Figure 3.12 illustrates a graph of the time-temperature profile of sample 3-NPR, where the deposition time was 5 minutes.

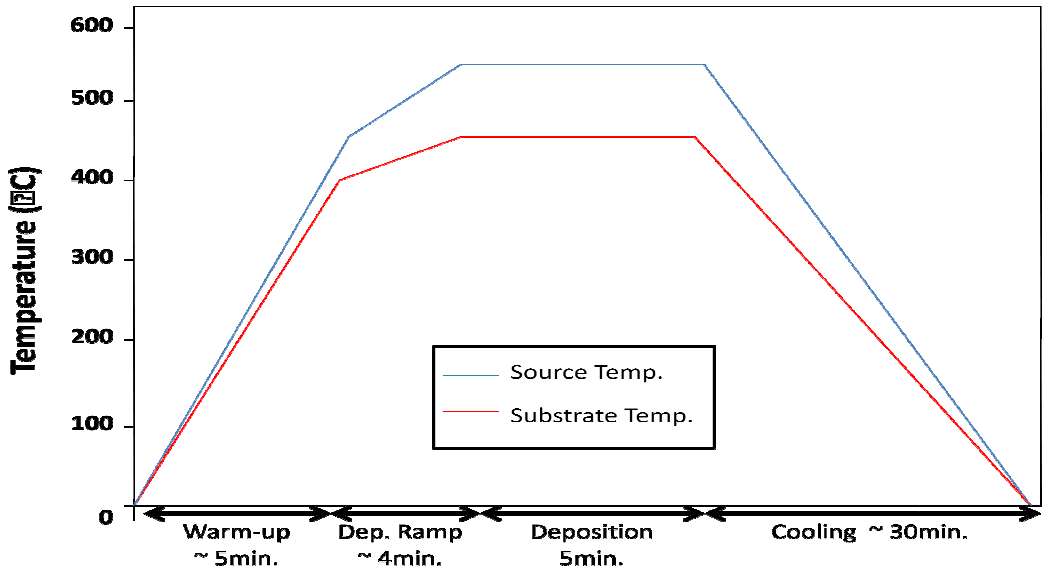


Figure 3.12. Graph of time-temperature profile for a Selective CdTe epitaxial growth with a warm-up and deposition ramp step.

3.7. CHARACTERIZATION METHODS

In order to analyze the high quality selective and planar CdTe films performed in this study, three different characteristic methods were used. All samples performed in this study were characterized using the scanning electron microscopy (SEM). However, the film structure was characterize using two methods, the x-ray diffraction (XRD) method for the planar CdTe films and the transmission electron microscope (TEM) for the patterned CdTe growth. The thickness of the planar CdTe films was measured using a KLA Tencor Alpha-Step IQ Profilometer.

3.7.1. Profilometer Method

The samples in this study were characterized by the profilometry technique (KLA Tencor Alpha-Step IQ Profilometer), where the thickness of the film was measure by moving a stylus across the film. The stylus movements are recorder and calculated using a computer interface, and then the results are plotted on a graph. The graph shows the x-axis representing the distance the stylus moves horizontally, and the y-axis representing the vertical movement of the stylus. The scan for each sample was performed at 50 µm/s, and a sampling rate of 50 Hz along the center of the sample. This measurement was done to obtain the film topography and analyzed the growth rate of the film.

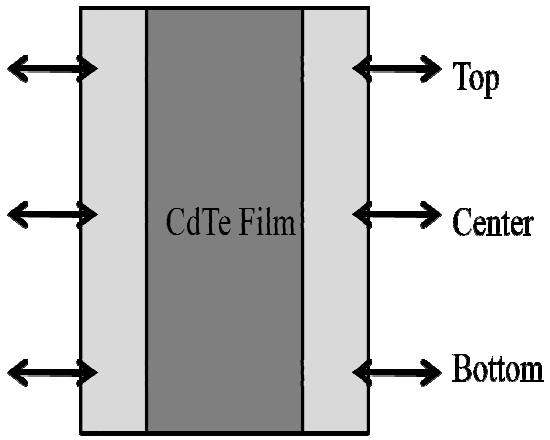


Figure 3.13. Si substrate with CdTe growth on top where the direction of the arrows identify the location where the stylus follows the path to be measure.

Several measurements were performed across different locations of the substrate to verify thickness uniformity across the sample as shown in Fig. 3.13 above.

3.7.2. Scanning Electron Microscopy (SEM) Method

The second characterization tool used in this study was the Hitachi 2-4800 Scanning Electron Microscope (SEM), which provided information on the film morphology, topography and element composition. The benefit of using the SEM for this study is its capability of high depth of focus, high resolution, and high magnification. The SEM is composed of an electron gun where electrons are emitted and accelerated towards the sample. The electrons are focused by electromagnetic coils onto the sample and the electron beam scans the surface. The electrons interact with the surface producing secondary and backscatter electrons, and these electrons are detected by the backscatter detector and it creates an image on the screen surface. The images presented in this study were obtained at a working distance of 15 mm, an electron beam of 20 kV of energy, and 20 μA of current. Some samples were coated with graphite paste on each corner to avoid charging of the sample. For the patterned films several tilted images were obtained either at 40º with a working distance of 16 mm or 60º at a working distance of 27 mm.

Moreover, the EDAX technique was used to prove the elemental composition of the planar CdTe/Si films performed in this study. The EDAX is a technique that where electrons from the beam collide with electrons in the film and the electrons are knocked out of their outer shell. The incident beam excites an electron in inner shell ejecting it from the shell and creating an electron hole where the electron was. Then, an electron with a higher energy level fills the hole, where the difference in energy between the higher and lower shells emits an x-ray [49]. Consequently, each element has its own unique x-ray with its certain amount of energy. As a result of the energy emitted by the x-ray, the characteristics of the element can be identified.

3.7.3. X-ray Diffraction (XRD) Method

The third characterization method used in this study was X-Ray diffraction (XRD), which provides information on the film crystalline quality such as lattice parameter, d-spacing, and preferred orientation by using the rocking curve method. XRD is based on Bragg's law,

$$\lambda = 2dsin(\theta) \tag{3.1}$$

where represents the wavelength of the x-rays, d is the spacing between the planes in the atomic lattice, and θ is the angle between the incident ray and the scattering planes. XRD occurs when the incidence angle and the diffraction angle θ, satisfy Eq. 3.1. The operation of the XRD begins with the rotation of the sample on it axis, where the x-ray source is fixed, and the detector rotates around the sample as shown in Fig. 3.15. The detector collects the diffracted x-rays and when the scan is complete, the x-ray peaks are calculated using Bragg's law. Once the scan is obtained, interface software is used to analyze the data obtained. The XRD results presented in this study were generated with a Cu k-alpha source at a voltage of 45 keV and a current of 30 mA. The step size and the time were different depending on the desire information for each sample.

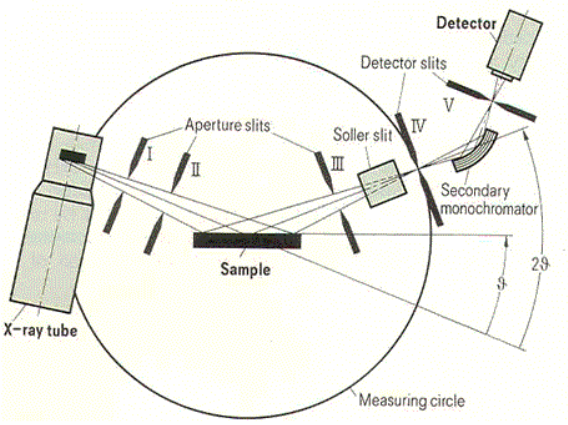


Figure 3.15. Schematic of XRD [46].

Chapter 4: Data and Results

The first set of experiments done in this study consisted on the planar growth of CdTe on CdTe(111) substrates using the CSS technique in order to obtain an optimize deposition recipe and use these parameters for the second set of experiments. The second set of experiments consisted of the planar growth of CdTe on Si(100) substrates using the CSS technique. Lastly, the third set of experiments consisted of the selective growth of a single CdTe grain on patterned Si(100) substrates in order to reduce dislocation densities at the CdTe/Si interface for subsequent growth of HgCdTe for infrared detector applications.

4.1 Planar CdTe Deposition on CdTe(111) and Si(100) via CSS

A set of experiments were performed where CdTe was grown on CdTe(111) and Si(100) substrates using the CSS technique. Moreover, a pre-heat step was performed prior to deposition, as wells as an annealing step after deposition in order to improve the film morphology. The pre-heat and annealing steps were developed by A. Escobedo *et al.* [3], and were used as base parameters for this study. In sections 4.1.1 and 4.1.2, the results of planar CdTe growth on CdTe(111) and Si(100) will be provided and the work performed in this study will be compared with the work performed by Escobedo [3].

4.1.1. Planar CdTe deposition on CdTe(111)

The first set of experiments performed in this study involve the planar deposition of CdTe on CdTe(111) substrates. The intent of these experiments is to attempt to reproduce the work done by Escobedo *et al.* [3] and to compare the planar deposition of CdTe on CdTe(111) and Si(100) substrates to the selective deposition of CdTe on micron and nanoscale pillars on Si(100), all by using the CSS method. Several set of experiments were performed by varying the source and substrate temperature.

Table 4.1 includes a summary of the experiments performed in this study, including the actual substrate temperature (which various from the set temperature), the source temperature, deposition time, and the corresponding variables for the annealing step.

Table 4.1. Experimental parameters for growth of CdTe on CdTe(111) substrates.

	Deposition					Annealing Step				
	Tsou (°C)		Tsub (°C)			Tsou (°C)		Tsub (°C)		
Sample	Set point	Actual	Set point	Actual	Time	Set point	Actual	Set point	Actual	Time
SP400530	530	530	400	404	2 hr.	0	284	400	337	1 hr.
SP350530	530	530	350	411	2 hr.	0	265	350	311	1 hr.
SP350520	520	520	350	403	2 hr.	0	265	350	310	1 hr.
SP350510	510	510	510	396	2 hr.	0	265	350	308	1 hr.

4.1.1.1. Film Thickness

The thickness of each CdTe film was measured using a KLA Tencor Alpha-Step IQ surface profilometer. Table 4.2 includes the source and substrate temperatures, as wells as the deposition time and thickness of each sample. The average growth rate based on these values varied between 5-10 µm/hr. This differs significantly from Escobedo's work, where the CdTe growth rate was approximately 1.5 µm/hr under similar conditions. An attempt was made to reduce the growth rate by decreasing the source temperature, however, this had an adverse effect on the quality of the CdTe film. The thickness for each sample was taken at the center of the CdTe film.

Table 4.2. Profilometer measurements of planar CdTe films on CdTe(111).

Sample	Tsou (°C)	Tsub (°C)	Actual Tsub (°C)	Dep. Time	Thickness
SP400530	530	400	404	2 hr.	20 µm
SP350530	530	350	411	2 hr.	10 µm
SP350520	520	350	403	2 hr.	8 µm
SP350510	510	350	396	2 hr.	2 µm

4.1.1.2. Film Morphology

A SEM image for the best CdTe film obtained in this study is shown in Fig. 4.1 for sample SP350530.

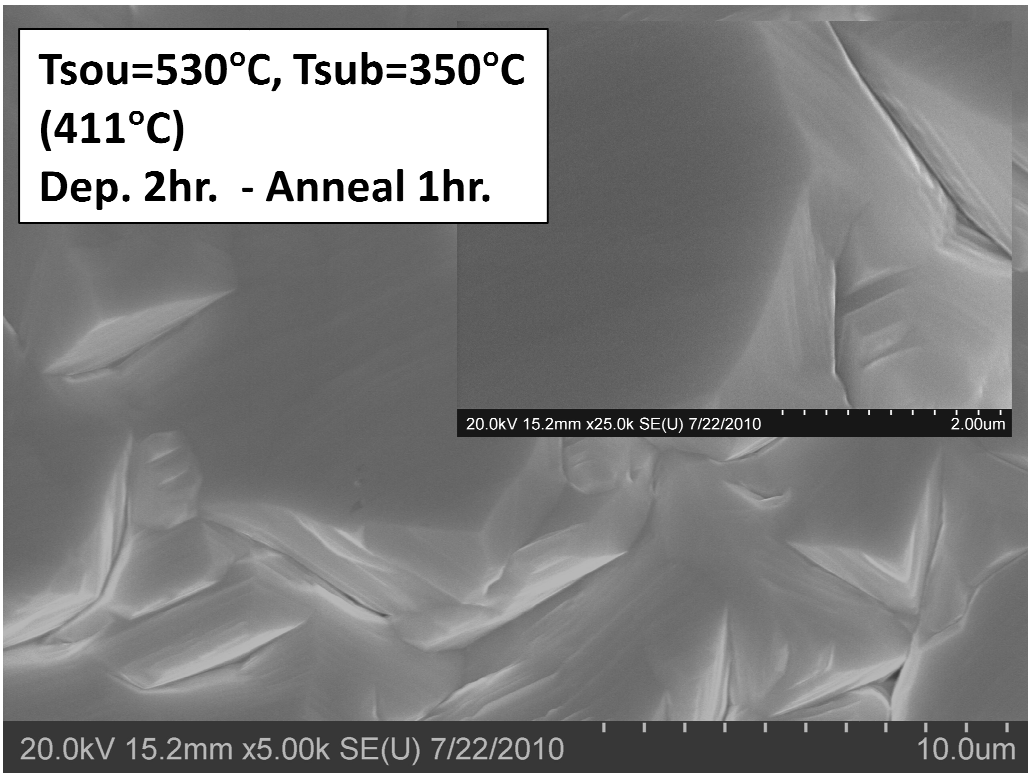


Figure 4.1. SEM comparison of planar CdTe on CdTe(111) from this study.

The planar CdTe growth on CdTe(111) substrates in Fig 4.1 corresponds to source and substrate temperatures of 530ºC and 411ºC, and He pressure of 5 Torr.

4.1.2. Planar CdTe deposition on Si(100)

The goal for the planar CdTe growth on Si(100) substrates was to obtain an optimized recipe to deposit high quality CdTe growth on Si(100) substrates via CSS, as well as reporting the effect of the grain size as a function of the source and substrate temperatures. Table 4.3 includes the actual

temperatures of the deposition and annealing steps for each of the samples. These films are compared to the CdTe/CdTe(111) films and the patterned growth on Si(100) substrates.

Table 4.3. Experimental parameters for planar CdTe growth on Si(100) substrates.

	Deposition					Annealing Step				
	Tsou (ºC)		Tsub (ºC)			Tsou (ºC)		Tsub (ºC)		
Sample	Set point	Actual	Set point	Actual	Time	Set point	Actual	Set point	Actual	Time
S350530	530	530	350	428	1 hr.	0	300	395	335	30 min.
S2350530	530	530	350	432	2 hr.	0	300	395	340	1 hr.
S300530	530	530	300	417	2 hr.	0	290	395	330	1 hr.
S325530	530	530	325	418	2 hr.	0	290	395	333	1 hr.
S350520	520	520	350	411	1 hr.	0	298	395	334	30 min.
S450550	550	550	450	450	2 hr.	0	295	395	338	1 hr.

4.1.2.1. Film Thickness

The thickness of each CdTe film was measured using a KLA Tencor Alpha-Step IQ surface profilometer. Table 4.4 includes the source and substrate temperatures, as well as the deposition time and thickness of each sample. The thickness measurement for each sample was taken at the center of each CdTe film as described in the experimental section 3.7.1.

Table 4.4. Profilometer measurements of planar CdTe films on Si(100).

Sample	Tsou (ºC)	Tsub (ºC)	Actual Tsub (ºC)	Deposition Time	Thickness
S350530	530	350	428	1 hr.	8 µm
S2350530	530	350	432	2 hr.	12 µm*
S325530	530	325	418	2 hr.	15 µm
S300540	530	300	417	2 hr.	20 µm
S350520	520	350	411	1 hr.	2.5 µm*
S450550	550	450	450	2 hr.	30 µm

**Rough film*

The CdTe growth rates for CdTe on Si(100) are comparable to those for CdTe growth on CdTe(111). Regardless of the substrate temperature, the growth rate varied between 6 and 10 μm/hr. When the source temperature was increased to 550ºC, the growth rate increased to 15 μm/hr.

4.1.2.2. Film Morphology and Element Composition

In this study several experiments were performed by varying the substrate temperature for a constant source temperature of 530ºC. Two additional experiments were performed, one with a source temperature at 520ºC in order to lower the growth rate and a second at a high source and substrate temperature, 550ºC and 450ºC, respectively. The latter experiment was performed in order to compare the planar CdTe growth to the patterned CdTe growth for the same source and substrate temperatures. The He pressure was set to 5 Torr for all the growth experiments, and the purge and the pre-heat steps were the same as those for the first set of experiments as outlined in Table 4.3. The actual source and substrate growth and annealing temperatures are included in Table 4.4. Note that in all cases, the annealing time is half the deposition time. Figure 4.2 includes SEM micrographs at low and high magnification for samples S350530, S2350530, and S450550. Similar to the first experiment where CdTe was grown on CdTe(111) substrate and to the work done by Escobedo, the best films were observed for a set source temperature of 530ºC and substrate temperature of 350ºC (Fig. 4.2 (b)). The actual substrate temperature varies from the set temperature due to the close proximity of the source and substrate and the set temperature is reported in order to keep track of each experiment. The actual substrate temperatures are included in Fig. 4.2 in parentheses.

Although there is a 19% lattice mismatch between Si and CdTe, Fig. 4.2 shows promising results for the planar deposition using the CSS technique. XRD results are included in section 4.1.3 where this work is compared to the CdTe/CdTe(111) films resulting from this study to those in Escobedo's work.

In addition, the CdTe/Si(100) film shown in Fig. 4.1(b) contains twins similar to those reported by Escobedo *et al.* [3] Zuniga *et al.* [51], Seto *et al* [52], and Jiang *et al.* [53] on Si, sapphire, GaAs, and Ga substrates.

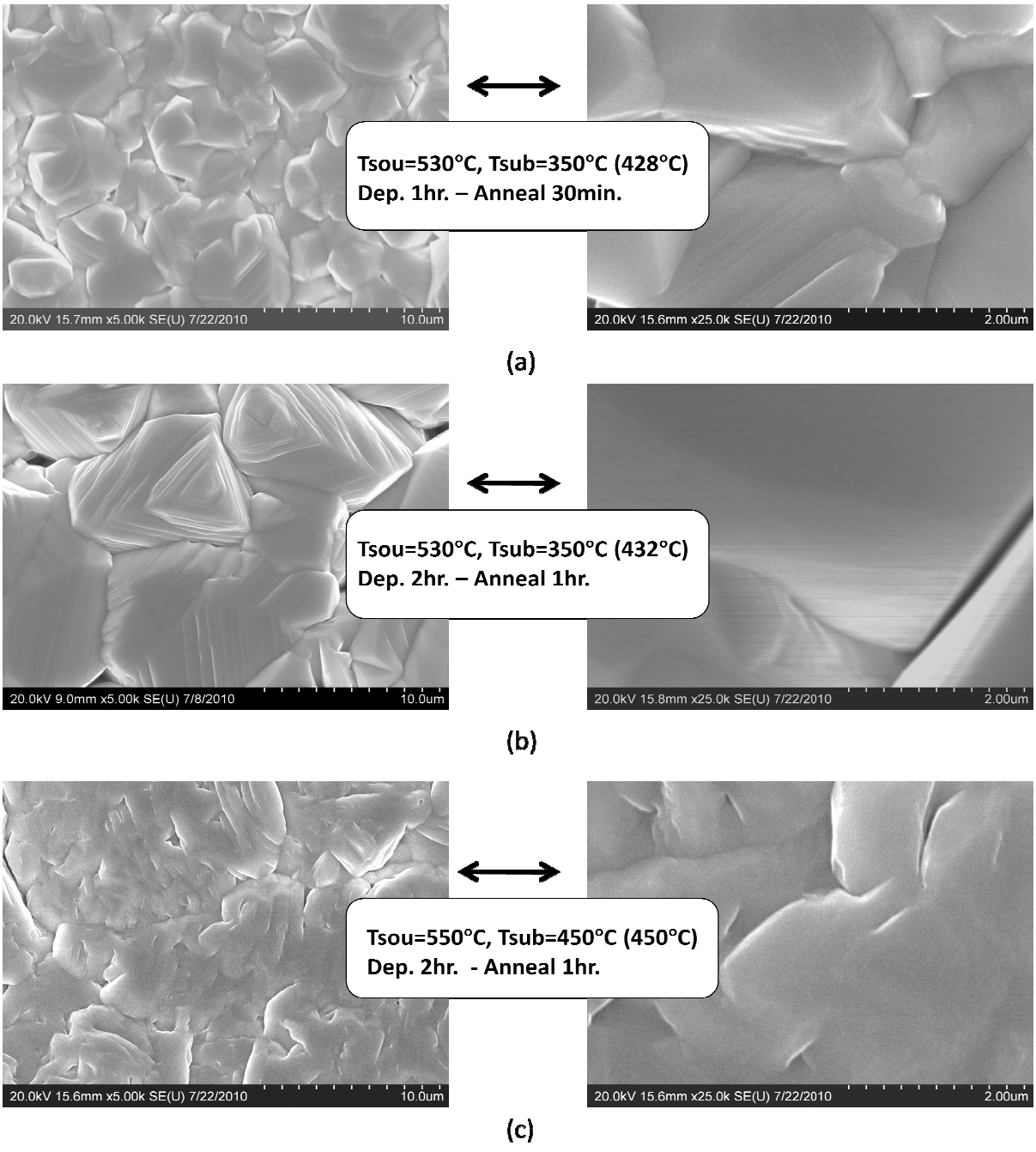
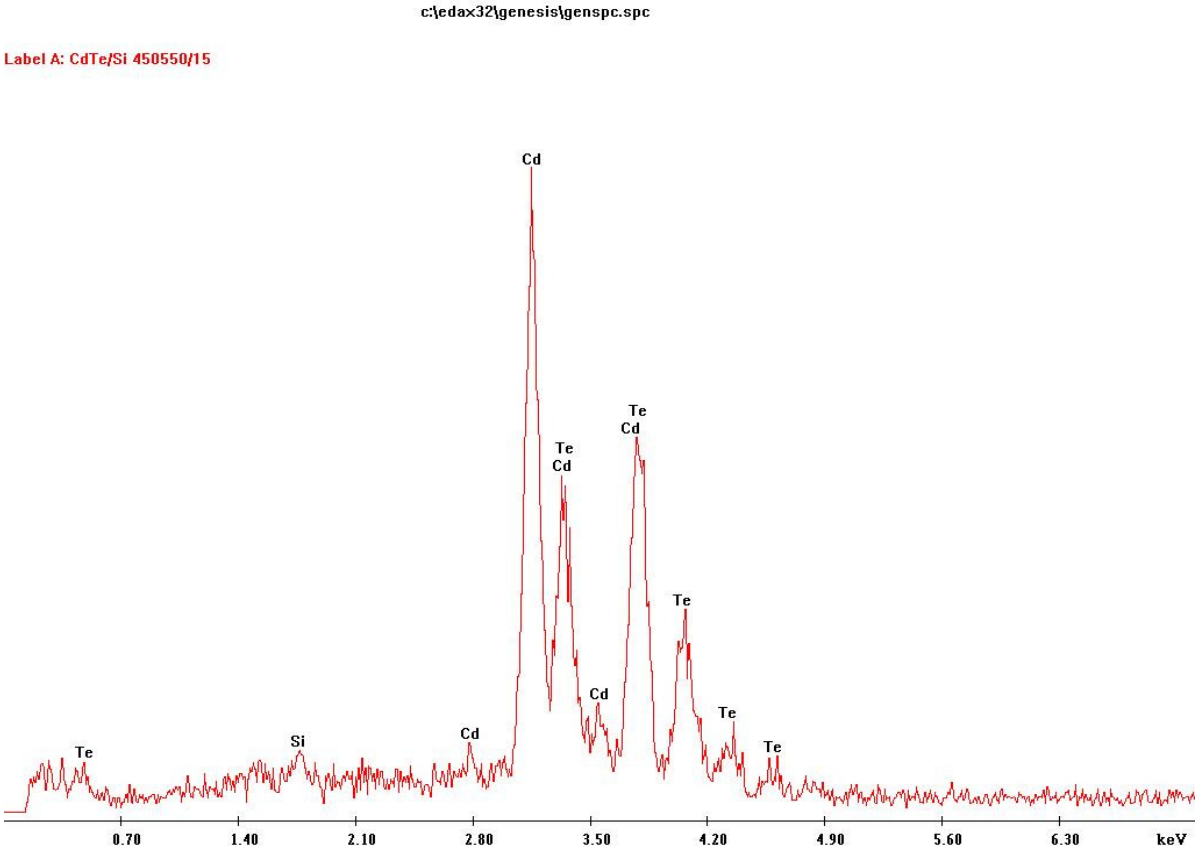


Figure 4.2. Surface view SEM image of CdTe/Si (100) for (a) sample S350530 where Tsou=530ºC and Tsub=350ºC for 1 hr. deposition and 3 0min. anneal, (b) sample S2350530 where Tsub=530ºC and =350ºC for 2 hr. deposition and 1 hr. anneal, (c) sample S450550 where Tsou=550ºC and Tsub=450ºC for 2 hr. deposition and 1 hr. anneal.

The elemental composition of sample S450550 is shown in Fig. 4.3. As it was mentioned before, each element has its own unique x-ray with its own amount of energy. The EDAX spectrum and corresponding data show that the CdTe film is composed of approximately 50% Cd and 50% Te atoms.



Elem	Wt %	At %	K-Ratio	Z	A	F
SiK	1.47	6.00	0.0089	1.2702	0.4727	1.0069
CdL	46.27	47.12	0.4650	1.0207	0.9649	1.0206
TeL	52.26	46.88	0.4243	0.9713	0.8359	1.0000
Total	100.00	100.00				

Element	Net Inte.	Backgrd Inte. Error	P/B
SiK	11.62	5.85	11.16	1.99
CdL	176.53	7.15	2.10	24.70
TeL	132.56	7.51	2.46	17.65

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Figure 4.3. EDAX spectrum showing elemental composition of the CdTe film on Si(100) for T_{sou}=550°C and T_{sub}=450°C.

4.1.3. Comparison of planar CdTe/CdTe(111) to planar CdTe/ Si(100)

Figure 4.4 illustrates three high magnification SEM images of planar CdTe growth on Si(100) and CdTe(111) substrates, where the CdTe growth was performed for 2 hours at =530ºC and =350ºC, and annealed for 1 hour at approximately 395ºC for the three samples. Figures 4.4 (a) and (b) include CdTe films on CdTe(111) and Si(100) substrates, respectively, resulting from this study. The corresponding XRD rocking curves are included in the next section.

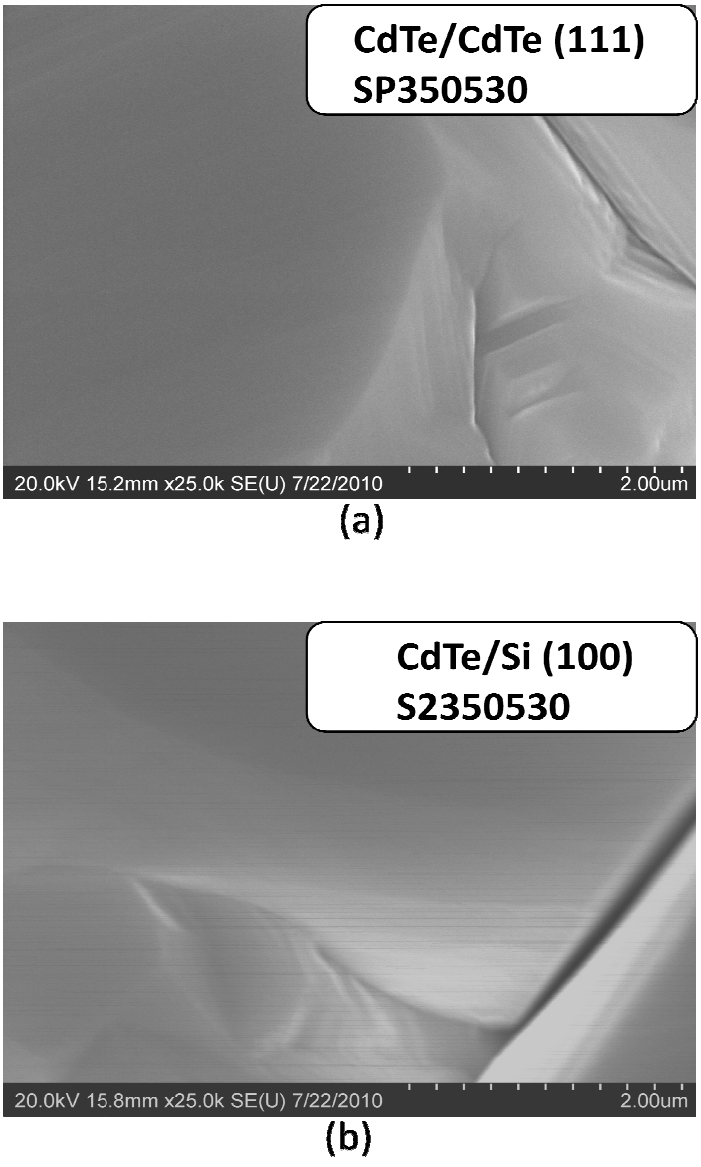

Figure 4.4. Surface SEM images of CdTe epitaxial growth on (a) CdTe(111) at 5 Torr, (b) Si(100) at 5 Torr.

4.1.4. XRD comparison of planar CdTe films on CdTe(111) and Si(100) substrates

The XRD results coincide with the SEM images shown in Fig 4.4. Figure 4.5(a) shows a peak at approximately 39.3º with a FWHM value of 180 arcsec for CdTe on CdTe(111). For Fig. 4.5(b), the peak at approximately 39.3º with a FWHM value of 216 arcsec for CdTe on Si(100). It was expected that the FWHM value for CdTe on Si(100) would be higher than CdTe on CdTe(111). Both FWHM values are higher compared to the value obtained by Escobedo [3] of 136 arcsec for CdTe on CdTe(111) (Fig. 4.5(c)).

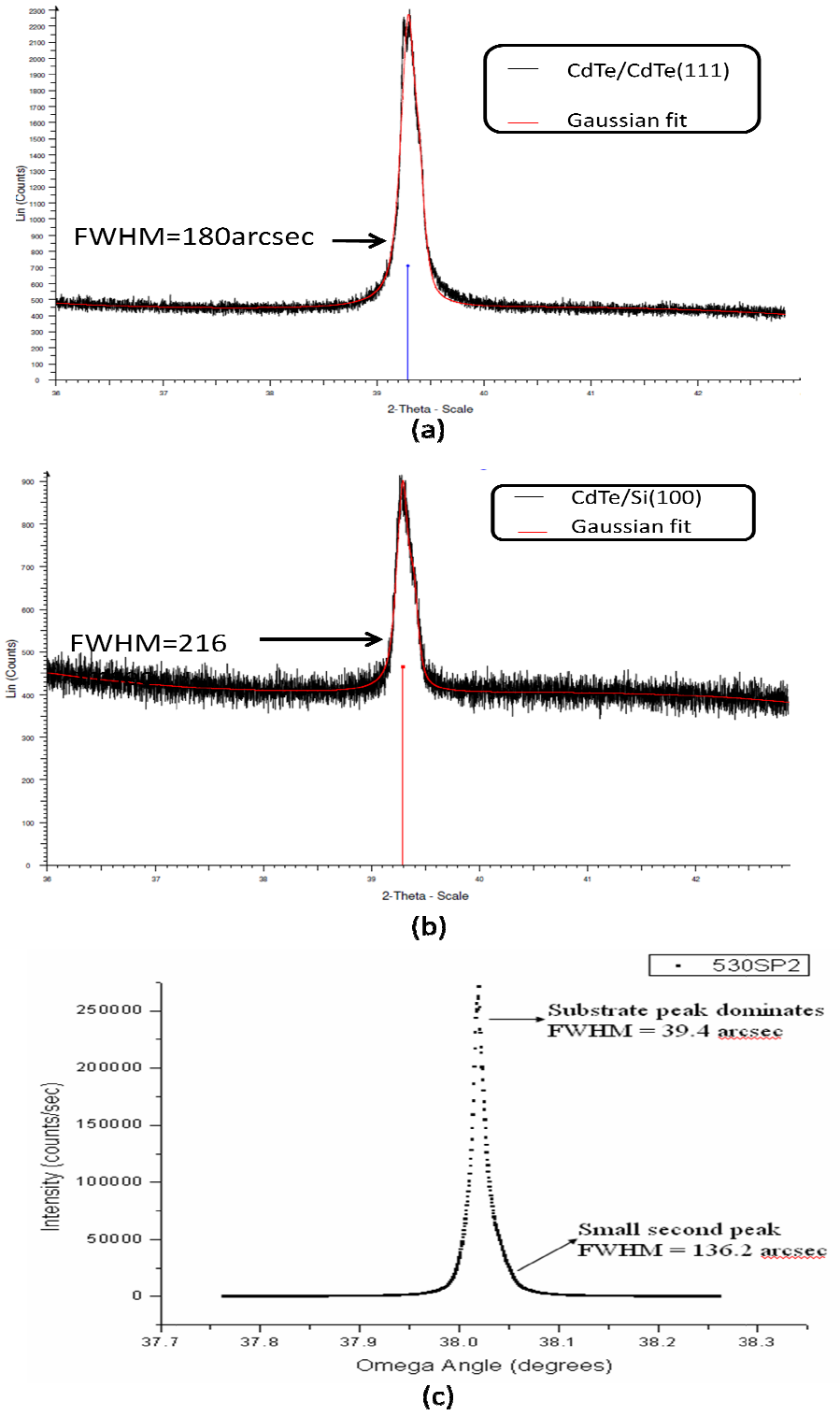

Figure 4.5. XRD rocking curve scan with calculated FWHM value for (a) sample SP350530, 10 µm CdTe film deposited on CdTe(111) at Tsou=530ºC and Tsub=350ºC for 2 hr. dep. and 1 hr. anneal, (b) sample S350530, 12 µm CdTe film deposited on Si(100) at Tsou=530ºC and Tsub=350ºC for 2 hr. dep. and 1 hr, and (c) sample 530SP3, 3 µm CdTe film deposited on CdTe(111) Tsou=530ºC and Tsub=350ºC for 2 hr. dep. and 1 hr [3].

4.2 SELECTIVE CDTE DEPOSITION ON PILLARS FOR SI(100) SUBSTRATES.

The ultimate goal of this study is the selective nano-heteroepitaxial growth of CdTe on Si(100) substrates. The Si(100) substrates were patterned by the photolithography method at the micron and nanoscale then dry etched to create pillars on the Si surface, followed by the selective growth of CdTe on the pillar surfaces using the CSS technique. Si substrates are being used in this study because they are available in large areas at a low cost, and can be used for the fabrication of silicon based integrated circuits for applications of HgCdTe infrared detectors [10]. According to prior work, it is known that dislocations at the CdTe/Si interface can be reduced for selective growth at the nanoscale as a result of dislocation densities migrating to the side walls [21]. Once high quality selective CdTe/Si(100) growth is achieved, further work will be done using Si(211) substrates. CdTe growth on CdTe(211) surfaces results in less twinning and lower dislocation densities. It is believed that high quality CdTe planar growth can be obtained by growing CdTe on high quality patterned surfaces using MBE.

4.2.1 Photolithography Method

Several experiments were performed in order to achieve a high quality pattern on Si(100) substrates. The experiments included both positive (S1813) and negative (AZ5214) photoresist (explained in detail in section 3.1.2). Table 4.5 includes a summary of the lithography parameters used that were successful in creating a pattern on the Si(100) substrates using positive and negative photoresist.

Table 4.5. Summary of successful parameters used to pattern Si(100) using positive and negative photoresist.

Sample	Photoresist	Exposure Time (sec.)	Flood Exposure (sec.)	Developer Time (sec.)
8-PPR	Positive	17	-----	95
10-NPR	Negative	13	99	40

Figure 4.5 illustrates two different patterns acquired from the photolithography process using positive (Fig. 4.5(a)) and negative (Fig. 4.5(b)) photoresist. In the positive photoresist process, the pattern consists of windows with a diameter of 2 µm, where the photoresist was exposed to the UV light through the windows in the mask. The photoresist was removed in these areas to create holes. The substrate was exposed to UV light for 17 seconds, followed by immersion in the developer for 95 seconds (Fig. 4.6(a)). For the negative photoresist, the photoresist was exposed to the UV light through the windows in the mask for 13 seconds, followed by a flood exposure for 99 seconds in order to reverse the positive photoresist into a negative image of the pattern. Then, the pattern was immersed in the developer solution for 40 seconds, resulting in a pattern where posts with 2 µm in diameter were obtained (Fig. 4.6 (b)).

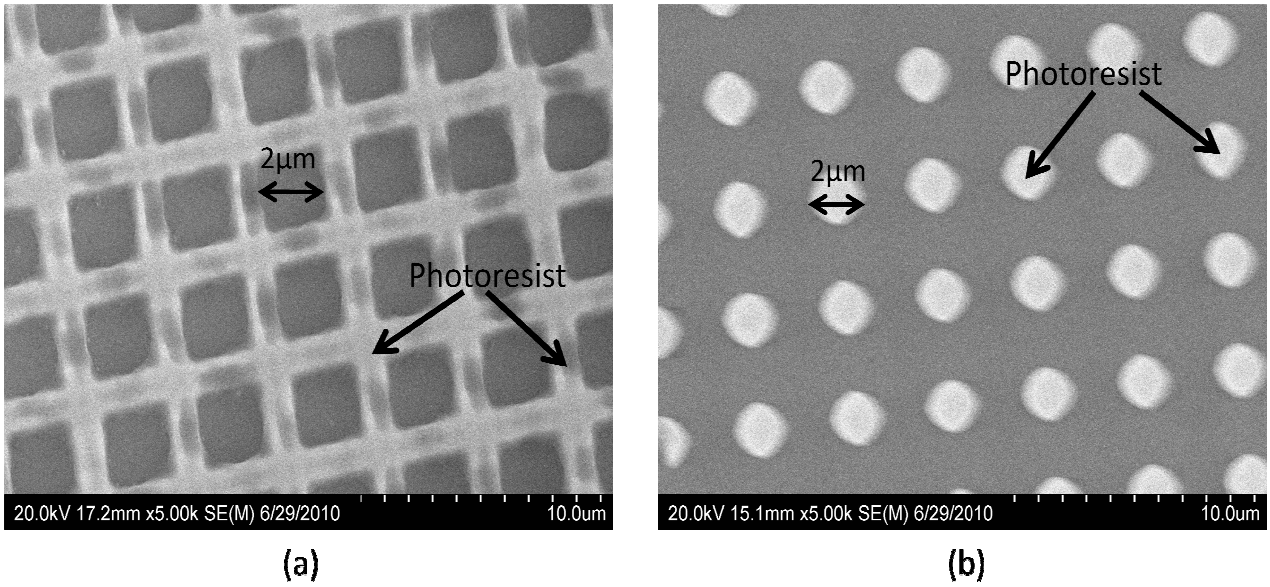

Figure 4.6. SEM pictures of (a) pattern on Si(100) substrate using positive (S1813) photoresist and (b) pattern on Si(100) substrate using negative (AZ5214) photoresist. The photomask consist of windows with 2 µm in diameter.

Once the pattern of the photoresist is achieved, the substrate is etched in order to create holes or pillars on the Si surface. The thickness of the photoresist applied to the substrate needs to be known in order to remove all photoresist from the substrate surface during the dry etching process. The

profilometer was used to measure the thickness of the photoresist. Figure 4.7 includes a graph showing the thickness of the photoresist, where the thickness was approximately ~56 nm (0.056 µm).

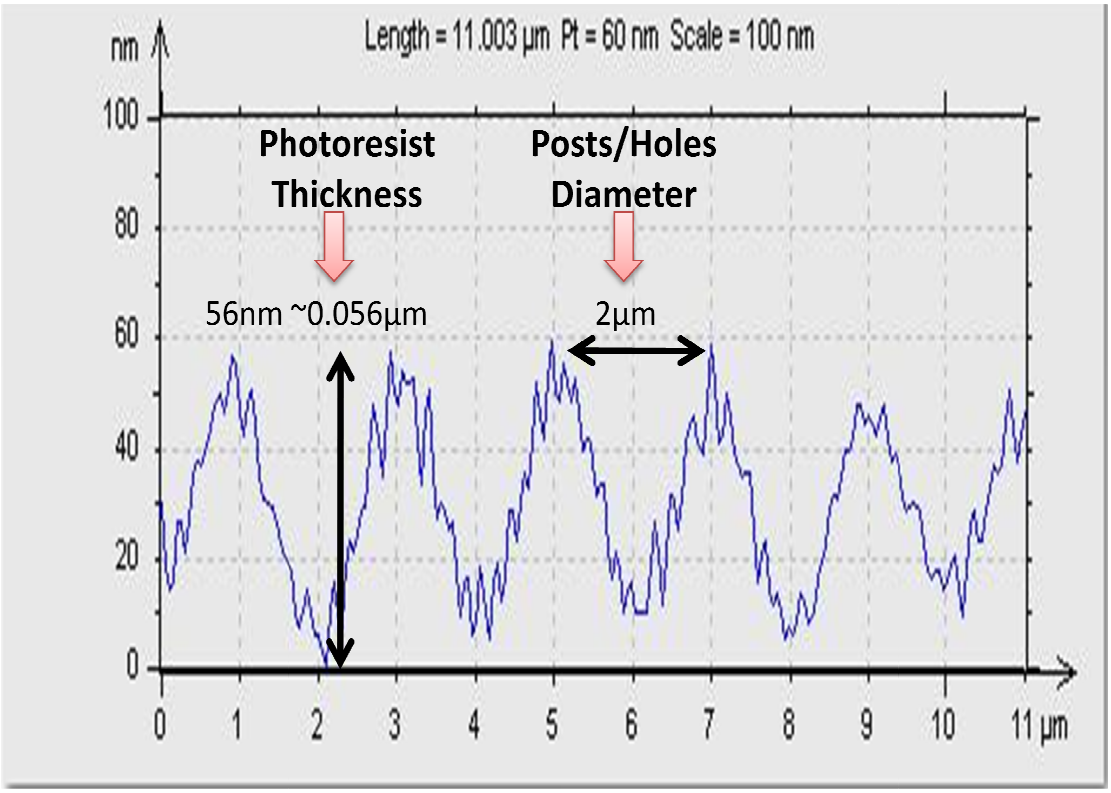

Figure 4.7. Profilometer scan to demonstrate the thickness of photoresist.

4.2.2. Dry Etching Parameters

Once a high quality pattern is obtained on the substrate, the next step is to etch the patterned substrate in order to create pillars. Since the purpose of this study was the selective CdTe nano-heteroepitaxial growth, the substrate needed to be etch enough to reduce the size of the pillars from 1 µm down to the nanoscale. Several sets of experiments were performed in order to obtain the optimize parameters to create pillars on the substrate (which are explained with detail in Section 3.2). In addition, Table 4.6 shows a summary of the parameters used to obtain high quality pillars from the dry etching method using positive and negative photoresist. In the case of the positive photoresist, the pattern was etched with an anisotropic etch in order to increase the size of the windows. Once the windows

intersect, posts are created and the remaining photoresist is removed. In the case of the negative photoresist, the same anisotropic etch was used in order to decrease the size of the pillars.

Table 4.6. Summary of successful parameters used to form pillars from negative and positive photoresist.

Sample	Result-Post size	Photoresist	Gas Flow (sccm)	RF Power (watts)	Gas Pressure (Torr)	Etch Time (min.)
6-PPR	1.5 µm	Positive	30	130	0.05	3.45
4-PPR	1 µm	Positive	30	120	0.06	5
5-PPR	600 nm	Positive	30	170	0.07	9
2-NPR	1.5 µm	Negative	30	160	0.05	4
3-NPR	1 µm	Negative	30	170	0.07	3.45
6-NPR	500 nm	Negative	30	170	0.09	3
5-NPR	450 nm	Negative	30	180	0.1	3.45

Five different sizes of pillars were obtained from the positive and negative photoresist (Table 4.6). A longer etch time was used in order to decrease the pattern size. Figure 4.9 includes tilt and surface SEM images for three different sizes of pillars achieved with positive and negative photoresist. The patterns shown in Figs.4.8(a) through (d) were obtained using positive photoresist and the patterns in Figs. 4.8(e) and (f) were obtained using negative photoresist. In order to deposit high quality CdTe grains selectively on top of the pillars, the top surface of the pillars needs to be flat and smooth. For this reason, several experiments were performed in order to obtain the etching rate for Si, where the etching rate is approximately 200 nm/min. The etching rate helped to obtain the correct time for the etching process in order to avoid over etching the pattern and for well define pillars. Figure 4.8(a) and (b) show tilt and surface view SEM images, respectively, resulting in 1 µm pillars using positive photoresist (Sample S4PPR). Figure 4.8(c) and (d) show tilt and surface view SEM images, respectively, resulting in 600 nm pillars using positive photoresist (Sample S14PPR). Figures 4.8(e) and (f) show tilt and surface view SEM images, respectively, resulting in 450 nm pillars (Sample S5NPR). It is evident from Fig. 4.8 that the high quality pillars were achieved using negative photoresist, because the surface is altered with high etching times (Fir. 4.8(b)), which are needed for reducing the size of the pillars.

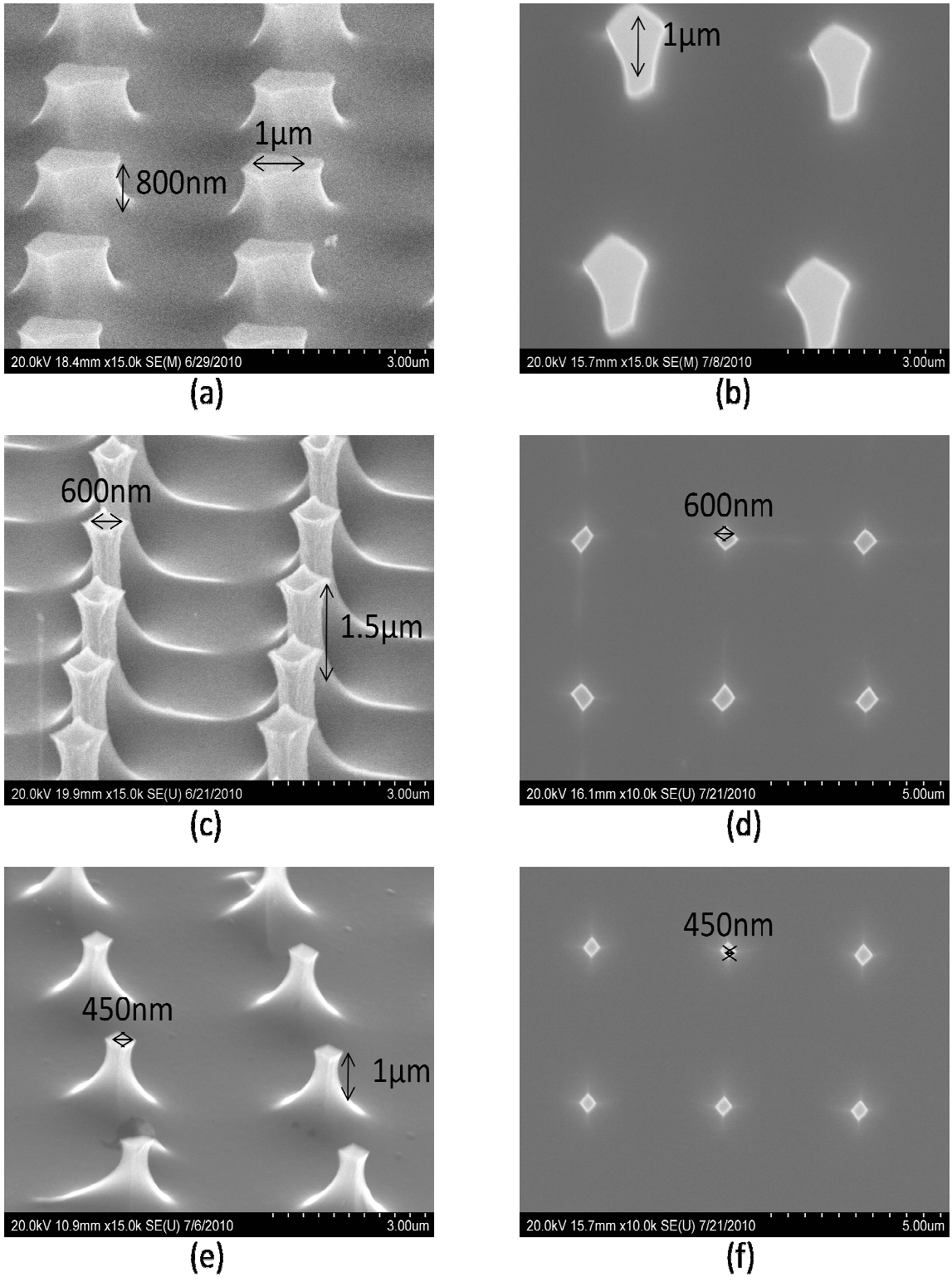

Figure 4.8. (a) Tilt and normal SEM views of (a) and (b) pillar 1 µm in diameter and 800 nm height, (c) and (d) pillar 600 nm in diameter and 1.5 µm height, (e) and (f) pillar 450 nm in diameter and 1 µm height.

4.2.3. Selective CdTe Deposition on Si(100) via CSS

The selective growth of CdTe on Si(100) substrates was performed using the CSS technique on the patterned samples described in Section 4.2.1. The pillars on the Si(100) substrates varied between 450 nm-1.5 µm, and CdTe deposition was limited to patterned substrates with 1µm pillars and substrates with pillars ranging between 450-500 nm. The experiments were designed in order to result in a single CdTe grain on top of each pillar, with maximum pattern uniformity on the substrate surface. Figure 4.9 includes a schematic of the designed selective growth.

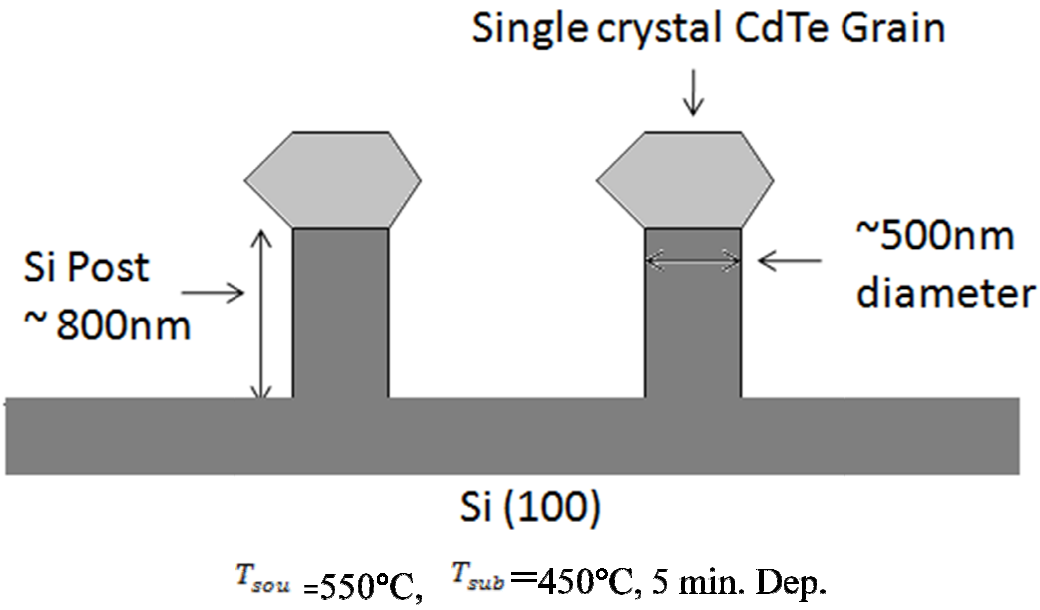

Figure 4.9. Schematic of selective CdTe growth on Si(100) substrate via CSS.

The parameters that defined the selective CdTe growth were the substrate and source temperature, as well as the deposition time. The pressure of the system was kept at 5 Torr throughout the warm-up and deposition steps. The initial deposition parameters used were based on the work performed by Escobedo, where he selectively deposited CdTe on a patterned CdTe/Si(211) substrate using a mask which exposed CdTe windows (See Fig. 4.21, in section 4.2.4). The parameters developed by Escobedo were Tsub=450ºC and Tsou=530ºC with a deposition time of 15 minutes.

These parameters were modified in this study in order to selectively deposit CdTe on patterned Si(100) substrates without a mask layer.

In the study by Escobedo, the window for selective deposition was narrow. Selective CdTe deposition on CdTe(211) windows was achieved only for a source temperature of 530ºC and a substrate temperature of 450ºC. For other source and substrate temperatures studied, inverse selectivity or no selectivity occurred [3]. In this study, selective CdTe deposition occurred for almost all substrate and source temperature values selected.

In order to analyze the morphology of the selective CdTe films, the SEM was used to confirm a high quality film. The SEM characterization provides information on how the deposition parameters, as well as the pattern structure affect selective growth and the growth of a high quality single CdTe grain on the Si(100) pillars. Other factors include a reactor warm-up deposition step and annealing of the CdTe source prior to deposition.

4.2.3.1. Selective CdTe growth on Si(100) without reactor warm-up steps and source anneal (Set I)

The first set of pattern experiments were performed with Si(100) substrates that were patterned with positive and negative photoresist in order to analyze the quality of the CdTe growth for each type of photoresist. Reactor warm-up steps were not included in the deposition process for this set of samples. For the next set of experiments the warm-up step was included and the source was annealed prior to each deposition. Table 4.7 includes the source and substrate temperatures, the deposition time, the type of photoresist, the pattern size and the quality of the CdTe deposition for each sample.

Table 4.7. Summary of experiments performed using positive and negative photoresist without warm-up steps and source anneal (Set I).

Sample	Pattern Size	Photoresist	Tsub (°C)	Tsou (°C)	Dep. Time	Uniformity	Quality
S2PPR	1.5 µm	Positive	450	530	15 min.	Yes	Multigranular
S2NPR	1 µm	Negative	450	530	15 min.	Yes	Multigranular

SEM images of the patterned substrate prior to the CdTe deposition and after the deposition process are included here for each of the samples listed in Table 4.7. For sample S2PPR, the Si substrate was patterned using positive (S1813) photoresist and was dry etched for 3 minutes with ionized gas, resulting in pillars at the micron scale (1.5 µm diameter, 1 µm pitch), and CdTe was deposited for 15 minutes in the CSS. Figure 4.10 includes a low and high magnification surface view SEM image of sample S2PPR, before and after deposition, illustrating selective CdTe growth on the patterned Si(100) substrate. The average size of the CdTe grains was 3.26 µm in diameter. The CdTe grains were multifaceted and multiple grains deposited on top of each pillar.

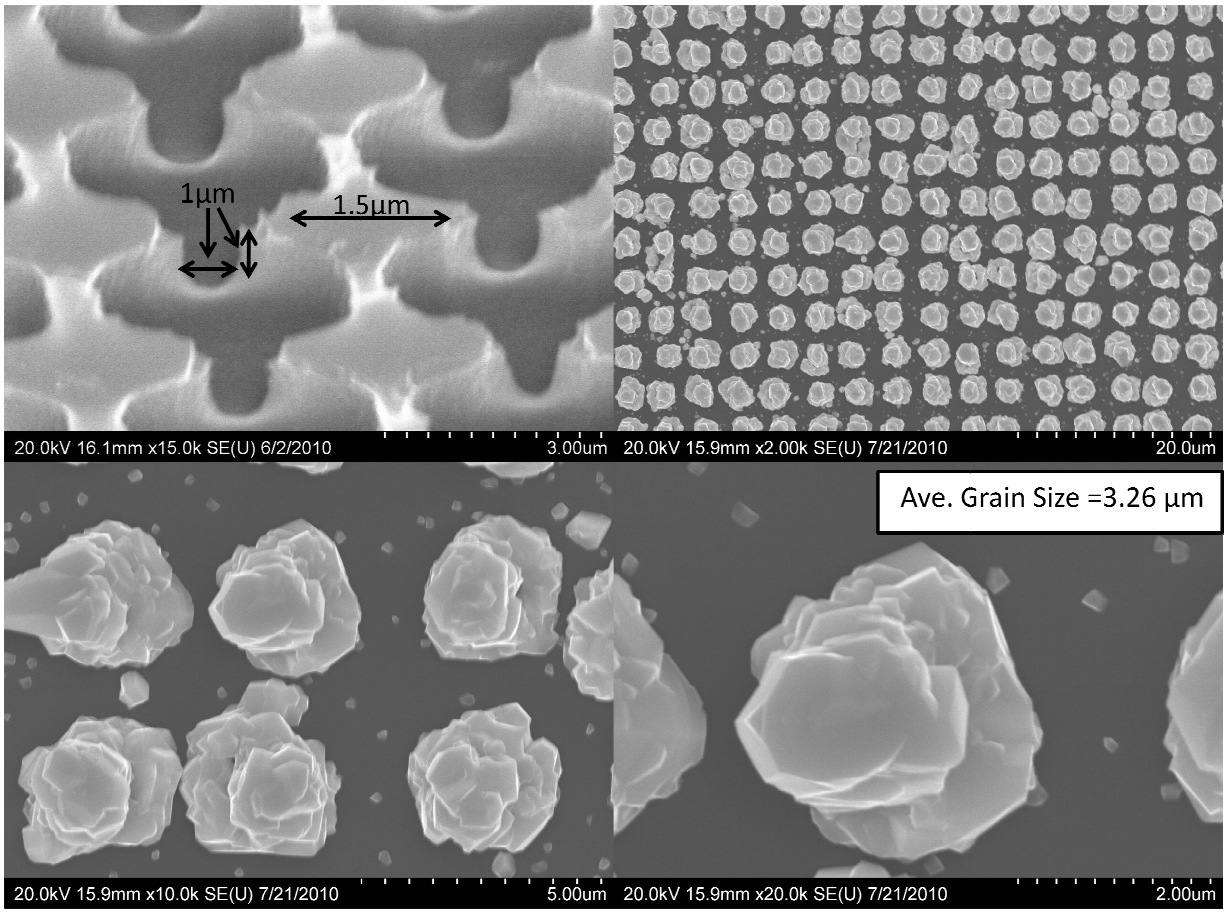

Figure 4.10. Surface SEM images of sample S2PPR, where the CdTe deposition process was performed for 15 minutes at Tsou=530ºC and Tsub=450ºC.

For sample S2NPR the substrate was patterned using negative (AZ5214) photoresist and was dry etched for 5 minutes with ionized gas, resulting in pillars at the micron-scale (1 µm diameter, 3 µm

pitch). The same deposition parameters were used for this sample (Table 4.8). Figure 4.11 includes a low and high magnification surface SEM image of sample S2PPR before and after deposition, illustrating selective CdTe growth on the patterned Si(100) substrate. The CdTe deposition is of better quality compared to the previous sample (S2PPR). In this case the average size of the CdTe grains was 4.35 µm in diameter.

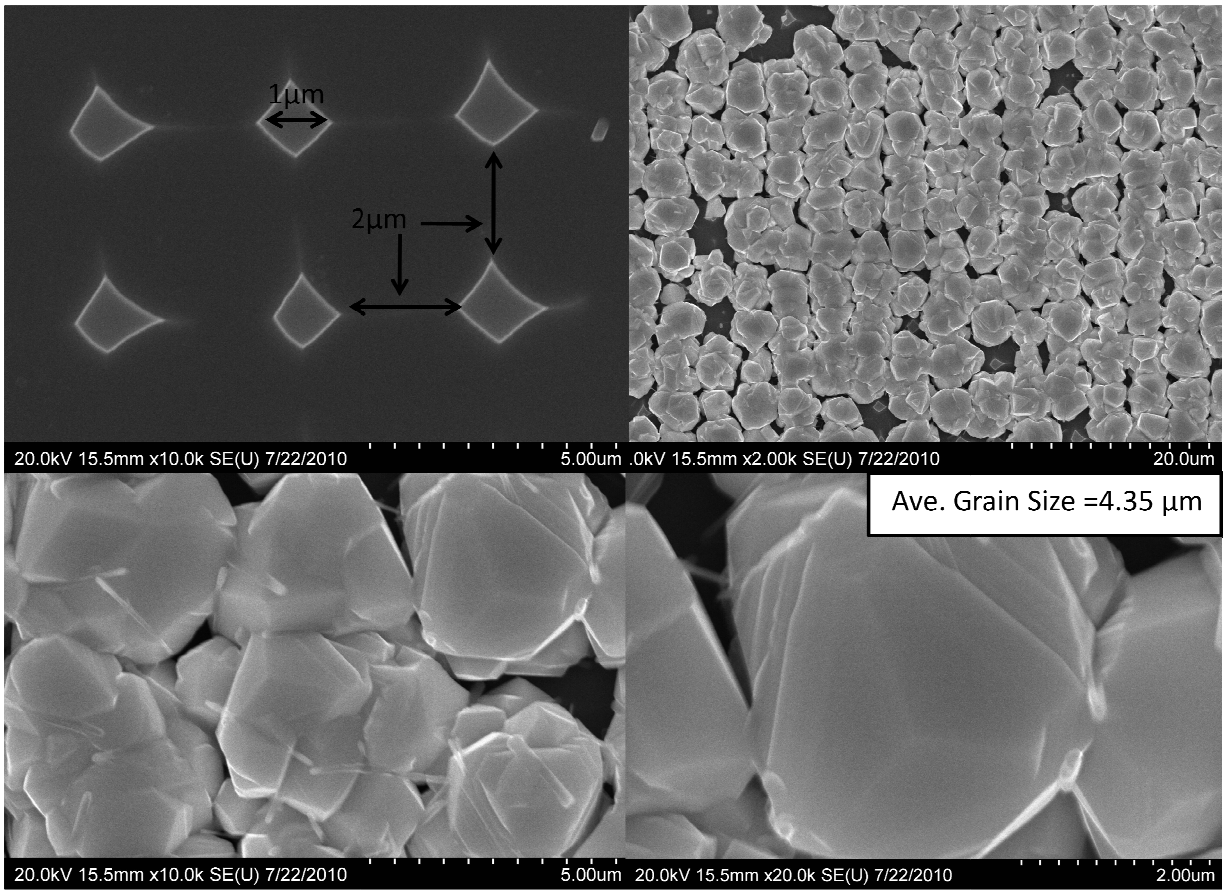

Figure 4.11. Surface SEM images of sample S2NPR, where the CdTe deposition process was performed for 15 minutes at Tsou=530ºC and Tsub=450ºC.

A comparison of Figs. 4.10 and 4.11 indicates that CdTe deposition on the sample prepared using negative photoresist resulted in more grains that grew in a uniform manner with smooth surfaces on the top surface of the grains (See high magnification view in Fig. 4.11).

4.2.3.2. Selective CdTe growth on Si(100) with 1µm pattern for 5 min. deposition (Set II)

For the next set of patterned experiments, it was decided to add reactor warm-up and deposition ramp steps, and the source was annealed prior to each deposition. Table 4.8 includes a summary of the experiments performed on Si(100) substrates with a 1µm pattern. Each deposition was carried out for 5 minutes for a substrate temperature of 450ºC and various source temperatures. The source temperature was increased from 540ºC to 560ºC in order to determine the effect on the grain size and morphology. The deposition time was decreased to 5 minutes in order to decrease the size of the CdTe grains. Table 3.8 in section 3.6.1 includes details pertaining to the deposition recipe for the rest of the samples performed in this study. As it was mentioned before, the source was annealed for 30 minutes at 600ºC in order to remove a thin oxide layer and produce a repeatable growth rates for all set of experiments. Since sample S2NPR (section 4.2.3.1) resulted in higher quality CdTe growth compared to sample S2PPR, it was decided to complete the rest of the experiments in this study with Si(100) substrates that were patterned only with negative photoresist.

Table 4.8. Summary of experiments performed on Si(100) substrates with 1µm pattern for 5 min. deposition (Set II).

Sample	Pattern Size	Photoresist	Tsub (°C)	Tsou (°C)	Dep. Time	Uniformity	Quality
S4NPR	1 µm	Negative	450	540	5 min.	No	Mutligranular
S3NPR	1 µm	Negative	450	550	5 min.	Yes	High quality
S10NPR	1 µm	Negative	450	560	5 min.	No	Multigranular

SEM images for the samples listed in Table 4.8 are shown in Figs. 4.12 through 4.14. These images include a surface view of the substrate before and after CdTe deposition. Multiple micrographs are provided for the CdTe growth at low and high magnification. As mentioned beforehand, only negative photoresist was used for the reminder of the study. Sample S4NPR was patterned with negative photoresist and was dry etched for 3.45 minutes with SF_6 ionized gas, resulting in pillars at the micron-scale (1 µm diameter, 2 µm pitch). The CdTe deposition was performed for 5 minutes at T_{sou}=540ºC and T_{sub}=450ºC, where the average grain size was 2.22 µm in diameter (Fig. 4.12). Sample

S3NPR was patterned with negative photoresist and was dry etched for 3.45 minutes with ionized gas, resulting in pillars at the micron-scale (1 µm diameter, 2.5 µm pitch). The CdTe deposition was performed for 5 minutes at Tsou=550ºC and Tsub==450ºC, where the average grain size was 4.17 µm in diameter (Fig. 4.13). Sample S10NPR was patterned with negative photoresist and was dry etched for 3.45 minutes with ionized gas, resulting in pillars at the micron-scale (1 µm diameter, 2 µm pitch). The CdTe deposition was performed for 5 minutes at Tsou=560ºC and Tsub==450ºC, where the average grain size was 4.70 µm in diameter (Fig. 4.14).

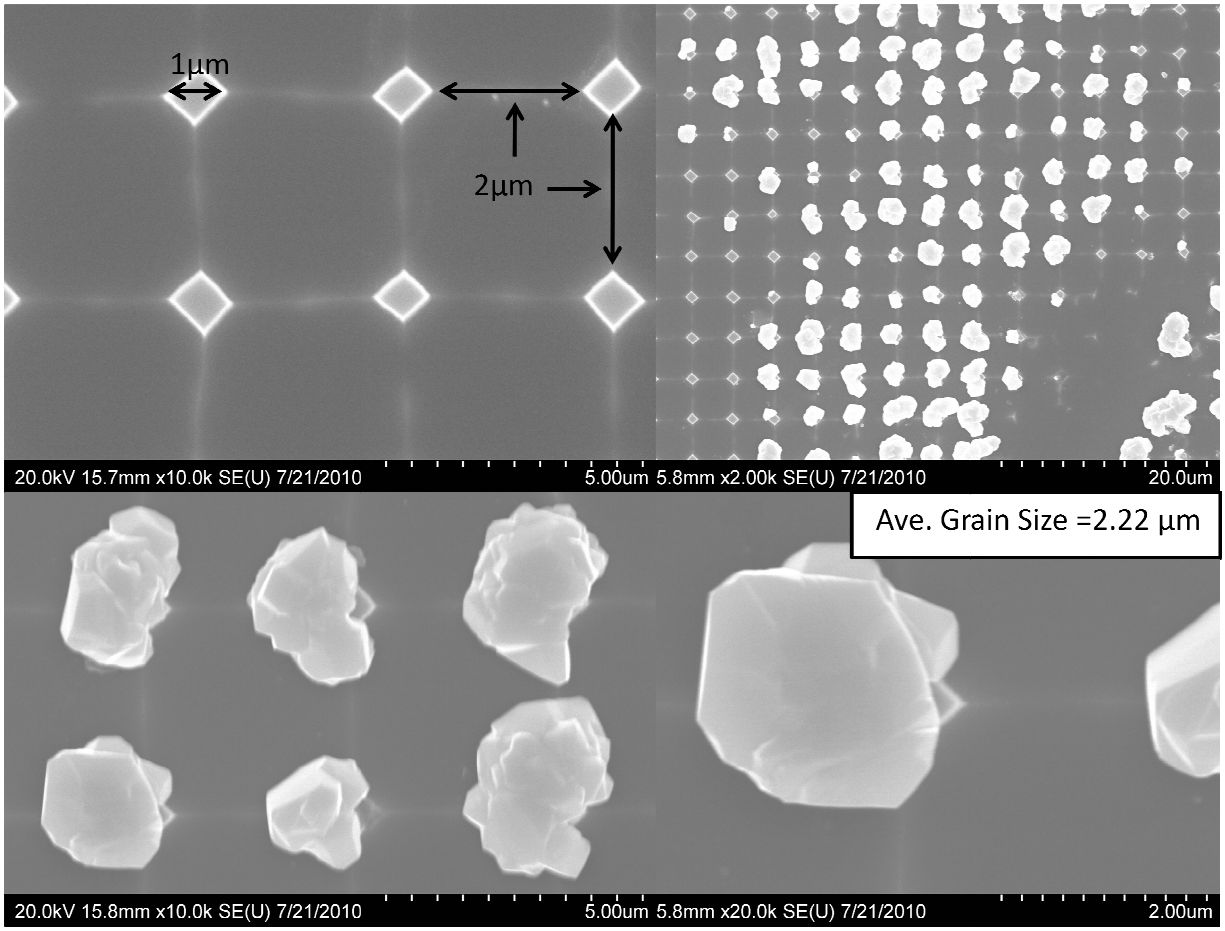

Figure 4.12. Surface SEM image of sample S4NPR, where the CdTe deposition process was performed for 5 minutes at Tsou=540ºC and Tsub=450ºC including the warm-up and deposition ramp steps.

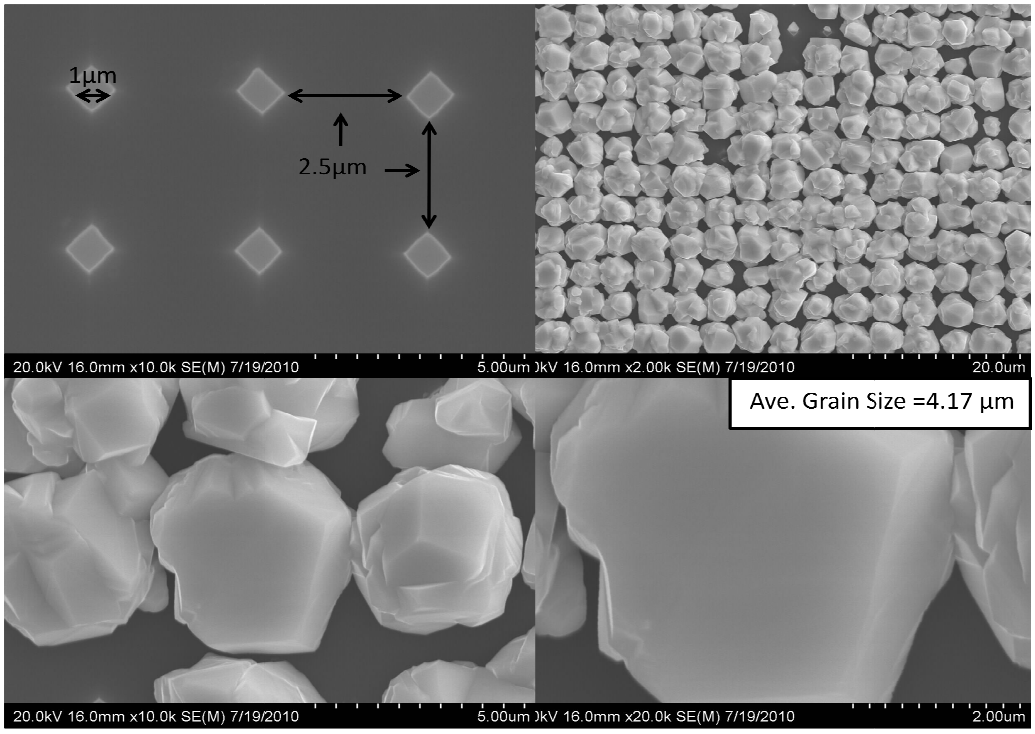

Figure 4.13. Surface SEM image of sample S3NPR, where the CdTe deposition process was performed for 5 minutes at Tsou=550ºC and Tsub=450ºC including the warm-up and deposition ramp steps.

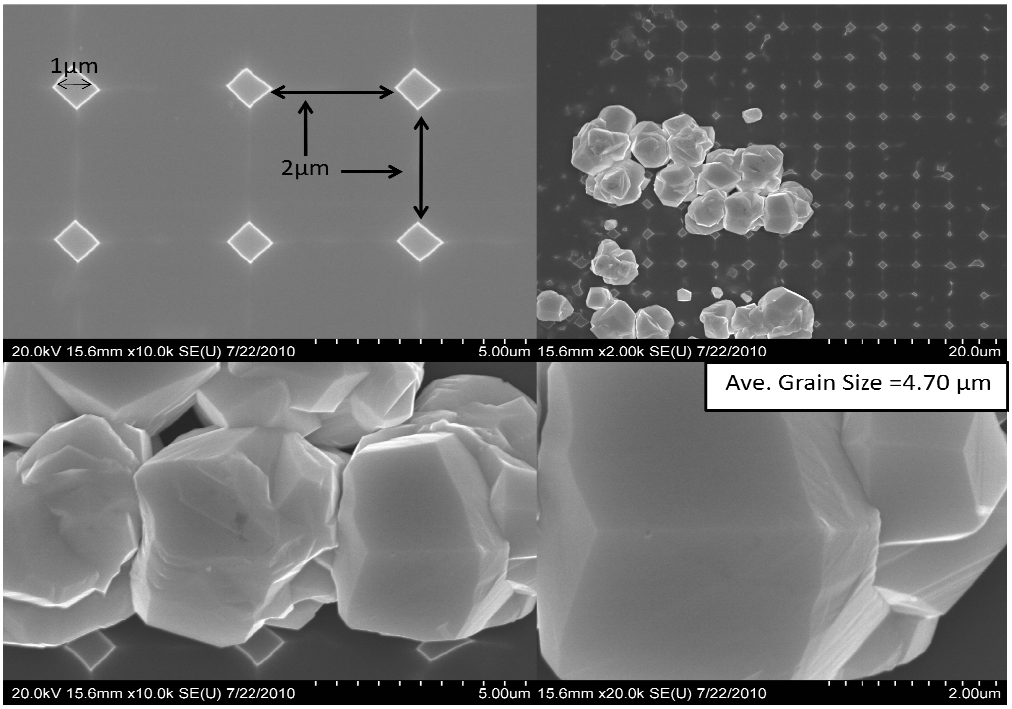

Figure 4.14. Surface SEM image of sample S10NPR, where the CdTe deposition process was performed for 5 minutes at Tsou=560ºC and Tsub=450ºC including the warm-up and deposition ramp steps.

Selectivity was achieved for all three samples, however, the CdTe did not deposit uniformly throughout the surface for all samples (Figs. 4.12 and 4.14). As the source temperature increased (constant substrate temperature of 450ºC), the CdTe grain size increased from 2.22 µm for a source temperature of 540ºC to 4.70µm for a source temperature of 560ºC. The CdTe grain deposited uniformly on the substrate surface for a source temperature of 550ºC (Fig. 4.13) and more grains that were considered high quality were observed for this sample. For this sample (S3NPR) the CdTe deposited appears to be a single grain, and the top surface of the grains was smooth, an indication of controlled growth. This will be confirmed with TEM analysis. The sample shown in Fig. 4.13 was considered to be the best sample in this work. The uniformity of the CdTe grain formation on the pillars could be due to the growth conditions of the pattern quality. It should also be noted that in most cases, growth appeared to nucleate at a corner of the pillars or on the side of the pillars. This is seen clearly for sample S9NPR in section 4.2.3.4. The average grain size was determined by measuring the largest dimension associated with 20 grains.

4.2.3.3. Selective CdTe growth on Si(100) with 450-500nm pattern for 5 min. deposition (Set III)

For the next set of patterned experiments similar temperature parameters were used for a smaller pattern size. Table 4.9 includes a summary of the experiments performed on Si(100) substrates with a 450 nm-500 nm pattern. Each deposition was carried out for 5 minutes for a substrate temperature of 450ºC and source temperatures between 530ºC and 550ºC. The CdTe deposition was performed for 5 minutes for all samples.

Table 4.9. Summary of experiments performed on Si(100) substrates with 450-500nm pattern for 5 min. deposition (Set III).

Sample	Pattern Size	Photoresist	Tsub (°C)	Tsou (°C)	Dep. Time	Uniformity	Quality
S5NPR	450 nm	Negative	450	530	5 min.	Yes	Multigranular
S6NPR	500 nm	Negative	450	540	5 min.	No	Multigranular
S5(2)NPR	450 nm	Negative	450	550	5 min.	No	Multigranular

SEM images for the samples listed in Table 4.9 are shown in Figs. 4.15 through 4.17. These images include a surface view of the substrate before and after CdTe deposition. Multiple micrographs are provided for the CdTe growth at low and high magnification. As mentioned beforehand, only negative photoresist was used for the reminder of the study. Sample S5NPR was patterned with negative photoresist and was dry etched for 3.45 minutes with SF_6 ionized gas, resulting in pillars at the nano-scale (450 nm diameter, 2 µm pitch). The CdTe deposition was performed for 5 minutes at T_{sou}=530ºC and T_{sub}=450ºC, where the average grain size was 3.70 µm in diameter (Fig. 4.15). Sample S6NPR was patterned with negative photoresist and was dry etched for 3 minutes with SF_6 ionized gas, resulting in pillars at the micron-scale (500 nm diameter, 2.5 µm pitch). The CdTe deposition was performed for 5 minutes at T_{sou}=540ºC and T_{sub}=450ºC, where the average grain size was 3.04 µm in diameter (Fig. 4.16). Sample S5(2)NPR was patterned with negative photoresist and was dry etched for 3.45 minutes with SF_6 ionized gas, resulting in pillars at the nano-scale (450 nm diameter, 3 µm pitch). The CdTe deposition was performed for 5 minutes at T_{sou}=560ºC and T_{sub}=450ºC, where the average grain size was 2.52 µm in diameter (Fig. 4.17).

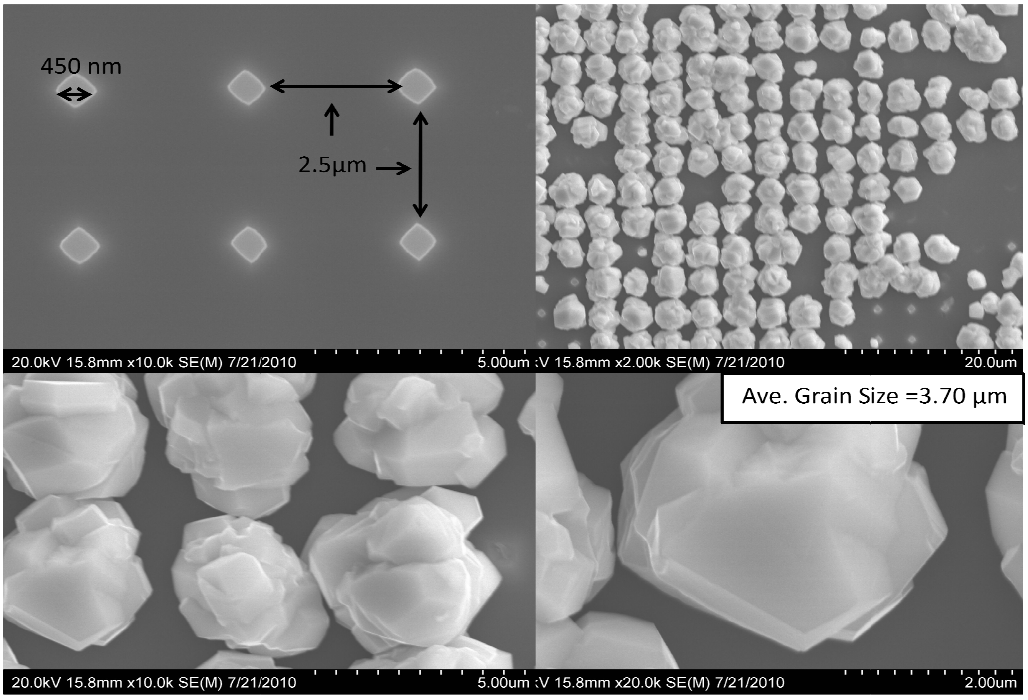

Figure 4.15. Surface SEM images of sample S5NPR, where the CdTe deposition process was performed for 5 minutes at Tsou=530ºC and Tsub=450ºC including the warm-up and deposition ramp steps.

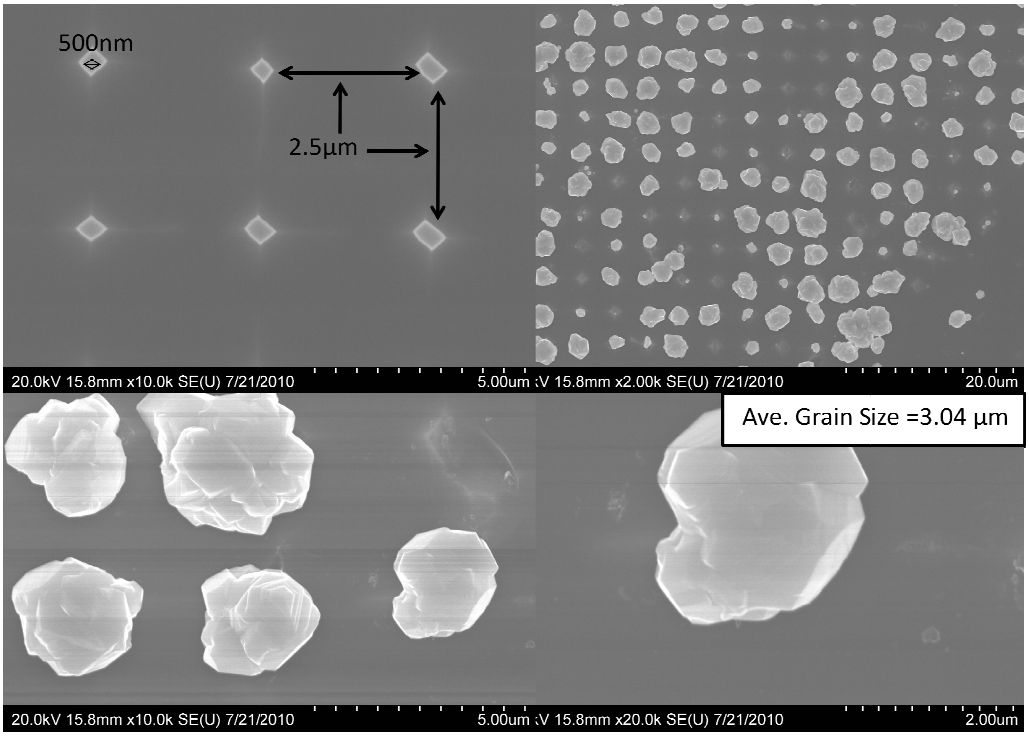

Figure 4.16. Surface SEM images of sample S6NPR, where the CdTe deposition process was performed for 5 minutes at =540ºC and =450ºC including the warm-up and deposition ramp steps.

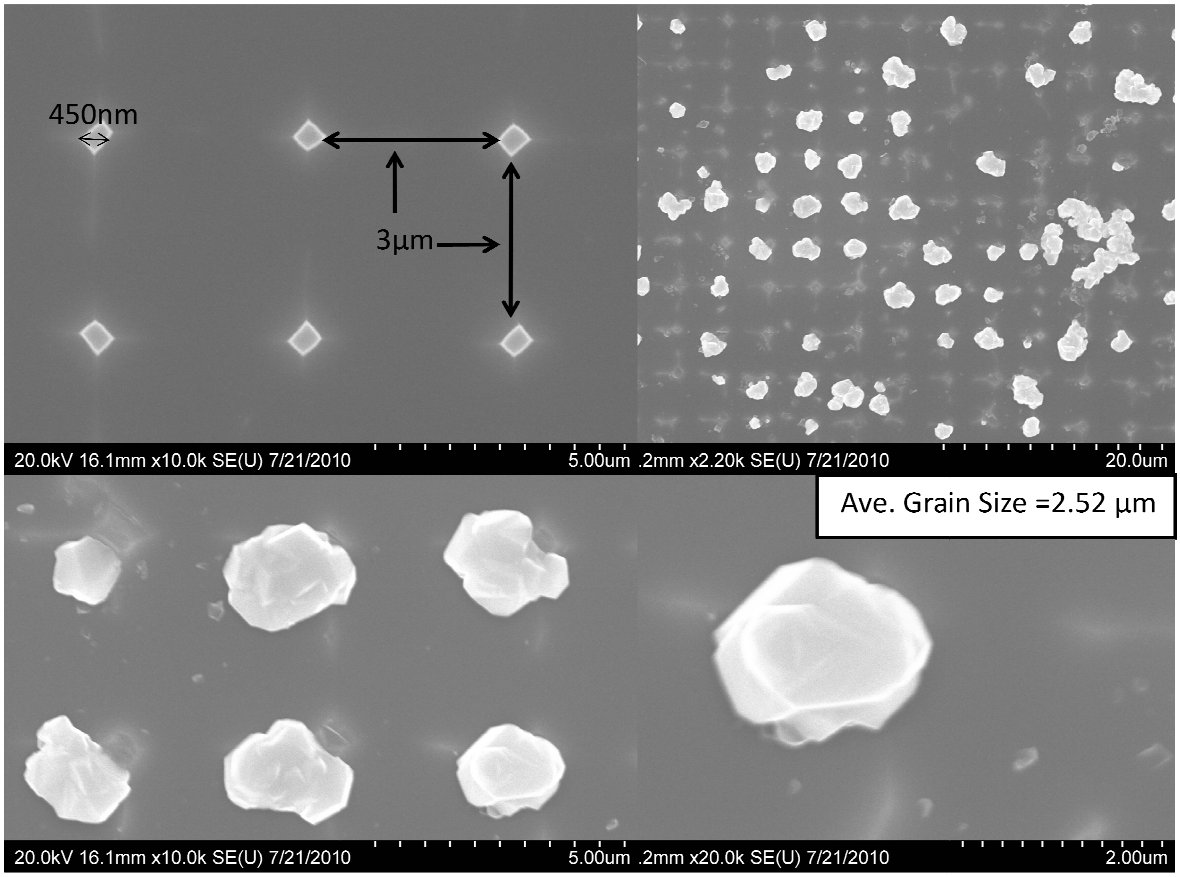

Figure 4.17. Surface SEM images of sample S5(2)NPR, where the CdTe deposition process was performed for 5 minutes at Tsou=550ºC and Tsub=450ºC including the warm-up and deposition ramp steps.

Selectivity was successfully achieved for all three samples, however, the CdTe did not deposit uniformly throughout the surface as the source temperature increased from 540ºC to 550ºC (Figs. 4.16 and 4.17). The uniformity of the CdTe grain formation could be due to the pattern quality. It can be noticed from Figs. 4.16 and 4.17 that the grain quality improved by increasing the source temperature from 530ºC to 540ºC, however, the uniformity of the pattern deteriorated (Figs. 4.15 and 4.16). Sample S6NPR is considered to be the best CdTe sample from set III, since the grains appear to be a single grain on top of each pillar and many of the grains exhibited smooth surfaces (Fig. 4.16). Because the uniformity in the CdTe growth across the patterned substrate was a problem for this set of experiments,

the deposition time was increased for the next set of experiments (Set IV). This was done in order to rule put time as a factor in growth uniformity.

As the source temperature increased, the CdTe grain size decreased from 3.70 µm for a source temperature of 530ºC to 2.52 µm for a source temperature of 550ºC.

4.2.3.4. Selective CdTe growth on Si(100) with 450nm-1µm pattern for 15 min. deposition (Set IV)

For the next set of experiments, it was decided to increase the deposition time from 5 minutes to 15 minutes, because insufficient nucleation was observed for the second set of patterned experiments where the growth time was only 5 minutes. By increasing the growth time to 15 minutes, sufficient growth time is given to ensure that this was not a limitation in the growth for this set of deposition temperatures and pattern size. Table 4.10 includes a summary of the experiments performed on Si(100) substrates with a 1 µm-500 nm pattern. Each deposition was carried out for 15 minutes in the CSS for substrate temperature of 440ºC and 450ºC, and source temperatures between 530ºC and 550ºC.

Table 4.10. Summary of experiments performed on Si(100) substrates with 450nm-1µm pattern for 15min. deposition (Set IV).

Sample	Pattern Size	Photoresist	Tsub (°C)	Tsou (°C)	Dep. Time	Uniformity	Quality
S1NPR	1 µm	Negative	440	530	15 min.	Yes	Multigranular
S9NPR	450 nm	Negative	450	540	15 min.	Yes	High quality
S8NPR	500 nm	Negative	450	550	15 min.	No	Mutigranular

SEM images for the samples listed in Table 4.10 are shown in Figs. 4.18 through 4.20. These images include a surface view of the substrate before and after CdTe deposition. Multiple micrographs are provided for the CdTe growth at low and high magnification. As mentioned beforehand, only negative photoresist was used for the reminder of the study. Sample S1NPR was patterned with negative photoresist and was dry etched for 3.45 minutes with SF_6 ionized gas, resulting in pillars at the micron-scale (1 µm diameter, 3 µm pitch). The CdTe deposition was performed for 15 minutes at T_{sou}=530ºC and T_{sub}=440ºC, and the average grain size was 4.20 µm in diameter (Fig. 4.18). Sample S9NPR was patterned with negative photoresist and was dry etched for 3.45 minutes with SF_6 ionized

gas, resulting in pillars at the nano-scale (450 nm diameter, 3 µm pitch). The CdTe deposition was performed for 15 minutes at Tsou=540ºC and Tsub=450ºC, and the average grain size was 2.00 µm in diameter (Fig. 4.19). Sample S8NPR was patterned with negative photoresist and was dry etched for 3 minutes with ionized gas, resulting in pillars at the nano-scale (500 nm diameter, 2.5 µm pitch). The CdTe deposition was performed for 5 minutes at Tsou=550ºC and Tsub=450ºC, and the average grain size was 4.99 µm in diameter (Fig. 4.20).

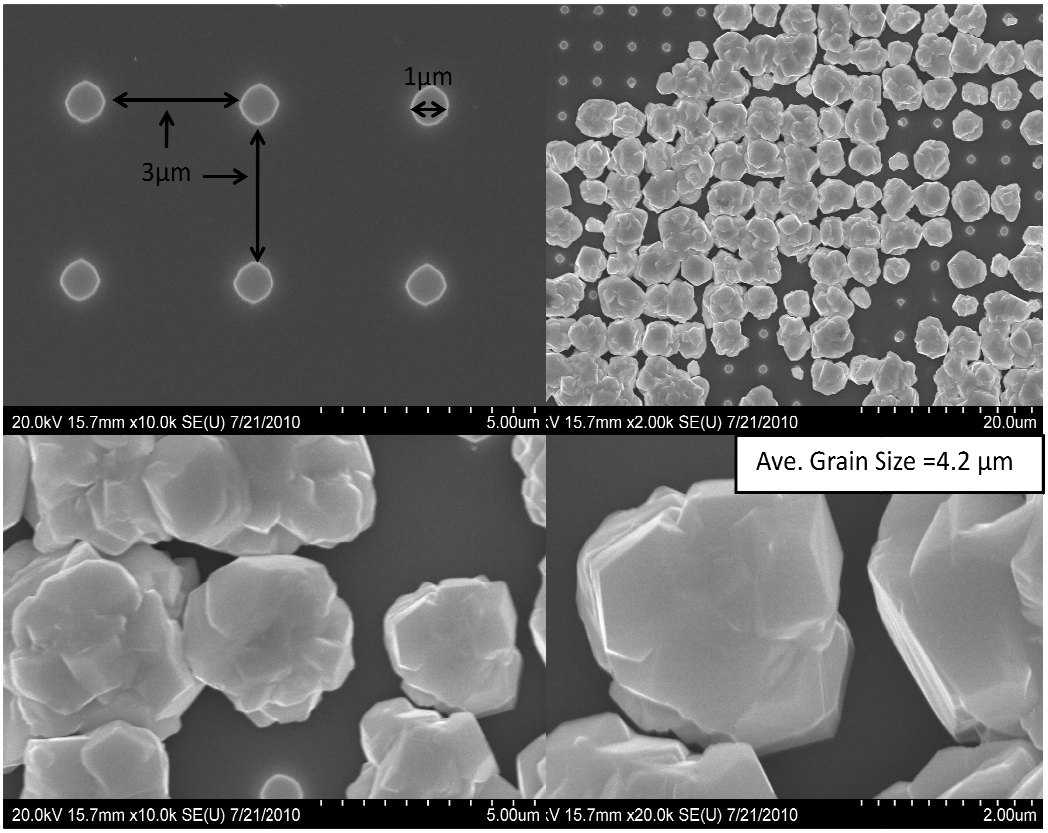

Figure 4.18. Surface SEM images of sample S1NPR, where the CdTe deposition process was performed for 15 minutes at Tsou=530ºC and Tsub=440ºC including the warm-up and deposition ramp steps.

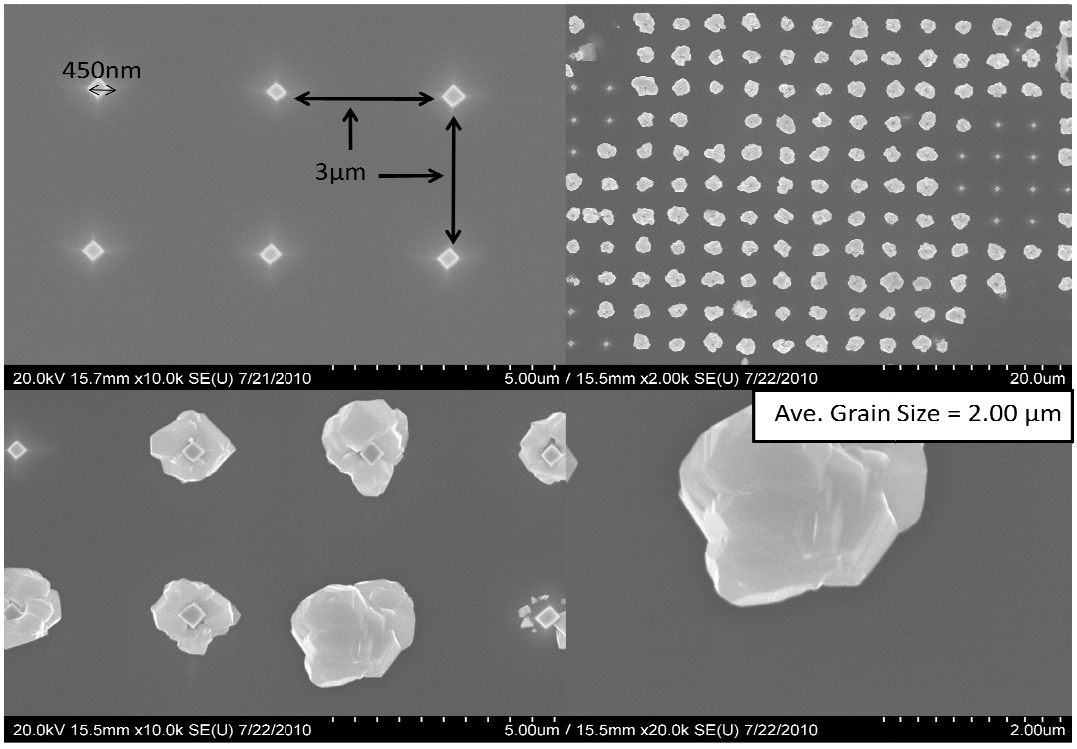

Figure 4.19. Surface SEM images of sample S9NPR, where the CdTe deposition process was performed for 15 minutes at Tsou=540ºC and Tsub=450ºC including the warm-up and deposition ramp steps.

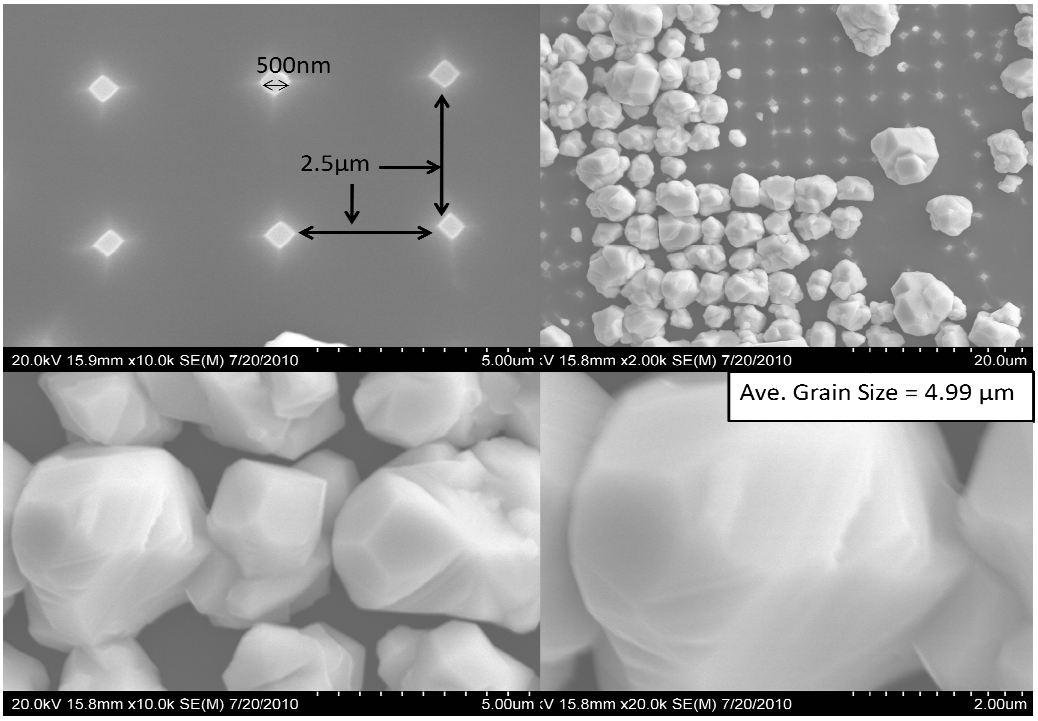

Figure 4.20. Surface SEM images of sample S8NPR, where the CdTe deposition process was performed for 15 minutes at Tsou=550ºC and Tsub=450ºC including the warm-up and deposition ramp steps.

Selectivity was achieved for all three samples, however as whit sets II and III of the patterned experiments, CdTe did not deposit uniformly throughout the sample with the highest source temperature of 550ºC (Fig. 4.20). For sample S1NPR, where the source temperature was 530ºC and the substrate temperature was 440ºC, the CdTe growth deposited uniformly on the patterned substrate, and the grains appeared to be of high quality with smooth surfaces. For sample S9NPR where the source temperature was increased to 540ºC, the grains also appeared to be of high quality. It is interesting to note that for this sample, the grains tended to nucleate and grow on the lateral sides of the pillar (Fig. 4.19). The increase in deposition time from 5 minutes to 15 minutes helped to improve the uniformity of the growth on the Si surface compared to samples where the growth times was only 5 minutes.

The grain size for this set of samples was dependent on the grain size and the deposition time of 15 minutes. The grain size was large (4.2 µm) for sample S1NPR (Fig. 4.18) which grew on 1 µm pillars at T_{sou}=530ºC, compared to sample S4NPR (2.22 µm) where the pillars were also 1 µm in size and T_{sou}=540ºC, but where the deposition time was only 5 minutes.

A comparison of sample S9NPR for T_{sou}=540ºC and sample S8NPR for T_{sou}=550ºC, where the pillars are 450 nm and 500 nm, respectively, the grain size increased from 2 µm to 4.99 µm as a result of the increase in source temperature.

4.2.4. Comparison to similar work

The best selective CdTe growth obtained in this study was for sample S3NPR, where selective CdTe growth was achieved for a deposition time of 5 minutes at source temperature of 550ºC and substrate temperature of 450ºC on a Si(100) substrate patterned with 1 µm pillars. The selective CdTe growth on a Si(211) substrate by A. Escobedo *et al.* [3] was compared to this sample. Figure 4.21 is a schematic of the work performed by Escobedo where Si(211) substrates with a CdTe film grown by molecular beam epitaxy (MBE) were patterned using a Si_3N_4 mask layer, where CdTe was then selectively grown on the CdTe windows using the CSS technique. The mask consisted of 1 µm windows within the Si_3N_4 layer exposing the CdTe underneath. The deposition was performed for 15 minutes at T_{sou}=530ºC and T_{sub}=450ºC. The differences between Escobedo's work and the study

presented here are (1) the substrate orientation, (2) a mask was not used in this work, and (3) a ZnTe buffer layer was used prior to CdTe deposition by MBE on the Si(211) substrates used by Escobedo [3]. Escobedo's goal was to deposit a single crystal CdTe grain on the CdTe(211) windows, where in this study, the goal was to deposit a single crystal CdTe grain on top of each Si(100) pillar without using a buffer layer and a mask layer. Figure 4.22 includes a comparison of the selective CdTe growth resulting from both studies.

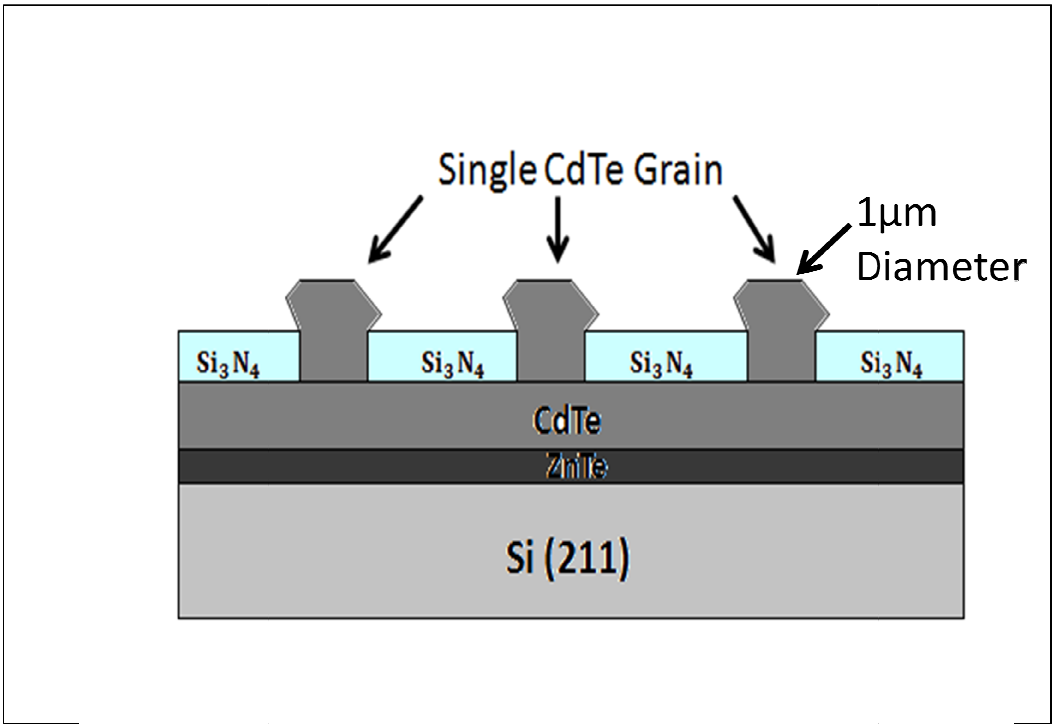

Figure 4.21. Schematic of selective epitaxial growth of CdTe on Si(211) substrate via CSS technique performed by Escobedo.

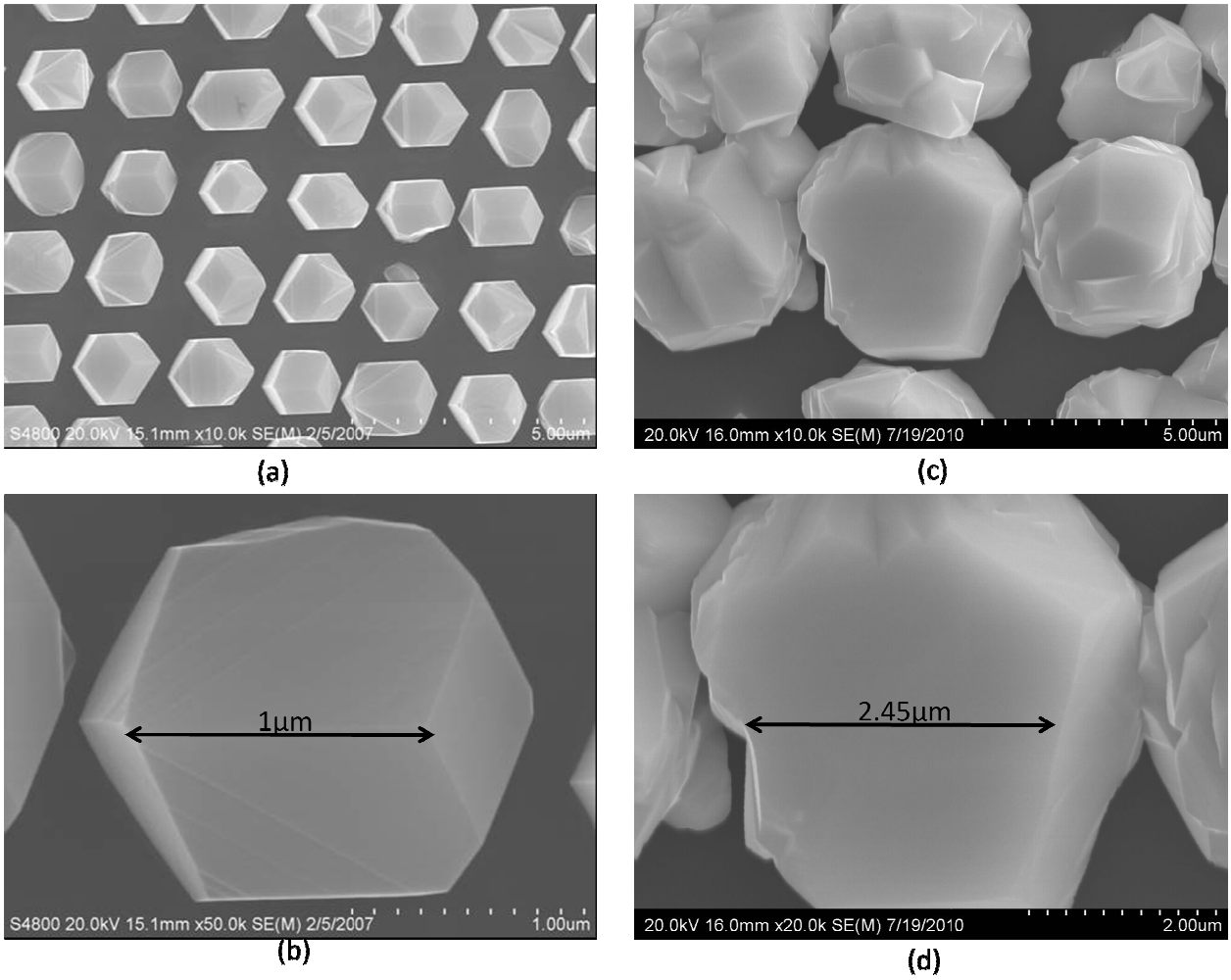

Figure 4.22. Surface SEM image of (a) Escobedo's work at low magnification, and (b) high magnification [3], (c) Sample S3NPR at low magnification, and (d) high magnification.

Fig. 4.22(a) and (b) are low and high magnification SEM images of Escobedo's work, showing single CdTe grains deposited on patterned CdTe/Si(211) substrates. The CdTe growth resulted in 1µm in diameter high faceted CdTe grains. TEM analysis confirmed that these were single crystal CdTe grains with twins.

Figs. 4.22(c) and (d) show the growth of 2.45 µm grains on 1 µm pillars without a buffer layer and without a mask. A TEM study will be performed for this sample in order to characterize the structure and quality of the CdTe grain. Similar work was performed by Bhat and Zhang [20], where

selective epitaxial growth of CdTe on patterned GaAs(100) substrates using a 100 nm mask layer was achieved. The GaAs(100) substrate was patterned using standard photolithography resulting in a 8x8 array of 5 µm x 5µm squares. The selective epitaxial growth of CdTe growth was performed via metalorganic vapor phase epitaxy (MOVPE) technique. Perfect selective growth was achieved at a temperature of 550ºC and a pressure of 25 Torr. Figure 4.23 illustrates a surface SEM image of the work performed by Bhat and Zhang, and the work performed in this study for the same sample shown in Figs. 4.22(c) and (d).

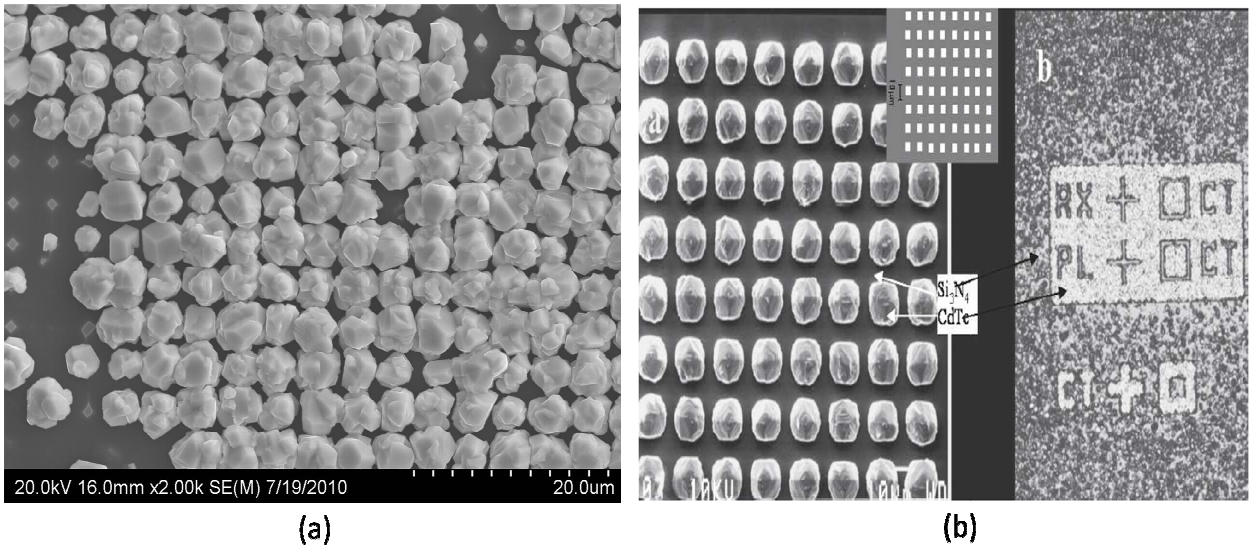

Figure 4.23. Surface view SEM image of (a) sample S3NPR via CSS technique, and (b) SEM image and optical micrograph of selective CdTe growth on GaAs(100) substrate using mask layer [20].

It can be observe from Fig. 4.23 that the work performed in this study is similar to that of Bhat and Zhang, even though CdTe was grown on two different materials, Si(100) and GaAs(100) substrates. No structural comparisons were made between the two studies.

Chapter 5: Conclusions

The first set of experiments consisted of the deposition of planar CdTe on CdTe(111) substrates, resulting in growth rates between 5 and 10 µm/hr, with a FWHM of 180 arcsec. The second set of experiments consisted of the deposition of planar CdTe on Si(100) substrates, resulting in growth rates between 6 and 10 µm/hr, with a FWHM of 216 arcsec. Lastly, CdTe was selectively deposited on patterned Si(100) substrates, where selectivity was achieved for all source and substrate temperatures analyzed. Selective CdTe grains were observed for T_{sou} =550ºC and T_{sub} =450ºC. Moreover, a summary of the most important results will be explained in the following section.

5.1 Planar epitaxial growth of CdTe on CdTe(111)

Several set of experiments were performed to achieve a high quality CdTe/CdTe(111) film via CSS technique. This set of experiments consisted of varying the source and substrate temperature. The following can be concluded from the results obtained:

1) The growth rate is proportional to the source temperature.
2) The average growth rate based on these values varied between 5-10 µm/hr. This differs from Escobedo's work, where the CdTe growth rate was approximately 1.5 µm/hr under similar deposition growth conditions.
3) As the T_{sou} was increased, the film morphology improved.
4) The highest quality film resulted from the growth parameters, where the T_{sou} =530ºC and T_{sub} =350ºC.
5) A rocking curve FWHM value of 180 arcsec was obtained for CdTe planar growth on CdTe(111). This compares to a FWHM value of 136 arcsec from prior work [3].

5.2 PLANAR EPITAXIAL GROWTH OF CDTE ON SI(100)

Several set of experiments were performed to achieve a high quality CdTe/Si(100) film using the CSS technique. This set of experiments consisted of varying the source and substrate temperature, as well as the deposition and annealing times. The following can be concluded from the results obtained:

1) The growth rate is proportional to the source temperature.
2) The CdTe growth rates for CdTe on Si(100) are comparable to those for CdTe growth on CdTe(111). The growth rate varied between 6 and 10 μm/hr. When the source temperature was increased to 550°C, the growth rate increased to 15 μm/hr.
3) The same parameters used to produce the highest quality CdTe films on CdTe(111) were found to be optimum for Si(100) as well.
4) Annealing improves the quality of the CdTe films on Si(100).
5) A rocking curve FWHM value of 216 was obtained for CdTe planar growth on Si(100).

5.3 SELECTIVE EPITAXIAL GROWTH OF CDTE ON SI(100)

Several set of experiments were performed to achieve a high quality selective CdTe/Si(100) film via CSS technique. This set of experiments consisted of varying the source and substrate temperature, as well as the deposition time. The following can be concluded from the results obtained:

1) CdTe selectivity was achieved for all substrate and source temperatures used in this study.
2) Selective growth of CdTe on Si(100) substrates was achieved without the use of a mask.
3) CdTe grains with smooth surfaces were achieved for some growth parameters, while multifaceted grains were also observed for other parameters.
4) The pattern quality may have an effect on the selective growth of CdTe grains in terms of quality and uniform CdTe growth.

5) Negative photoresist results in a smooth surface for subsequent deposition.
6) Increasing T_{sou}, increases the grain size.
7) Increasing the deposition time increases the grain size and the uniformity of the selective CdTe deposition.
8) Decreasing the pattern size decreases the grain size.
9) The CdTe appears to nucleate on the sides of the pillars.
10) High quality CdTe grains on patterned Si(100) substrates were observed for T_{sou}=550ºC and T_{sub}=450ºC for 5 minutes of growth.

Overall, the results presented in this thesis demonstrated that it is possible to produce high quality CdTe films using the CSS technique. In addition, it was proved that CdTe can be selectively deposit on patterned Si(100) substrates resulting in high quality films for the subsequent growth of HgCdTe films. Especially important, is that this was accomplished without the use of a mask.

5.4 FUTURE WORK

1. TEM will be performed to examine the quality of the grain structure or the CdTe/Si interface.
2. Selective deposition on patterned Si(211) substrates without a buffer layer and without a mask, since Si(211) substrates results in less twins.

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Curriculum Vita

Aryzbe Diaz was born on November 7, 1984 in Cd. Juarez, Chihuahua, the oldest daughter of Silvia Vences and Venancio Diaz. She moved to El Paso, Texas when she was 11 years old, without knowing a word of English. In May 2003 she graduated from Montwood High School in the ten top percent of her class out of 650 students, and with the National Honor Society honors. She started her professional career as an Electrical and Computer Engineer at the University of Texas at El Paso (UTEP) on August 2003. As an undergraduate student, she had the opportunity to just dedicate all her time to school work, which it was worth it because this helped her to obtained good grades in her courses. In May 2008, she earned her Bachelor's of Science in Electrical and Computer Engineering, and enrolled in the UTEP graduate school in Fall 2008. As a graduate student, she became a member of the NanoMIL group at UTEP and obtained a position as a research assistant. Being a research assistant gave her a great experience in her field, semiconductor devices, and the opportunity to expose her work in conferences as wells as working with other research assistants from other fields. Also, she had the opportunity to work as a tutor with the GEAR UP organization at Jefferson High school, helping freshman students with their mathematic courses. In January 2010, she was awarded the National Science Foundation (NSF) Bridge to the Doctorate Fellowship, which support her financially to finish her Master's career and continue with her Ph.D.

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