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# Nanoprobe I-V Characterization of CdTe/CdS Micro and Nano-patterned Solar Cells

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NANOPROBE I-V CHARACTERIZATION OF CDTE/CDS MICRO AND  
NANO-PATTERNED SOLAR CELLS

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Heber Prieto

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**To my lovely parents and sisters.**

NANOPROBE I-V CHARACTERIZATION OF CDTE/CDS MICRO AND  
NANO-PATTERNED SOLAR CELLS

by

HEBER PRIETO, B.S.E.E.

THESIS

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Special thanks to my parents and sisters whose support and love were very important to keep me motivated during this work.

## **ABSTRACT**

This thesis presents a novel way to characterize micro and nano patterned cadmium telluride thin film solar cells via a nano-probe system. A historical review of CdTe-based solar cells is presented first followed by review of the technology developed to produce the patterned CdTe cells. A detailed presentation is then provided on the use of a Zyvex nanoprobing system to characterize the patterned solar cells. The I-V response of micro- and nano-patterned solar cells stimulated under different e-beam conditions is presented and analyzed. Suggestions of how to improve the technique are provided. This work documents, for the first time, the I-V testing of isolated CdTe grains of different feature size.

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## CHAPTER 1: INTRODUCTION

### 1.1 History of CdTe solar cells

CdTe is one of the most promising materials for solar cells fabrication because of its ideal bandgap, low manufacturing cost and maximum theoretical efficiency of 29%. [1] Over the last 26 years many technological developments have been achieved to increase the efficiency of CdTe/CdS cells. To date, the highest recorded efficiency is 17.3% for laboratory scale CdTe/CdS devices. Some of the most important developments include a cadmium chloride ( $\text{CdCl}_2$ ) treatment for CdTe growth and re-crystallization, thinning of the CdS thickness to increase quantum efficiency, and the creation of a stable back-contact. Figure 1 presents a timeline of the world record conversion efficiencies achieved by companies and academia. [2]

The research of cadmium telluride (CdTe) as a solar energy material began in the 1950's, but it wasn't until the 1960's when General Electric (GE) started fabricating devices in mass production. In 1976 the creation of the first high efficiency CdTe solar cell (8.1%) using vapor deposition in vacuum was achieved. This work was done at Matsushita Electric Industrial Co. by Nakayama and Matsumoto. In this work, a model cell was made to clarify the junction formation and their preliminary conclusion was that the solar cell had a hetero-junction structure. [3]

In 1980, the research initiated by Monosolar Inc. and headed by Basol, focused their efforts on cathodic electro-deposition of CdTe. Such efforts increased the fill factor, which resulted in an efficiency of 10.3%. Also, this research work introduced the formation of a rectifying junction between the n-type and p-type films. [4]

In 1981 the Eastman Kodak Co. implemented the close spaced sublimation (CSS) technique and the use of oxygen during thin film growths of CdTe-based photovoltaics. The use

of oxygen by Tyan and Perez-Alburne enhanced the doping of the p-type CdTe layer and resulted in solar cell efficiencies of 10.5% [5]

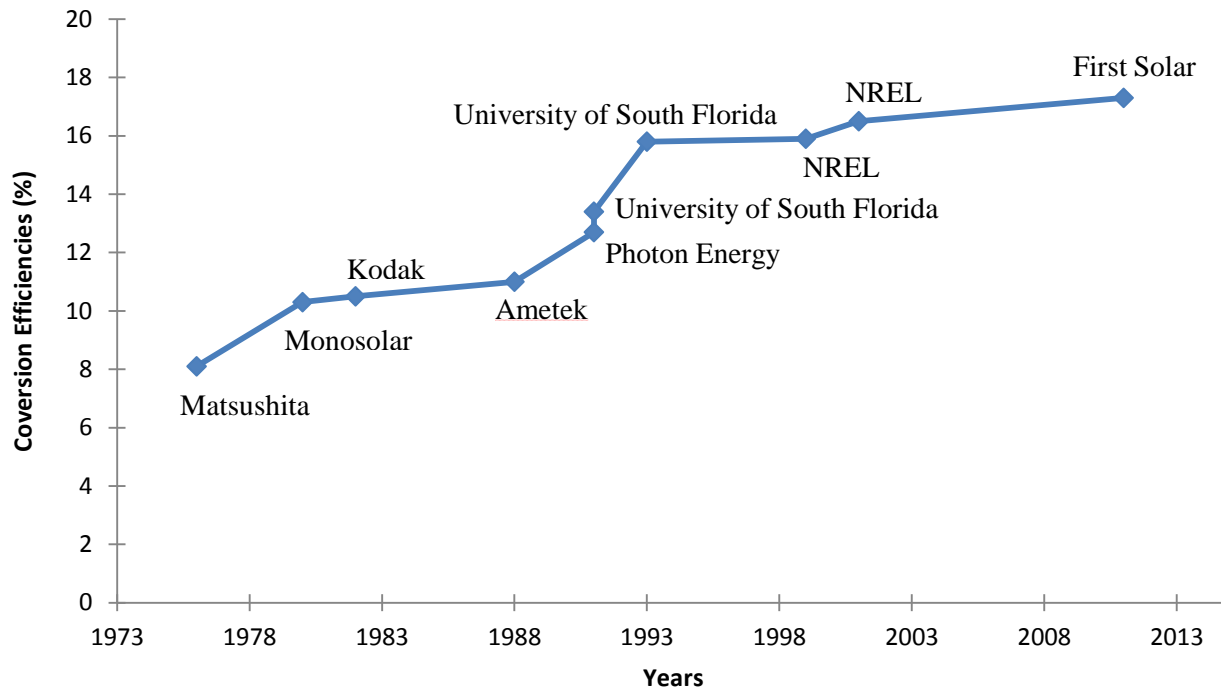


Figure 1. Record breaking CdTe solar cells chart. [2]

Later in 1988, Ametek Applied Materials Laboratory created an 11% efficient CdTe cell by eliminating problems related to a low-resistance back contact. Moreover, the team headed by Meyers demonstrated that an increment in the efficiency was possible by reducing absorption and reflection in the top layers. [6]

In 1984, Photon Energy Inc. (PEI) started major efforts for the production of efficient, large-area and low-cost photovoltaic modules. One of the big improvements made by PEI in 1989 was to make a thinner layer of CdS which allowed more light to reach the junction and increased the efficiency to 12.3%. [7] Two years later (1991), the same company beat its own record efficiency to 12.7% by reducing the resistivity of the tin oxide ( $\text{SnO}_2$ ) layer. [8]

Also, in 1991, an efficiency of 13.4% was reported by the University of South Florida. In this development, the deposition techniques used by Dr. Chu's team were chemical bath deposition (CBD) for the CdS layer and close-space sublimation (CSS) for CdTe. [9] The same group of researchers increased the efficiency to 14.6% in the following year. The differences are noted in the deposition of a thinner CdS layer, the deposition of CdTe at a higher temperature and the use of magnesium fluoride ( $\text{MgF}_2$ ) used as antireflection coating. [10] Furthermore, the University of South Florida team reported a new record of 15.8% in 1993 by optimizing its process. [11]

The National Renewable Energy Laboratory (NREL) matched the USF record in 1999 and surpassed it in 2001 producing a 16.5% efficient CdTe based solar cell. Dr. Wu and his team utilized the CBD technique for the CdS layer and CSS for CdTe in the fabrication of photovoltaics. Among the biggest improvements developed by NREL was the use of cadmium stannate (CTO) instead  $\text{SnO}_2$  and the introduction of zinc stannate (ZTO) as a buffer layer; these helped in the reduction of series resistance and increase of shunt resistance, respectively. [12]

As noted in Figure 1, NREL kept the title for creating the CdTe solar cell with highest efficiency for ten years. However, in 2011, First Solar achieved a new world record for CdTe photovoltaics of 17.3%. [13]

Table 1. Summary of CdTe solar cell record efficiencies parameters.

<b>Company</b>	<b>Year</b>	<b>CdS deposition Technique</b>	<b>CdTe deposition Technique</b>	<b>Jsc (mA/cm<sup>2</sup>)</b>	<b>Voc (mV)</b>	<b>FF</b>	<b>Efficiency (%)</b>
<b>Matsushita</b>	1976	Screen printing	Screen printing	11.2	690	Info. not available	8.1
<b>Monosolar</b>	1980	Electrodeposition	Cathodic electrodeposition	21.23	725	.67	10.3
<b>Kodak</b>	1982	CSS	CSS	17	750	.62	10.5
<b>Ametek</b>	1988	Pyrolysis	Electrodeposition	20.1	763	.72	11
<b>Photon Energy</b>	1991	Spray Deposition	Spray Deposition	26.21	799	.605	12.7
<b>University of South Florida</b>	1991	CBD	CSS	21.9	840	.726	13.4
<b>University of South Florida</b>	1993	CBD	CSS	25.09	843	.740	15.8
<b>NREL</b>	2001	CBD	CSS	25.88	845	.755	16.5
<b>First Solar</b>	2011	Info. not available	Info. not available	Info. not available	Info. not available	Info. not available	17.3

As it is shown by Table 1, the efficiency and deposition techniques for CdTe solar cells have improved with time. One of the electrical characteristics that improved the most is the short circuit current density ( $J_{sc}$ ), which is very close to attaining the maximum expected value for CdTe thin films. As mentioned before, other improvements include, progress in the thickness and uniformity of the CdS layer, creation of an optimal back contact, as wells as the implementation of cadmium chloride ( $CdCl_2$ ) treatment.

Although major advancements have been realized, there is potential to increase the efficiency further by increasing the open-circuit voltage ( $V_{oc}$ ) and fill-factor (FF). In order to accomplish this, several fundamental problems will need to be addressed including; a large lattice mismatch (~10%) between CdTe and CdS, the spatial/morphological non-uniformity of grains in thin films, and the high density of defects and grain boundaries. These problems have been identified as major contributors to the low efficiencies primarily through low  $V_{oc}$  and low FF.[14]

## CHAPTER 2: PATTERNED SOLAR CELLS BACKGROUND

### 2.1 UTEP research on CdTe thin films

In order to overcome the problems inherent with random polycrystalline thin films, a fabrication technique to create ordered arrays of high quality crystals has been developed by UTEP researchers. [15]

The work by Terrazas focused in the deposition of a patterned dielectric growth mask and the selective-area deposition of ordered CdTe poly-crystals. The schematic in Figure 2 represents the main idea of using a dielectric mask to accomplish the growth selectivity of CdTe.

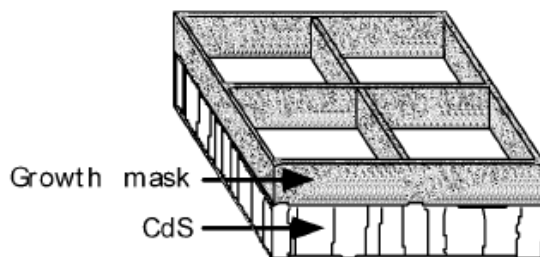


Figure 2. Schematic representation of dielectric mask on CdS film. [15]

Growth selectivity is the growth of a material in specific regions of the substrate. This is achieved by the difference in surface mobility between the dielectric and substrate materials. [16] Thus, Figure 3 shows a CdTe selective deposition on CdS/dielectric substrate.

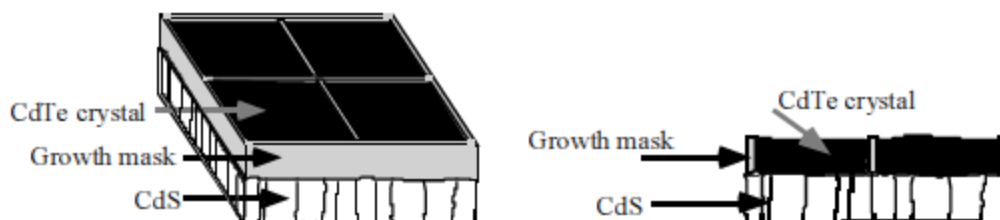


Figure 3. Perspective (left) and cross-sectional (right) schematics of a 2x2 array of ordered CdTe crystals grown on CdS. [16]

Previous work has shown that  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$  can be used as growth masks to achieve selective-area deposition and realize the structure shown in Figure 3. However,  $\text{SiO}_2$  was selected for the work by Terrazas since it is believed to be more suitable than  $\text{Si}_3\text{N}_4$  for passivation of CdTe.

Patterned deposition of the mask was achieved using copper grids. The copper grids contained a squared array of wires (200, 400 or 600 mesh). The 200 mesh had wires with a width of  $10\text{ }\mu\text{m}$  separated by  $115\text{ }\mu\text{m}$ . Similarly, the 400 and 600 mesh had wire widths of  $7\text{ }\mu\text{m}$  and  $5\text{ }\mu\text{m}$ , and separations of  $55\text{ }\mu\text{m}$  and  $37\text{ }\mu\text{m}$ , respectively. Figure 4 shows the way these grids were placed on the substrate. [15]

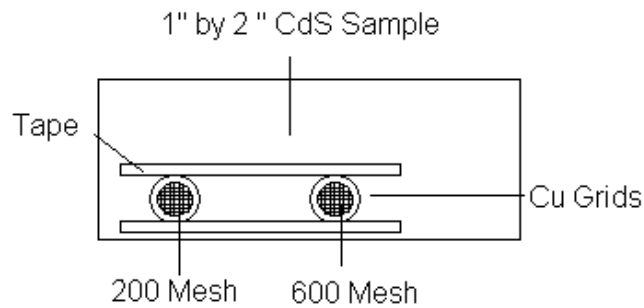


Figure 4. Plan view of grids placed on the substrate. [15]

It is important to mention that, the work done by Terrazas resulted in negative tone relative to the structure of Figure 3. In other words, the  $\text{SiO}_2$  was patterned into isolated squares, and the CdS was patterned into a connected grid. As shown in Figure 5, the CdTe deposited on CdS in three kinds of selectivity; positive, zero and negative.

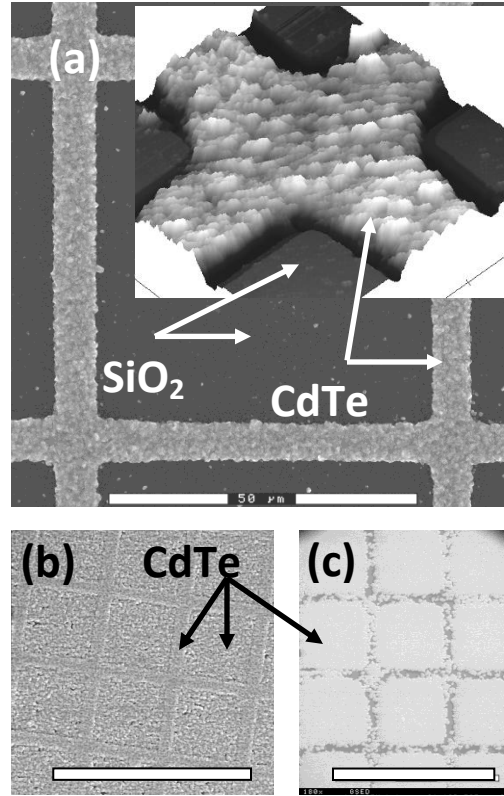


Figure 5. Comparison of selective growth of CdTe on CdS at different temperatures. As the temperature is increased, the selectivity transitions from (a) positive to, (b) zero to (c) negative selectivity. [15]

Following the work done by Terrazas; C. Lopez focused efforts to decrease the area of the patterned windows from 6 to 1 micron and also to obtain a positive selectivity and non-inverted structure. [17] In this research work, photolithography and a lift-off process was used to create the patterned  $\text{SiO}_2$  layers on CdS. The basic process sequence is shown in Figure 6. [17]

Lopez then proceeded to deposit CdTe on the patterned substrates. SEM images of selective-area depositions of CdTe showing the effect of CdTe thickness and patterning size are shown in Figure 7. Each column represents a distinct CdTe thickness of either 300 nm, 750 nm or 1000 nm from left to right. Each row corresponds to a different patterning pitch of 2  $\mu\text{m}$ , 3  $\mu\text{m}$ , 4  $\mu\text{m}$ , 5  $\mu\text{m}$  or 6  $\mu\text{m}$  respectively from top to bottom. [18]

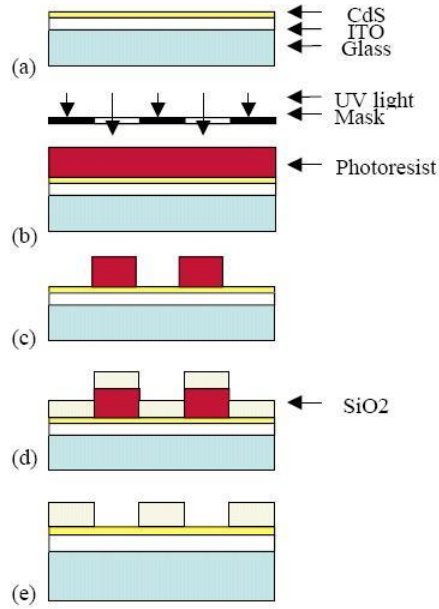


Figure 6. Illustration of the process sequence for a negative photoresist SiO<sub>2</sub> substrate patterning. (a) Glass/ITO/CdS substrate (b) negative photoresist applied to the substrate and UV light exposure through the photomask (c) sample after exposure and photoresist development (d) silicon dioxide deposition (e) final structure following lift-off procedure. [18]

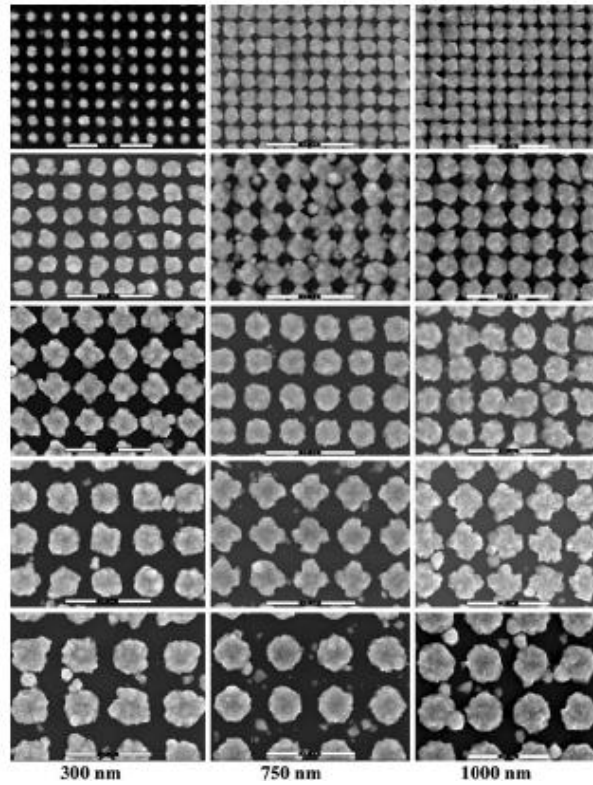


Figure 7. Plan view SEM images of ordered arrays of CdTe on CdS. The size of the patterning increases from top to bottom while the thickness of the CdTe increases from left to right. [18]

More work on selective deposition of CdTe has been performed by other researchers. For instance, work done by Bommena [19], also demonstrates the selective growth of CdTe on nano-patterned silicon substrates by using molecular beam epitaxy (MBE) as shown in Figure 8.

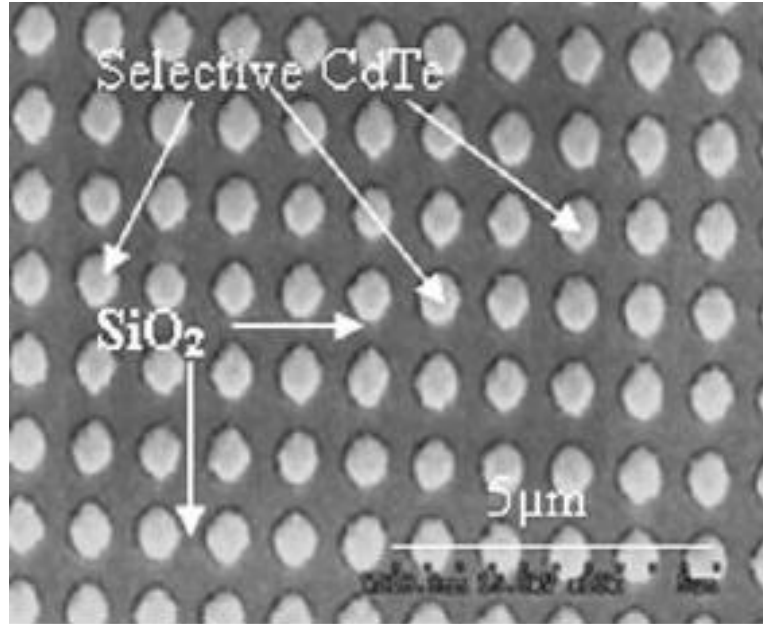


Figure 8. Selective CdTe after 3600 s of growth. [19]

Rodriguez [20] continued the research of the CdTe ordered arrays applied into the fabrication of micro-patterned solar cells. The work accomplished by Rodriguez showed, for the first time, the use of CdTe micro-arrays for the development of thin film photovoltaics (Figure 9).

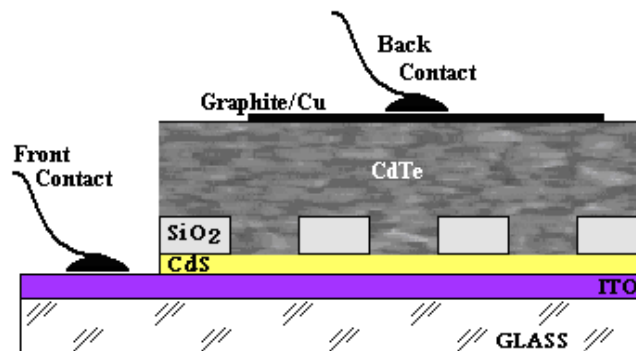


Figure 9. Cross sectional view of completed micro-patterned solar cell. [20]

Recently, the NanoMIL research group has been working to improve the efficiency of CdTe photovoltaics by using nano-size windows to reduce the defects in CdTe layer and at the CdS/CdTe interface. One of the biggest challenges of this project has already been achieved by selectively depositing CdTe on nano-patterned substrates of 300nm in feature size as shown by Figure 10. The next step for this achievement is the fabrication of nano-patterned solar cells.

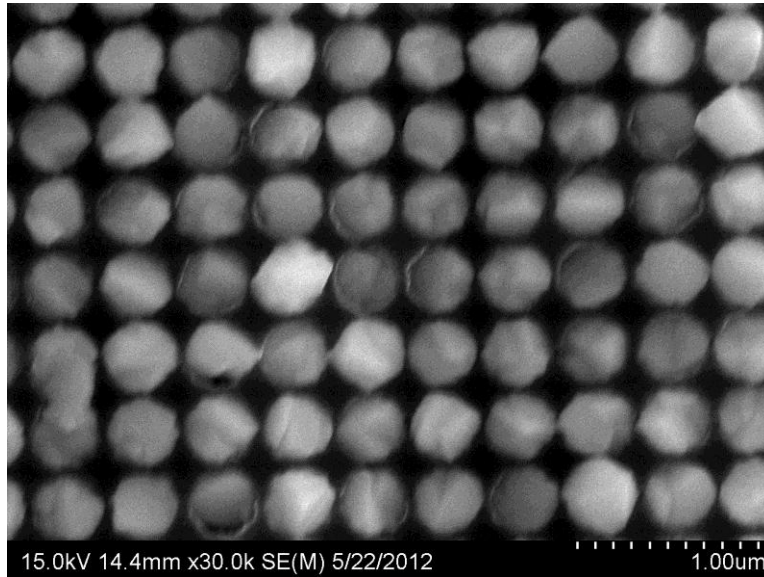


Figure 10. SEM top view of nano-patterned CdTe/CdS substrate.

## 2.2 Motivation and contribution of this thesis

It was found that the combination of defects present in grain boundaries and the random nature of common processes complicate the scientific study and technological development in random polycrystalline thin-films. The Nano-Materials Integration Laboratory (NanoMIL) at UTEP has proposed an approach to overcome these problems associated with random polycrystalline thin films. The approach consists of two main steps: (1) the creation of a micro/nano patterned mask and (2) the selective-area deposition of CdTe ordered poly-crystals. [15] It is believed that these ordered structures have several advantages over random polycrystalline films. One advantage is that, when precisely deposited, uniform crystals in size

and shape are created. Another advantage is that recombination centers produced by the large lattice mismatch between CdS and CdTe ( $\sim 10\%$ ) can be greatly reduced. [15] The motivation of this thesis is to measure the I-V performance of individual grains using a nano-probe.

The contribution of this thesis is to perform electrical characterization of isolated CdTe grains grown on nano and micro-patterned substrates. The characterization consists of obtaining I-V measurements from grain arrays and correlating the I-V performance to the input stimulus and microstructure of the CdTe grains. The I-V response of the measured islands will give information primarily on the open-circuit voltage and current density. Also, future work to improve the nano-probing technique is discussed in this paper.

## CHAPTER 3: SAMPLE FABRICATION

In this Chapter the process to fabricate the device shown in Figure 9 is discussed. As it can be observed from Figure 9, the device is composed of different layers, these layers are deposited utilizing different techniques.

### 3.1 Cadmium Sulfide Deposition

The CdS film is the n-type layer of the photovoltaic device. Its main function is to transport electrons to be collected to the front contact. This film is deposited by chemical bath deposition (CBD) on commercial purchased ITO/glass substrates. The advantages of this deposition technique are; it is relatively inexpensive, the thickness of the layer is easy to control and it is uniform. In other words, it avoids the formation of pinholes. Once the proper cleaning procedures of the ITO/glass are followed, as described by Ordonez [21], the CdS is ready to be deposited.

Cadmium sulfide is grown via an aqueous solution made of cadmium acetate, ammonium acetate and ammonia. [17] This mixture is added to a beaker with DI water heated at 70°C. Once the substrate is submerged in this solution, thiourea is slowly added in intervals of 30 seconds. The deposition rate under the conditions mentioned above is around 2nm/min. A thickness from 60 to 80nm was attained in most of the samples used in this research. A yellowish color on the substrate characterizes the CdS presence. Cadmium sulfide is highly transparent due to its large band gap (2.4 eV) which easily permits the transmission of light to the CdTe. After the CdS is deposited, the substrate is ready for the patterned mask growth.

### 3.2 SiO<sub>2</sub> film deposition techniques

Micro and nano-patterned films deposited with different methods were used for this research work. The SiO<sub>2</sub> was deposited using plasma-enhanced chemical vapor deposition (PECVD). The SiO<sub>2</sub> mask was then patterned using standard optical lithography for micro-patterned samples and Step and Flash Imprint Lithography Reverse Tone technique for nano-patterned films.

#### 3.2.1 Micro-patterned windows

The method used for the creation of the micro-patterned substrates is standard optical lithography. This process involves the creation of patterns on a wafer's surface. This technique uses light to transfer a pattern to a photoresist in the substrate. First, 200 nm of SiO<sub>2</sub> is deposited via PECVD on CdS/ITO/glass substrates. Subsequently, a negative photoresist is applied to the substrates. Then, the photoresist is patterned and finally the SiO<sub>2</sub> is etched.

Figure 11 and Figure 12 show patterned substrates with window openings in the SiO<sub>2</sub> layer. The substrates consist of patterned-SiO<sub>2</sub>/CdS/ITO/glass.

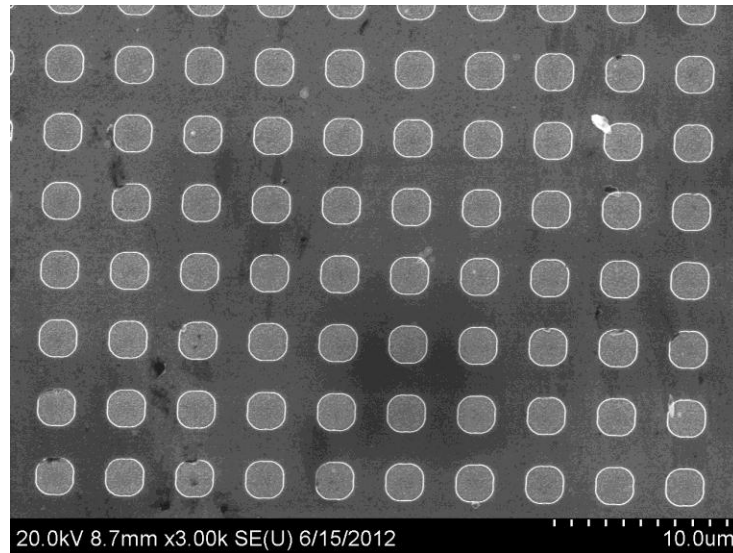


Figure 11. SEM image of patterned SiO<sub>2</sub> on CdS with 2  $\mu$ m feature size at 3.0k magnification

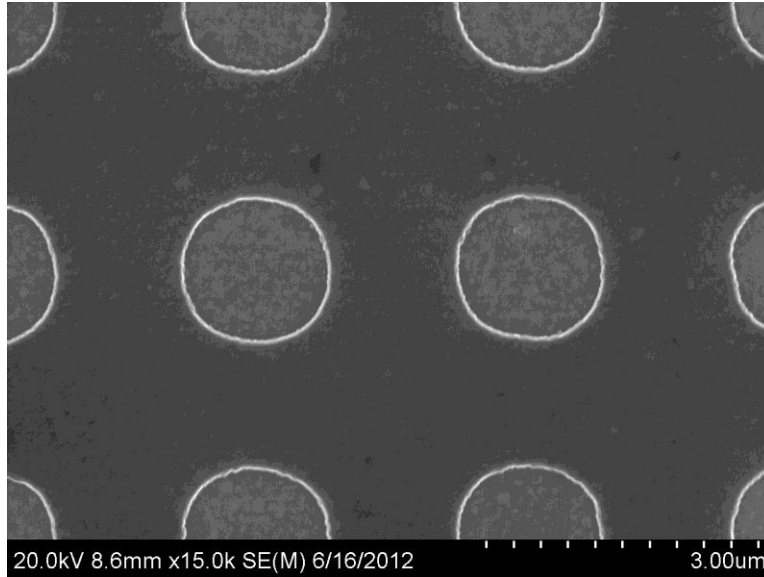


Figure 12. SEM image of patterned SiO<sub>2</sub> on CdS with 1.5 μm feature size at 15.0k magnification.

### 3.2.2 Nano-patterned windows

The nano-patterned substrates used in this work were obtained using Step and Flash Imprint Lithography Reverse Tone (SFIL/R). This is a relatively new method to create nanometer scale patterns. The SFIL/R is a reverse variant of SFIL which provides advantages such as; higher selectivity during etching compared to other pattern techniques, superior *in situ* alignment and defect control. [22] An in depth explanation of this technique can be found in the work done by Miller. [23]

Arrays of nanometer-scale holes in SiO<sub>2</sub> of approximately 300 nm in diameter were achieved using SFIL/R. Figure 13 shows CdTe selectively deposited in the 300 nm holes as desired for this work.

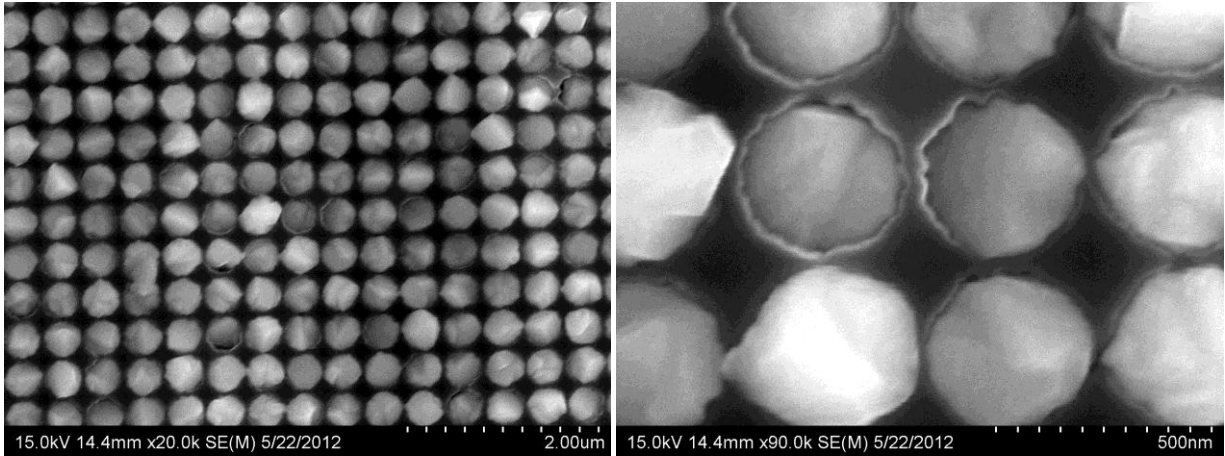


Figure 13. SEM images of CdS patterned sample 300nm feature size taken at 20.0k (left) and 90.0k magnification (right).

### 3.3 Cadmium Telluride growth

A CSS reactor shown in Figure 14 was used to deposit CdTe on each of the samples. The apparatus consists of two graphite plates that hold the substrate (top) and source (bottom), which are separated by 1.1 mm thick glass spacers. The source material is a 1.5"x1.5"x0.1" CdTe single crystal.

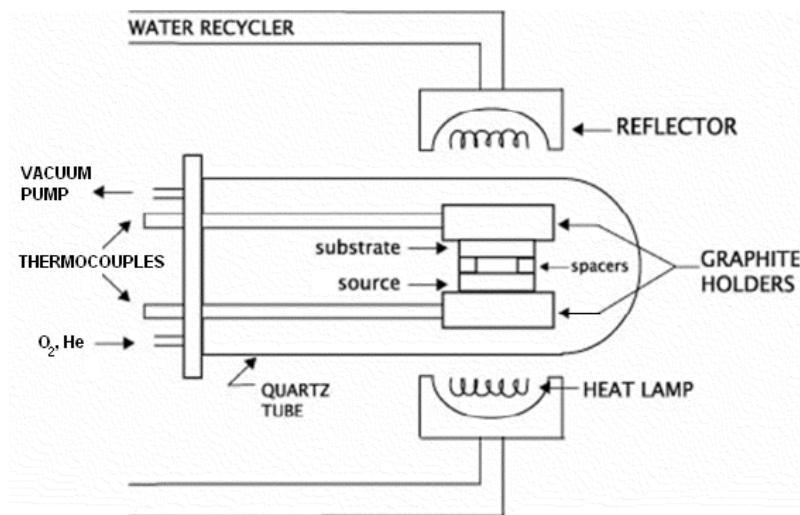


Figure 14. CSS reactor apparatus. [20]

During deposition, a source temperature of 550 °C is used, while the substrate temperature is kept at 500 °C for 700 seconds in a He atmosphere. As a result, CdTe is selectively deposited on the CdS through micrometer sized holes as depicted by Figure 15.

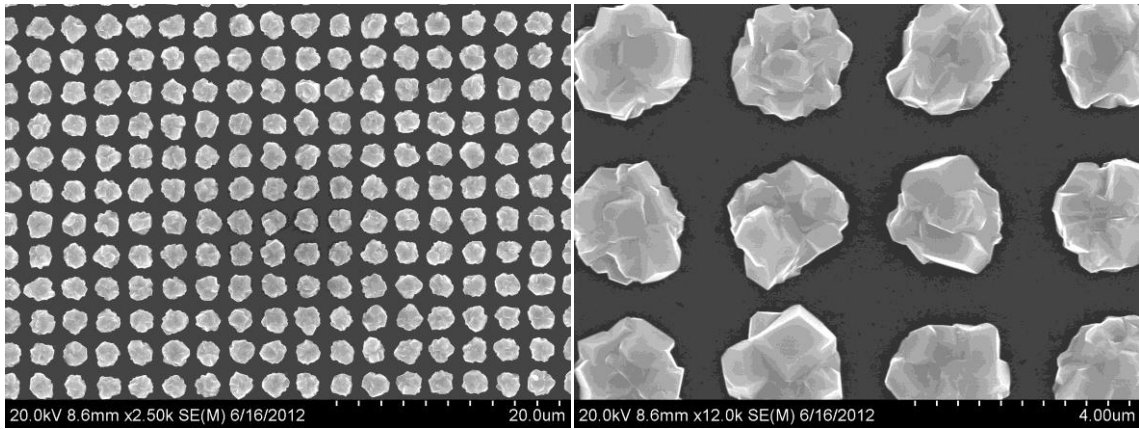


Figure 15. SEM images of CdTe selectively deposited on patterned sample of 1.5 $\mu$ m feature size, taken at 2.50k (left) and 12.0k magnification (right).

## **CHAPTER 4: NANOPROBING METHODOLOGY**

### **4.1 Benefits of micro and nano I-V testing**

One of the objectives of this work is to characterize the I-V response of isolated CdTe grains. As mentioned earlier, electrical characterization of individual grains will give insight of the benefits of using patterned templates for fabrication of thin-film solar cells. By having template windows and achieving selective growth of CdTe it is possible to obtain the I-V response of individual CdTe grains on a substrate.

Additionally, the different feature sizes of the windows enable study of the effect of the grain size on the I-V characteristics. Moreover, the use of additional characterization techniques, such as transmission electron microscopy (TEM) and atomic force microscopy (AFM) can be used to associate electrical characterization to crystal growth and microstructure of the grains.

### **4.2 Nano-probing in other applications**

There are various applications in which nano-probe systems are utilized. The nano-probing technique has been used on characterization of carbon-nano tubes, MOS-Capacitors, SRAM transistors and conductive ink. In the case of carbon-nano tubes, a nano-probing system is used to move nano-particles and to setup electric contacts for nanostructured materials fabrication as shown in Figure 16. [24]

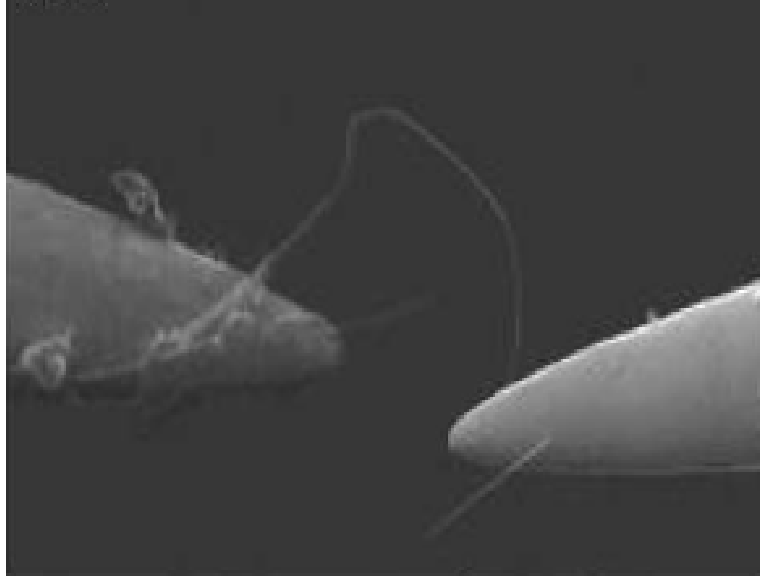


Figure 16. Panoramic image of fabricating carbon nanotube transistor via nano-probes. [24]

Failure analysis labs have used these probing systems to isolate individual field-effect transistors and to evaluate bit cell errors caused by interface trapped charges and doping related issues through C-V measurements (Figure 17). [25] These individual transistors and logic devices are nano-probed with SEM based nano-prober systems mostly outfitted with four probes. [26]

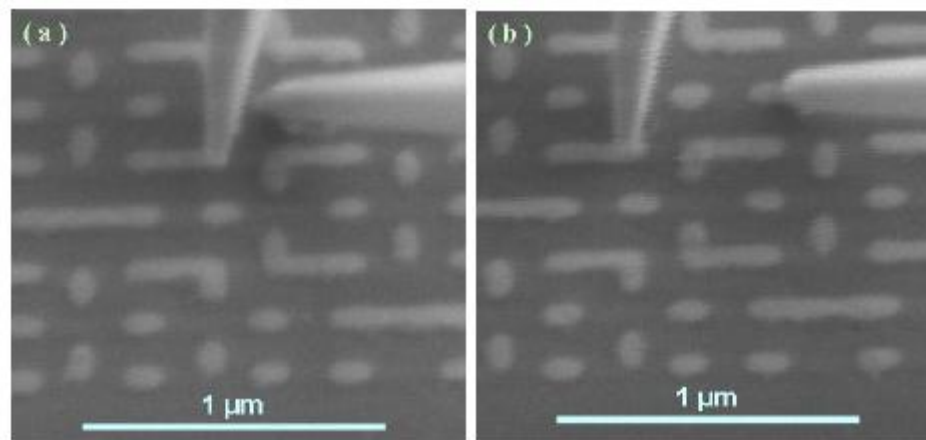


Figure 17. Probes touching down on the contacts for C-V measurement. (a) PMOS and (b) NMOS SRAM [25].

Nano-probe systems have also been used to measure the resistance of conductive inks as illustrated by Figure 18. This conductive ink is used in the manufacturing of printable electronics which have attractive applications such as; smart medical packages, barcodes to track merchandise, toys, and credit cards among others. [27]

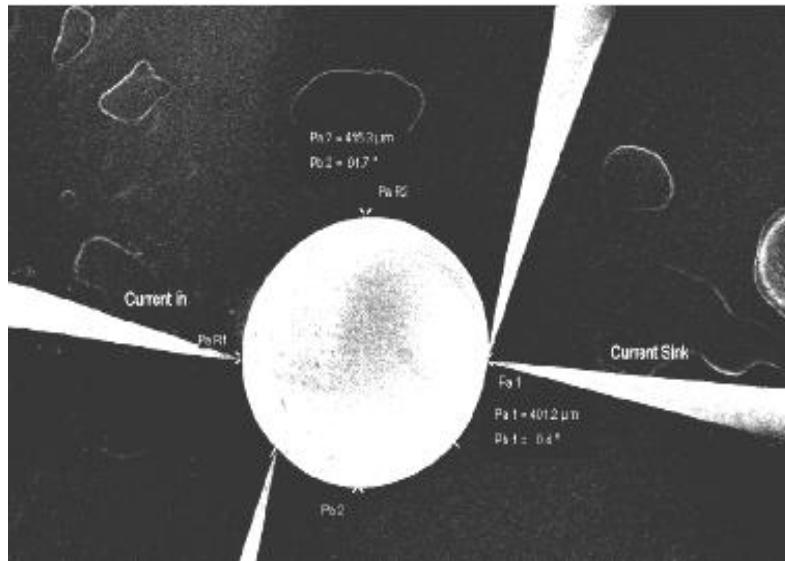


Figure 18. Image of four probes touching for resistance measurement on 400 μm In/Cu/Ag alloy solder ball. [27]

### 4.3 Nano-probing Equipment

A Zyvex S100 Nano-manipulator System is a tool for positioning and testing for micro and nano-scale research and development applications. [28] It consists of a controller as shown in Figure 19, and a piezo-actuated manipulator capable of vacuum and air-operation (Figure 20). The S100 is outfitted with two tungsten nano-effector probes with 45 degree bend and a tip diameter of 50 nm (Figure 21).

In this work, the Zyvex S100 was used in conjunction with a Hitachi 4800 SEM. The SEM served the dual purposes of imaging the sample and probes during probe steering and landing, and for stimulating the solar cell with an electron-beam during I-V measurement.

A scanning electron microscope (SEM) projects images of larger areas of the sample in real-time so the user can quickly find the region of interest. [29] For the purposes of this work, the SEM electron-beam, was utilized instead a light source in order to study the behavior of the device.



Figure 19. Zyvex S100 Controller.

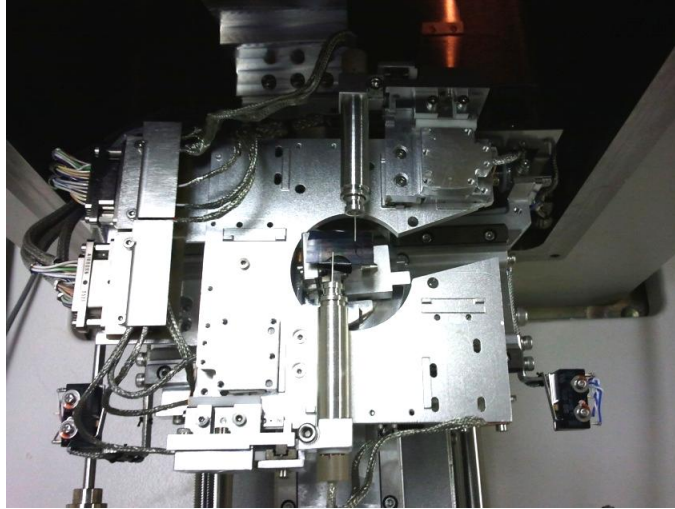


Figure 20. S100 unit with nano-probes installed



Figure 21. Nano-probe used in experimentation.

#### 4.4 Nano-probing Technique

Nanoprobining consists of two major steps, manipulating the probes over the samples and landing them on the surface to make electrical contact. Figure 22 shows a schematic of a prepared sample being tested and how both of the nano-probes are landed on the sample before performing the I-V test. It is necessary to have an area on the side of the solar cell to connect to the ITO layer. This requires that the CdS at the edge of the sample be etched with HCl to expose

the ITO. Once the ITO is exposed, solder is attached to the etched area using an ultrasonic soldering machine to ensure a good contact between the negative nano-probe and the ITO.

The next step of nano-probing technique is to identify the patterned areas to be contacted by the probes. This is done by using a low magnification view in the SEM and driving the positioners to the regions of interest. Figure 23 shows an image of the nano-probes positioned above the areas of interest.

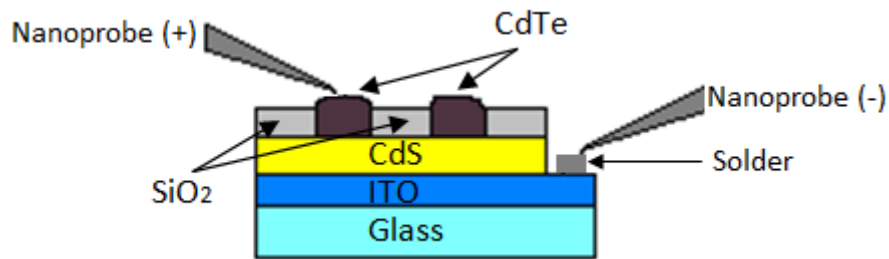


Figure 22. Schematic of nano-probes contacting a sample under test.

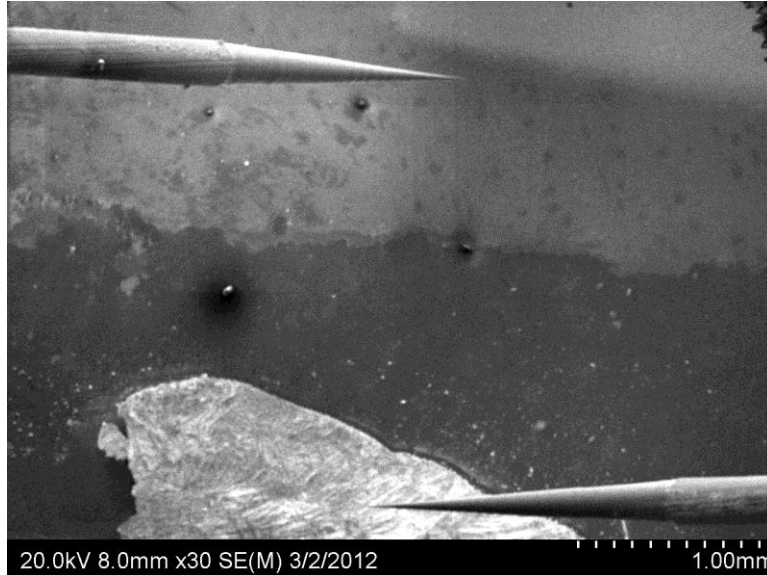


Figure 23. SEM low magnification image of nano-probes above areas of contact: CdTe (top) and solder (bottom).

Landing the nano-probes is quite challenging and requires practice and skill. In some cases the nano-probes can be damaged due to hard landings onto the substrate. Figure 24

shows probes that were bent due to hard landing. The difficulty in landing increases with reduced patterning size to the nanoscale. In addition to damaging the probes, the CdTe grains and sample can also be damaged by the probe. Figure 25 shows that the probe moved out of place causing damage to the grain after the voltage was applied. Moreover, residue from the CdTe grains can contaminate the nano-probe. To overcome these issues, practice and training is necessary to develop the landing technique.

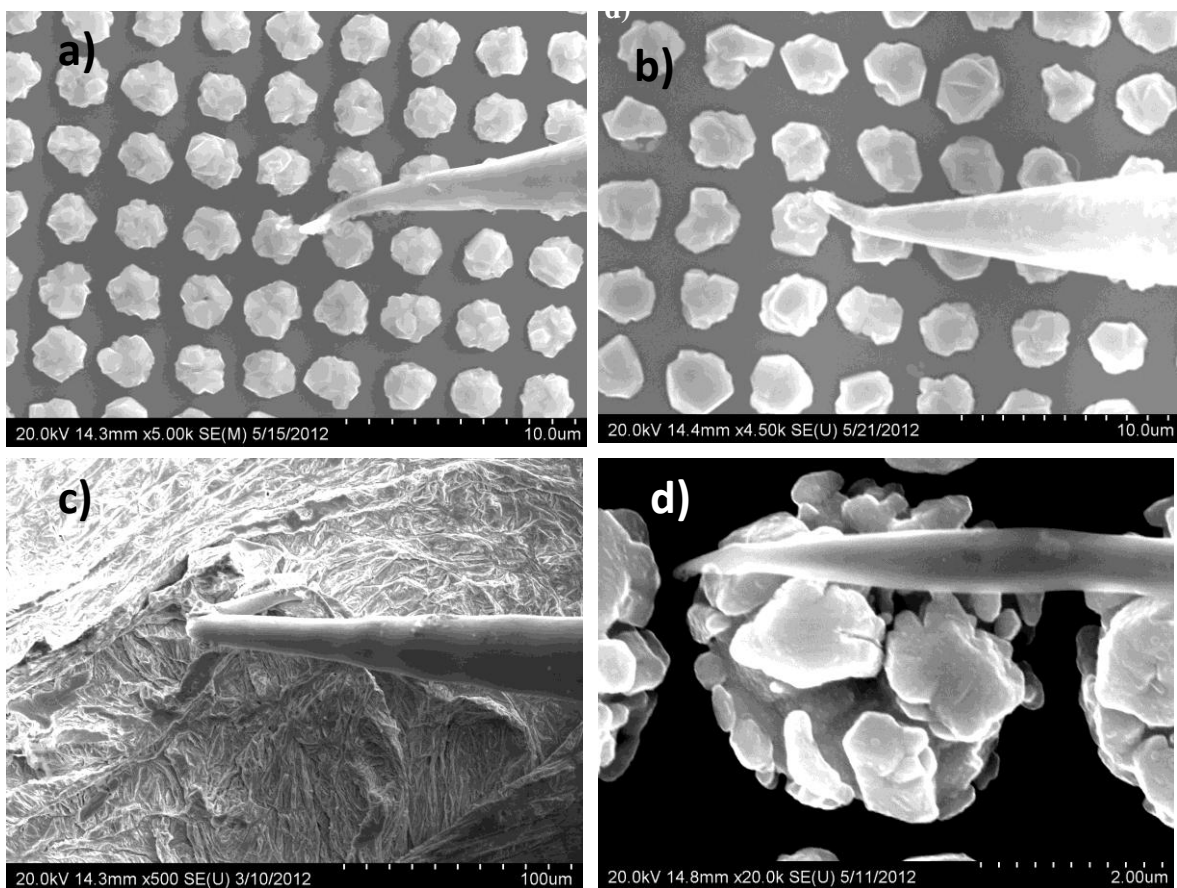


Figure 24. Failure landing of nano-probes on a) and b) CdTe grains, c) Solder drop and d) ZnTe/CdTe grain.

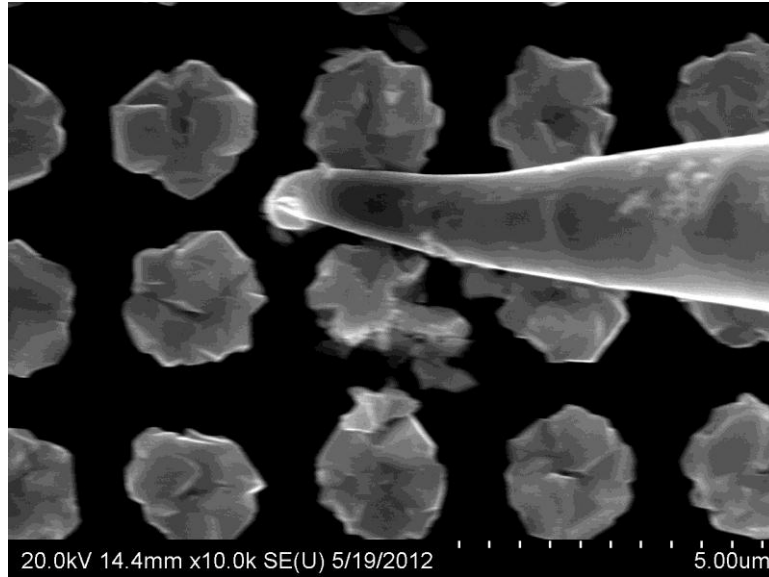


Figure 25. CdTe grain damaged by nano-probe.

After landing and contacting the nanoprobes, the next phase is to stimulate the solar cell to create electron-hole pairs with either light or energetic electrons, and to measure the I-V response through the nanoprobes. For the case of electron-beam stimulation, the SEM working conditions were set to focus (instead of raster) the electron beam on the CdTe grain being probed. The accelerating voltage and condition of the condenser lenses were set to different values depending on the various experiments being performed.

A Keithley 2400 source-meter and software that manage the components were used to conduct the I-V testing. The source-meter shown in Figure 26 combines a precise, low noise DC power supply with a low-noise, high impedance multimeter. [30]

The K-2400 model is capable of measuring a voltage from 1 $\mu$ m to 211 V, and a current from 10 pA to 1.055 A. The voltage measurement accuracy is 10 mV and 570  $\mu$ A for current accuracy measurements.

The software used is directly interfaced to the Keithley 2400. This software captures the I-V curve response from the device being tested. The accuracy of the measurements is also

measured in power line cycles (PLC), where the fastest speed setting (0.01 PLC) results in increased noise and less digits in the reading. Using 10.0 PLC provides the best noise rejection but, results in a slowest speed measurement. Usually, the software is adjusted to work at 1.0 PLC, 10 ms of voltage setting time and provides a graph composed of 100 plotted points, which results in a step time of 1 second.



Figure 26. Front panel of K-2400 Source-meter.

## **CHAPTER 5: RESULTS OF NANOPROBE I-V TESTING**

This chapter presents for the first time the electrical characterization of patterned solar cells using a nano-probing system. The procedures and results for measuring the electron-beam current are presented. The effect of varying important SEM parameters on the I-V response of the patterned cells is also presented. Moreover, I-V characterizations of arrays of CdTe grains with and without back-contacts having feature sizes of 2, 1.5, 1  $\mu\text{m}$  and 300 nm are shown.

### **5.1 Measurement of electron beam current**

An SEM has two parameters that modify the amount of current projected by the e-beam, the accelerating voltage and the condition of the condenser lenses. The accelerating voltage is the velocity of the electrons; while the condition of the condenser lenses controls the diameter of the e-beam. Experiments were performed to observe the effect of both parameters on the amount of current impinging the samples and to observe effect on the I-V response of the micrometer sized solar cells.

The SEM beam current was measured using a Faraday cup and pico-ammeter as shown in Figure 27(a) and Figure 27(b), respectively. A Faraday cup is a metal cup designed to catch charged particles. Using this device and with the help of a pico-ammeter it was possible to measure the amount of current coming from the e-beam. The measured current as a function of accelerating voltage and condition of the condenser lenses is shown in Table 2 and Figure 28. It is observed that by increasing the amount of accelerating voltage (and by decreasing the condition of the condenser lenses), the amount of the e-beam current increases. This is expected since the accelerating voltage determines the velocity of the electrons, while the condition of the condenser lenses determines the spot size of the e-beam.



Figure 27. (a) Faraday cup model and (b) Keithley 485 Picoammeter.

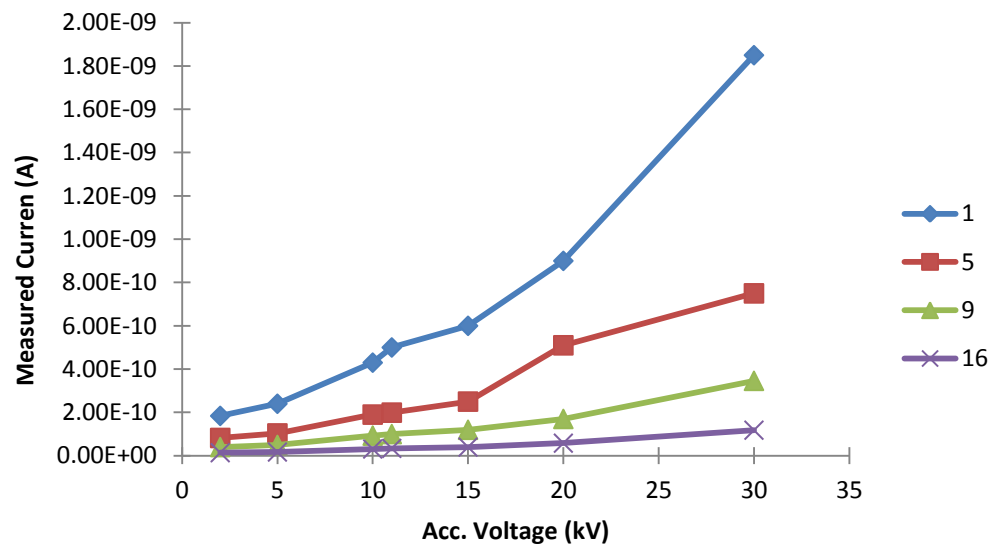


Figure 28. Measured e-beam current varying accelerating voltage and condenser lenses conditions.

Table 2. E-beam current measurements

Condenser Lenses conditions								
Acc. Voltage (kV)	1	3	5	7	9	11	13	16
30	1.85E-09	1.14E-09	7.50E-10	4.96E-10	3.46E-10	2.50E-10	1.82E-10	1.18E-10
20	9.00E-10	5.60E-10	5.10E-10	2.40E-10	1.70E-10	1.20E-10	9.00E-11	5.80E-11
15	6.00E-10	3.70E-10	2.50E-10	1.70E-10	1.20E-10	8.70E-11	6.30E-11	4.00E-11
11	5.00E-10	3.10E-10	1.99E-10	1.39E-10	1.00E-10	7.30E-11	5.30E-11	3.40E-11
10	4.30E-10	2.70E-10	1.90E-10	1.30E-10	9.30E-11	6.70E-11	4.70E-11	3.10E-11
5	2.40E-10	1.55E-10	1.03E-10	7.00E-11	5.00E-11	3.80E-11	2.60E-11	1.70E-11
2	1.84E-10	1.23E-10	8.20E-11	5.80E-11	4.00E-11	3.00E-11	2.20E-11	1.40E-11

## 5.2 Effect of SEM conditions on I-V response

Experiments were performed to observe the effect of the electron beam on the I-V response of the actual micrometer solar cells. In particular, the accelerating voltage and condition of the condenser lenses were varied and the response of the solar cells was observed. Figure 29 shows a cross section image of a typical micro-patterned solar cell used for this set of experiments.

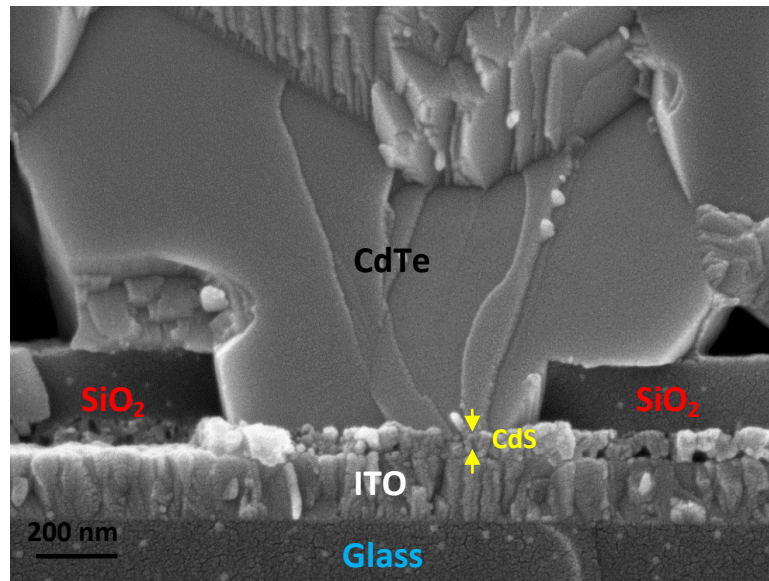


Figure 29. SEM cross section image of CdTe grain grown on patterned substrate.

One set of experiments focused on studying the effect of the accelerating voltage while keeping all the other parameters constant. The patterning size of the CdTe grains was 2.0 microns. The condition of the condenser lenses was kept constant at 5. In one experiment, the accelerating voltage was sequentially set to 10 kV, 20 kV and 30 kV. Figure 30 shows the measured I-V characteristic of the solar cell and shows that by increasing the accelerating voltage, the Voc increased. Interestingly, the Voc's were much greater than the band gap of CdTe (1.5 eV).

In order to study the effect on the Voc further, a second experiment was performed in which the accelerating voltage was sequentially set to 20 kV, 30 kV and back to 20 kV. The I-V response from this experiment is depicted in Figure 31. In this experiment the Voc did not track the accelerating voltage as clearly as in the previous experiment. Initially, the Voc increased with accelerating voltage (from 20 kV to 30 kV) but then remained high when the accelerating voltage was decreased from 30 kV to 20 kV. Another thing to note in this data is that the short-circuit current was less compared to the previous. One possible explanation for this is that the contact to the cell was not as good. Another hypothesis is that when the voltage is increased, the charge in the sample is also increased, leaving the sample electrically charged.

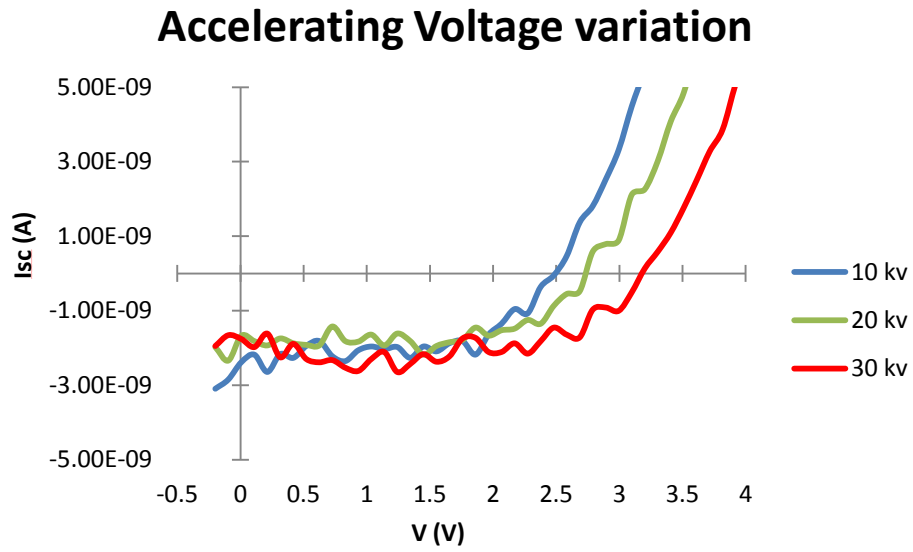


Figure 30. I-V curve obtained by varying the accelerating voltage in a sample.

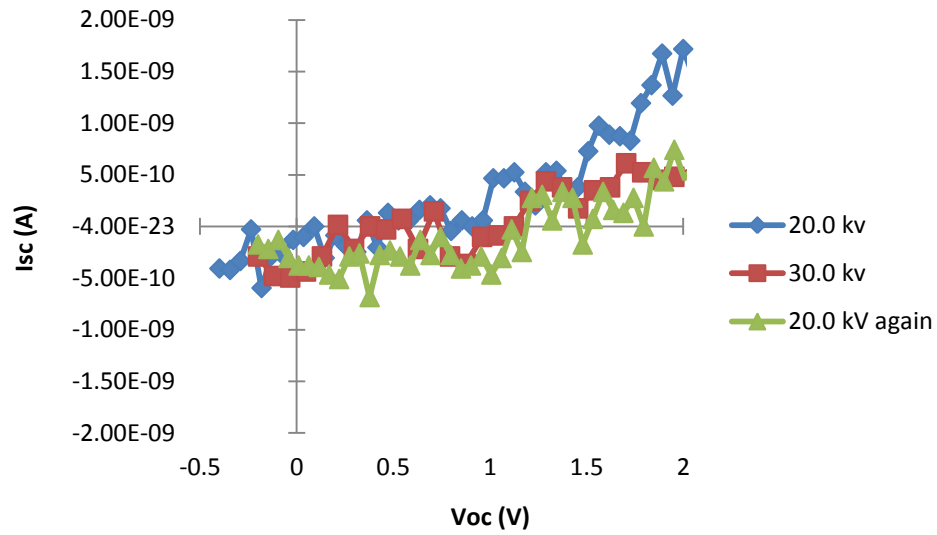


Figure 31. Effect of accelerating voltage in sample.

Another experiment focused on studying the effect of the condition of the condenser lenses while keeping all the other parameters constant. The patterning size of the CdTe grains was 2.0 microns. The accelerating voltage was kept constant at 20 kV. Before analyzing the results it is important to remember that a smaller number on the condition of the condenser

lenses gives a higher current and smaller spot size as shown in Figure 28. Figure 32 shows the I-V response and indeed, the short-circuit current and  $V_{oc}$  increased with smaller number of condition.

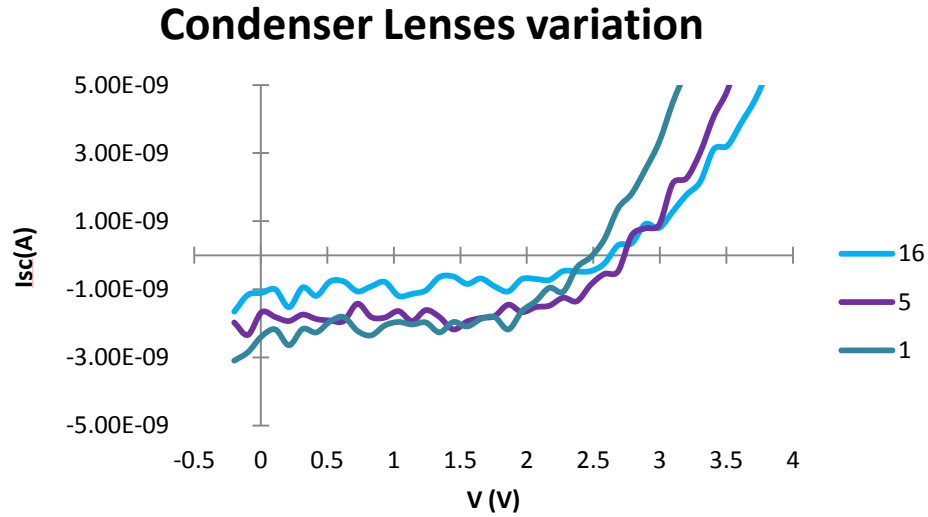


Figure 32. I-V curve obtained by varying the condenser lenses conditions in a sample.

One experiment tested the difference in the I-V response when the e-beam was on compared to off. It is observed in Figure 33 that the characteristic obtained when the e-beam is off is similar to a diode I-V curve in the dark. In contrast, a distinct short-circuit current is observed when the e-beam is on.

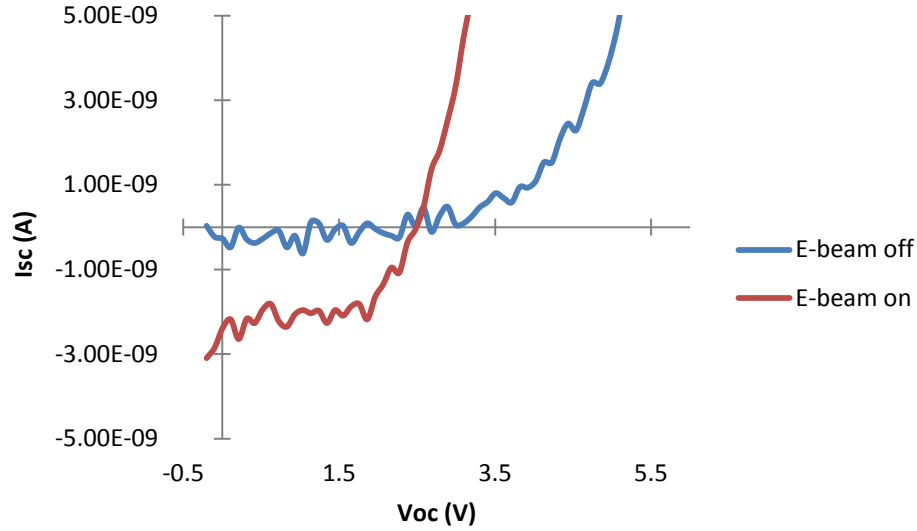


Figure 33. I-V measurement in the dark compared with e-beam on.

### 5.3 I-V response of micro and nano-patterned arrays

In this section, the I-V responses of solar cell arrays of 2.0, 1.5, 1.0 and 0.3 micro-meter size are presented. The work of Galloway predicts that an accelerating voltage of 20 kV and an electron-beam current of 0.5 nA gives an electron-hole pair generation rate similar to Air Mass 1.5. [31] Therefore, for all the measurements in this section the SEM accelerating voltage was set to 20 kV and the condition of the condenser lenses was set to 5 so that approximately 0.5 nA electron beam current was achieved for stimulation. For each case, an SEM image of the grains is shown followed by the I-V responses of the grains.

#### 5.3.1 2 $\mu\text{m}$ feature size results

Figure 34 shows an SEM image of the four, 2  $\mu\text{m}$  sized CdTe grains that were tested. A nano-probe is shown landed on grain number 3. The voltage bias was varied from -0.2 to 8.0 V. The I-V characteristics of the four grains are shown in Figure 35.

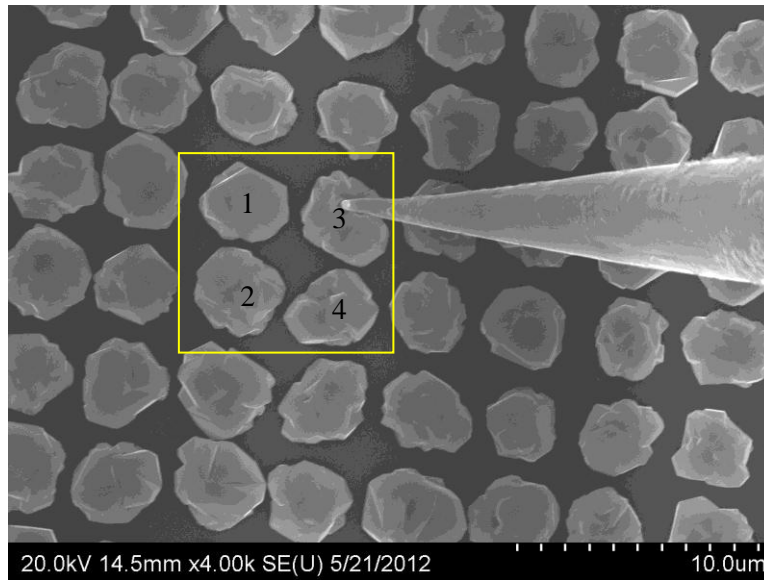


Figure 34. SEM top view image of nano-probe measuring an array of 4 grains of 2 $\mu$ m size.

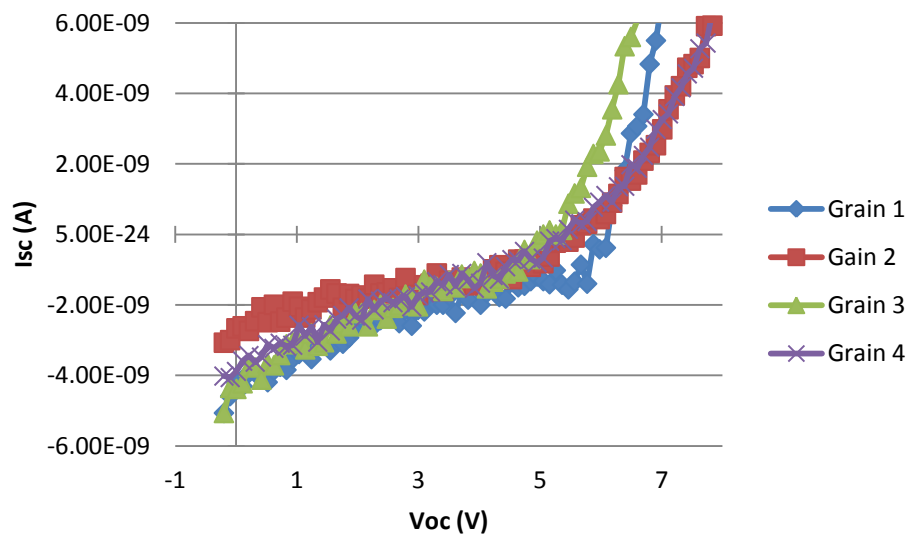


Figure 35. I-V response for grains measured in Figure 34.

### 5.3.2 1.5 $\mu\text{m}$ feature size results

A similar test was performed on a sample of 1.5  $\mu\text{m}$  feature size as depicted by Figure 36. This time the I-V test was performed using an array of six grains. The results obtained from this sample were very different from any expected I-V response. When a voltage bias of -0.2 V to 2.0V was used to collect the current-voltage data, no I-V curve was obtained. However, by increasing the amount of bias to -0.2V to 8V, a graph finally could be obtained for all the grains as shown in Figure 37 and Figure 38.

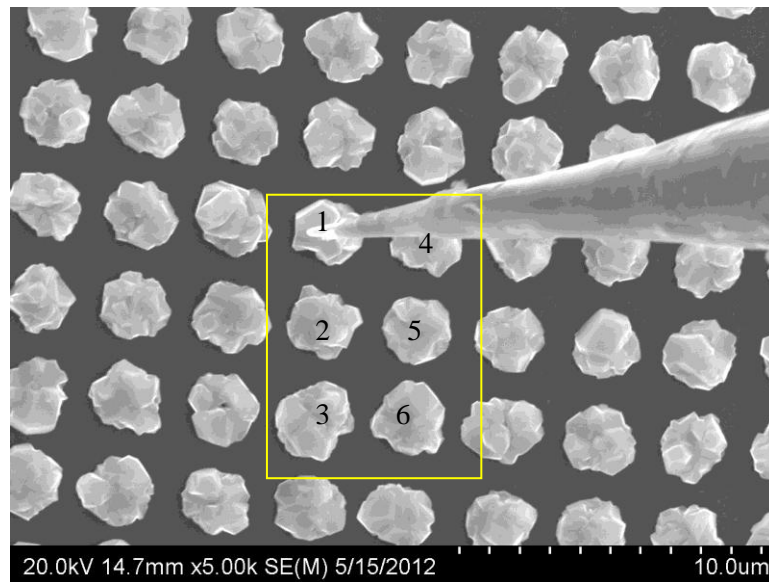


Figure 36. SEM top view of nano-probe measuring an array of six 1.5  $\mu\text{m}$ . feat. size CdTe grains.

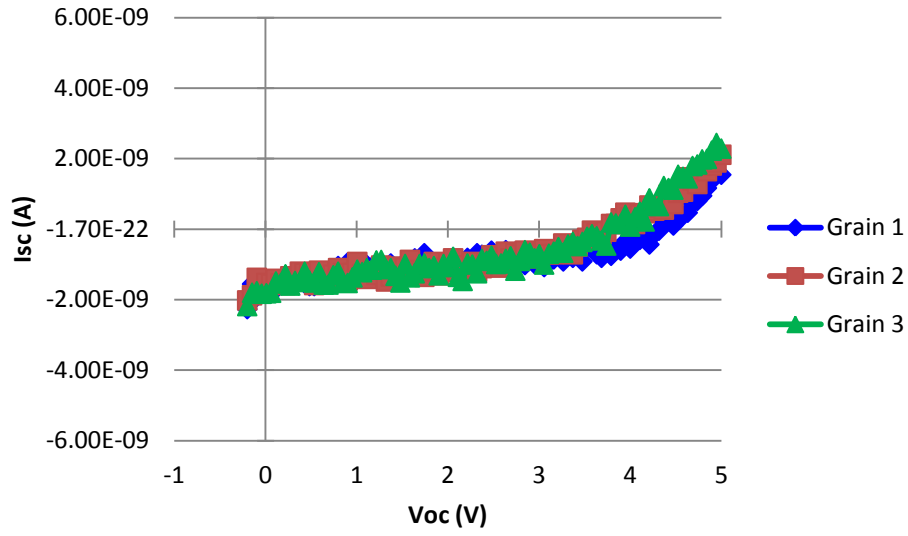


Figure 37. I-V response from Grains 1, 2 and 3 from Figure 36.

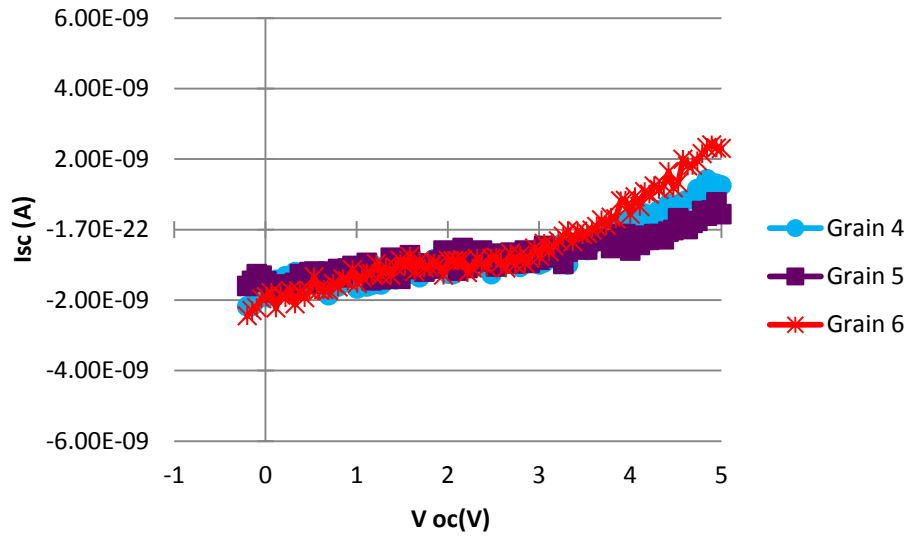


Figure 38. I-V response from Grains 4, 5 and 6 from Figure 36.

### 5.3.3 1 $\mu\text{m}$ feature size results

The next sample tested was a 1 $\mu\text{m}$  patterned feature size. As it is shown in Figure 40, grain-1 presented an open circuit voltage of 278 mV and a short circuit current of 3.61e-10 A,

while grain-2 showed a Voc of 849 mV and a Isc of 7.81e-10 A. These results were obtained by using a voltage bias from -0.2 V to 5.0V.

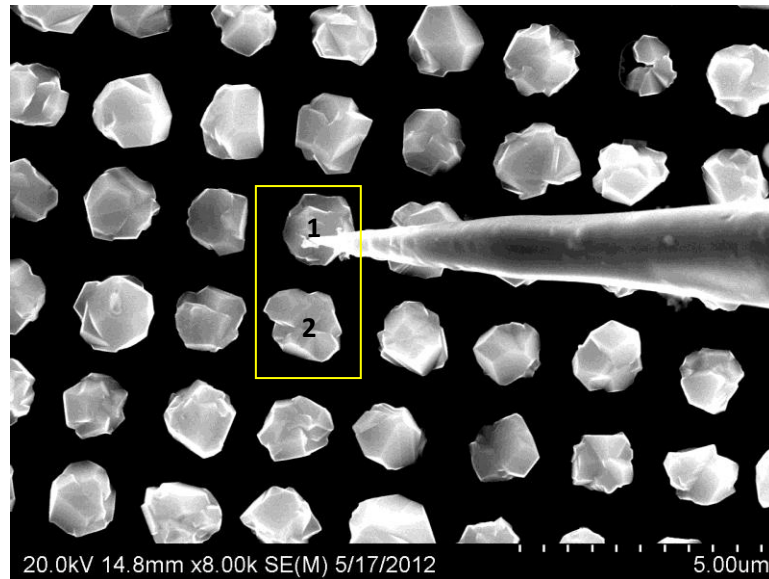


Figure 39. SEM top view of nano-probe measuring two adjacent 1  $\mu\text{m}$ . feat. size CdTe grains.

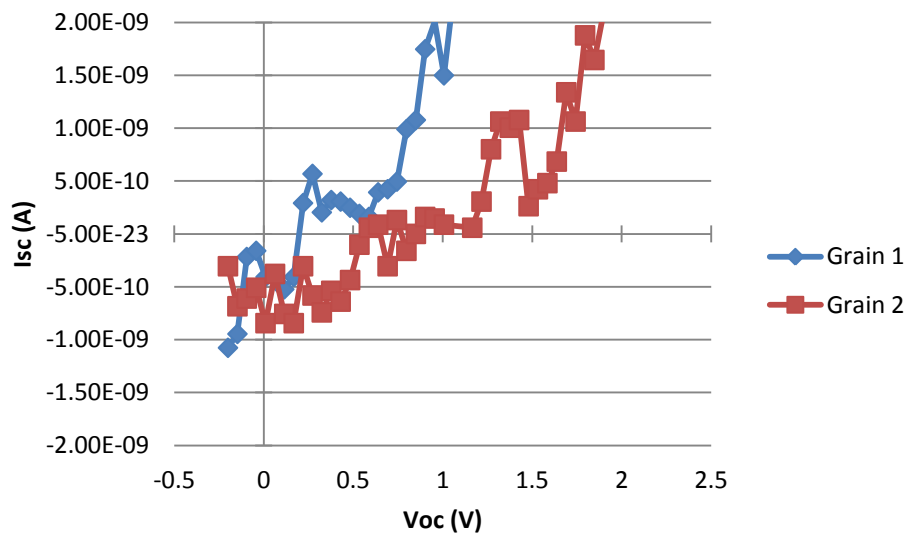


Figure 40. I-V measurement obtained from two different CdTe grains.

#### 5.3.4 300 nm feature size results

Figure 41 shows an SEM image of 300 nm CdTe grains. The yellow box in the image shows an array of 4 grains was selected for current-voltage testing. The voltage bias applied to this sample was of -0.2 V to 5.0 V. The I-V characteristics of the four grains are shown in Figure 42.

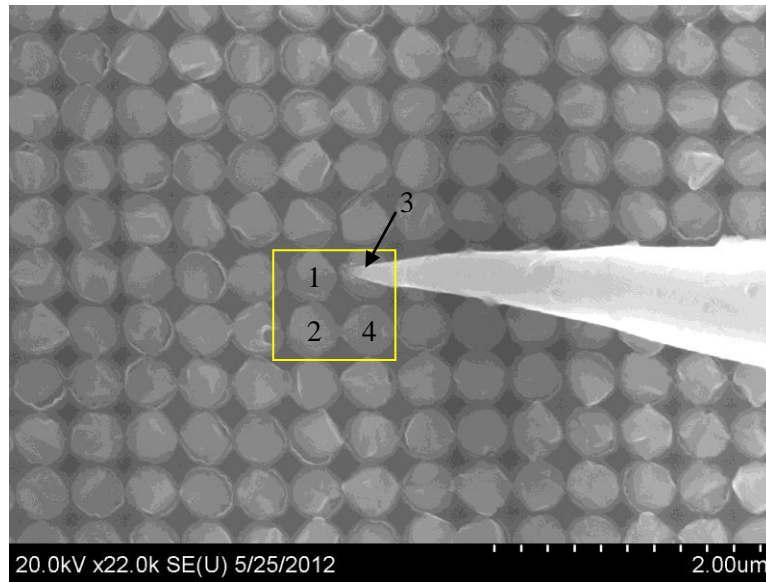


Figure 41. SEM top view of 300 nm. feature size sample. Nano-probe measuring array of four grains.

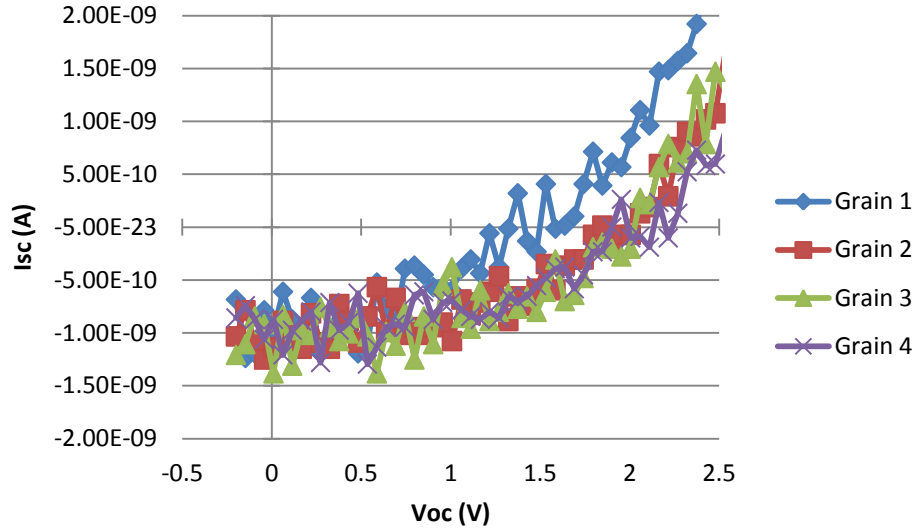


Figure 42. I-V response of grains marked in Figure 41.

Two important observations from the I-V results are; the large degree of noise in the data and high Voc's observed. In order to address the large amount of noise, two back-contact were tested and are discussed in the following section. Plausible reasons for the high Voc's are treated in the next Chapter.

## 5.4 I-V response of cells with ZnTe and Cu back-contacts

### 5.4.1 I-V response of ZnTe back-contacted cells

According to previous researchers an intermediate layer of zinc telluride (ZnTe) produces a low-resistive CdTe contact. [14] Thus, in order to mitigate problems related with noise in the signal and to obtain better data, ZnTe was selectively deposited on the substrate by close spaced sublimation technique as shown in Figure 43. As it can be appreciated from Figure 44 the deposition of ZnTe did not result in such improvement as it was expected. However, the values of Voc were .907 and 1.79 V and the Isc was 1.21 e-10 and 3.64e-10 for Grain 1 and 2

respectively. It was at this time that it was decided to experiment with copper for the back contact.

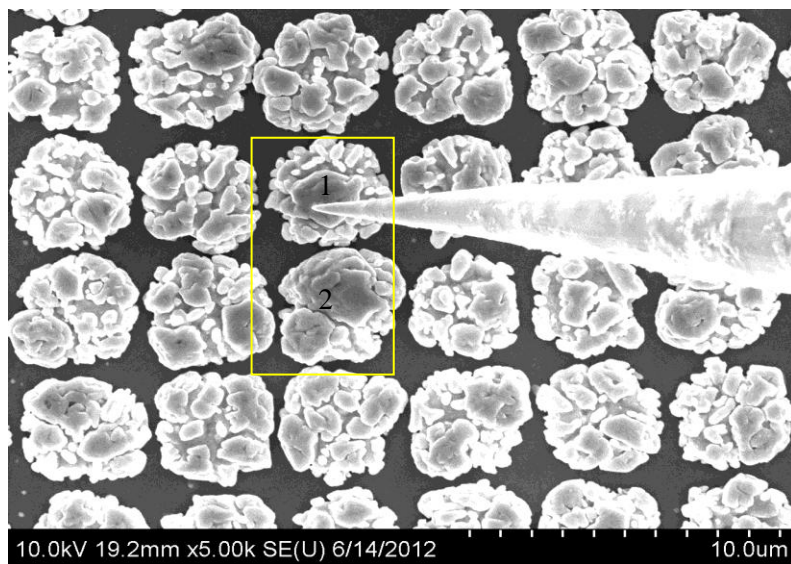


Figure 43. SEM image of nano-probe contacting grains from sample with ZnTe on CdTe.

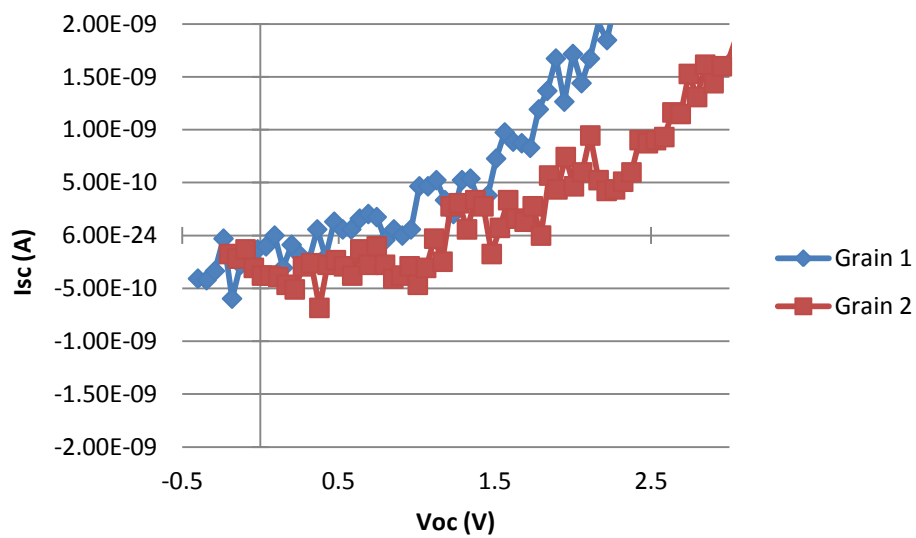


Figure 44. I-V response of grains measured in Figure 43.

#### 5.4.2 I-V response of Cu back-contacted cells

It is well known that copper is one of the most common materials used in solar cells for creating back contacts. By using a method known as angle evaporation it was possible to selectively deposit a thin layer of copper on the mesas of CdTe without causing shorting or contacting adjacent grains. In order to do this, it was necessary to find an indicated angle that would prevent the formation of a uniform layer of copper in the surface as shown in Figure 45.

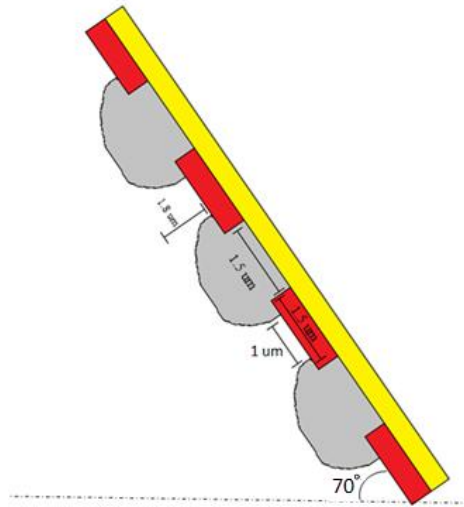


Figure 45. Schematic of sample setup for Cu angle evaporation deposition.

After the Cu deposition procedure, SEM characterization was performed on the sample in order to verify the expected results. Figure 46 c) and d) show the successful deposition of copper in the desired areas. The areas that appear like shadows in d) belonging to where copper wasn't deposited, while in the light regions on the  $\text{SiO}_2$  the presence of Cu is visible.

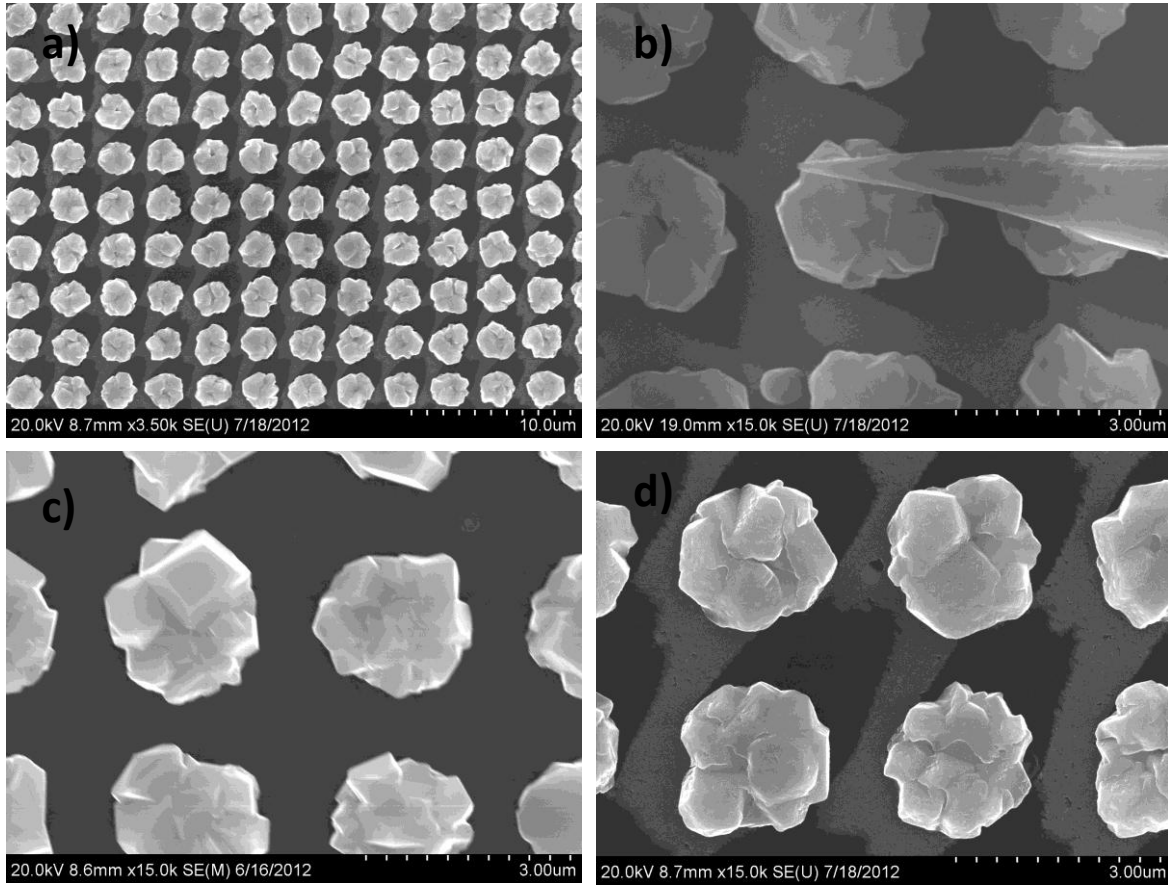


Figure 46. a) SEM image of CdTe array after Cu deposition, b) Nano-probing on CdTe grain where Cu is deposited. Comparison of: c) SEM image of sample before Cu was deposited and d) SEM image of same sample after Cu evaporation.

In order to correlate these statements, energy dispersive X-ray spectroscopy (EDAX) was performed in three particular regions of the sample as described by Figure 47 a). As we can see from figures 1 to 3, the presence of copper is different on each area. In Figure 47 (1) the presence of Cu is predominant on top of the CdTe grain.

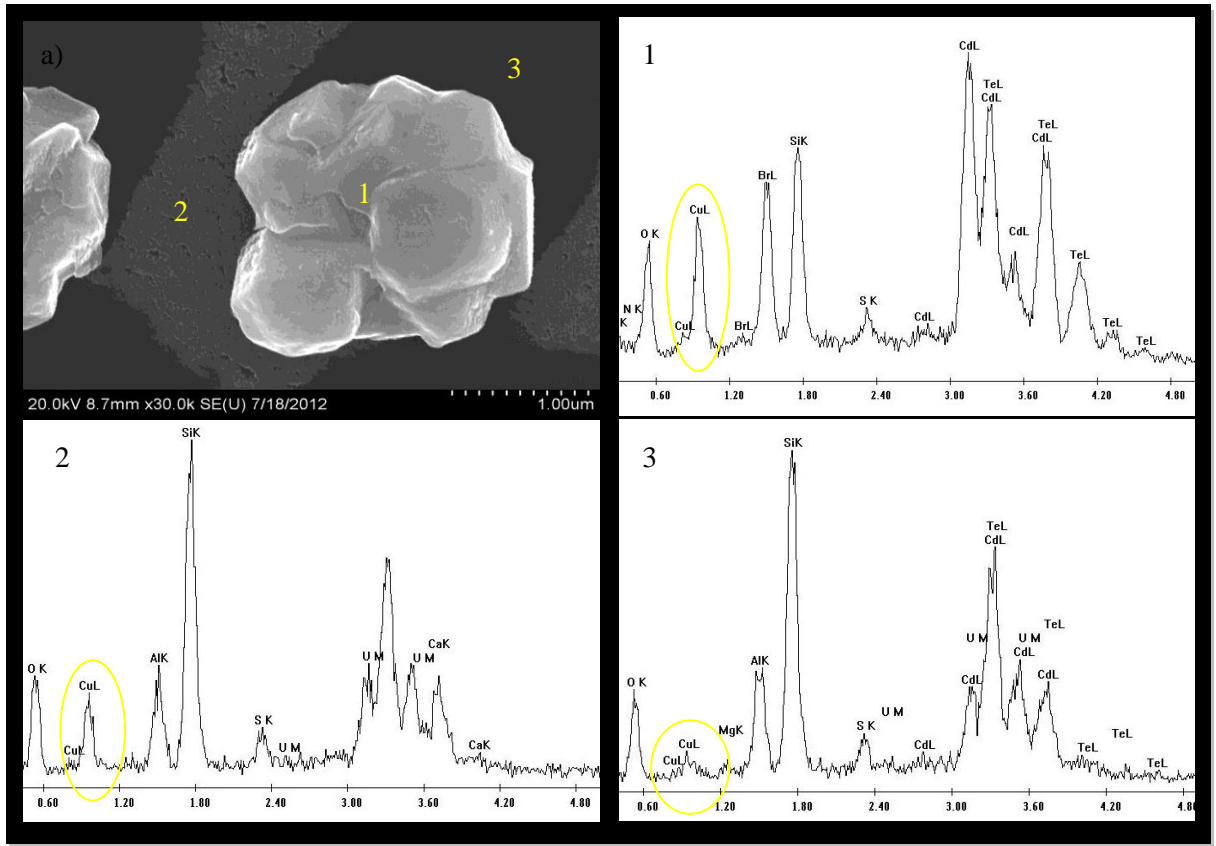


Figure 47. a) SEM image of substrate after Cu deposition. As it is shown, it is denoted with three different regions. 1) EDAX spectra run on top of CdTe grain 2) EDAX measurement on the SiO<sub>2</sub> region where Cu is present 3) EDAX spectra on region shadowed by CdTe grain, Cu is not deposited.

After the copper deposition was performed, a nano-probe test was performed in one of the grains as shown in Figure 46 b). The results of this test are displayed in the I-V curve of Figure 48. In difference from the rest of the I-V characteristics illustrated in this paper, the signal obtained from this particular sample showed a clear exponential response with negligible noise and a higher value in the short circuit current ( $V_{oc}=1.96$  V and  $I_{sc}=4.50e-8$ ). This demonstrates that the use of Cu in the back contact enhances the device performance.

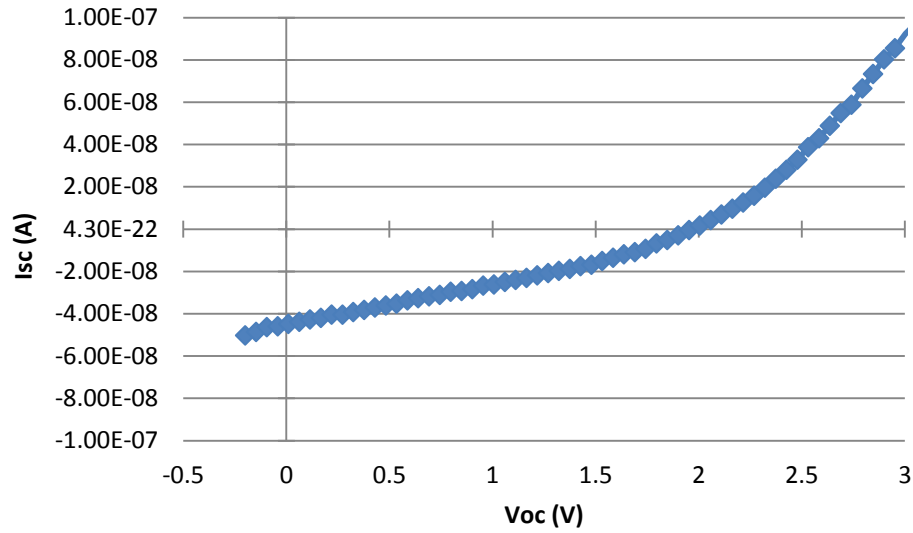


Figure 48. I-V response of CdTe grains using Cu as contact.

As a final observation, it can be appreciated from the experimental results in this Chapter that the open circuit voltage values obtained are very high for all of the tests. These values exceed the maximum theoretical value that CdTe solar cells can attain. In the following Chapters, a further explanation of this effect as well as some assumptions and calculations to find the reasons of this phenomenon are presented.

## CHAPTER 6: RELATIONSHIP BETWEEN OPEN CIRCUIT VOLTAGE AND BANDGAP

### 6.1 Background of Voc in CdTe solar cells

As stated in the introduction, CdTe is an excellent candidate for photovoltaic devices because of its optimal band gap for solar absorption ( $\sim 1.5$  eV) and theoretical efficiencies reaching 29%. Nevertheless, the largest efficiency reported is only 17.3%. One of the factors that has limited a further efficiency increase of these cells is the open circuit voltage ( $V_{oc}$ ). As we observed from Table 1, there has been an improvement through the years of short circuit current ( $J_{sc}$ ) relative to  $V_{oc}$ . Dominant factors that control the  $V_{oc}$  are; 1) the carrier concentration in CdTe ( $< 10^{15} \text{ cm}^{-3}$ ) and 2) minority carrier lifetime present ( $< 10$  ns.) as shown in Figure 49. [32] The status of current polycrystalline CdTe is shown in the Figure.

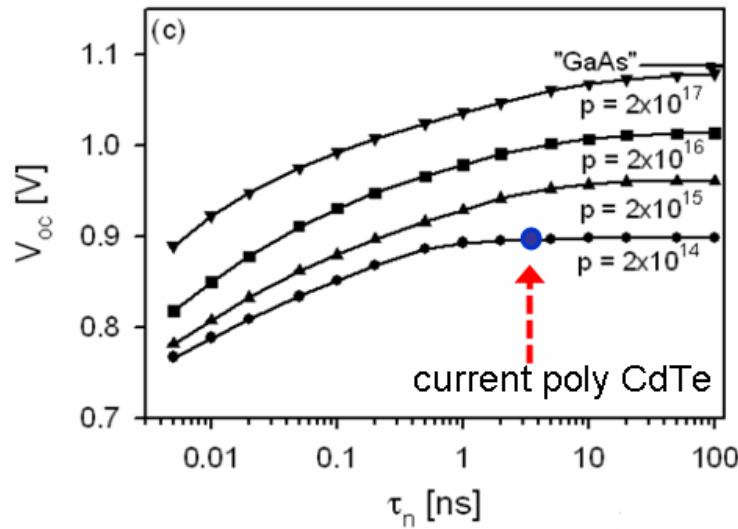


Figure 49. Graph showing  $V_{oc}$  vs. carrier lifetime. [32]

### 6.2 Voc as a function of Bandgap

The open-circuit voltage is the maximum voltage available from a solar cell, and this occurs when the current through the device is zero. The  $V_{oc}$  corresponds to the amount of

forward bias on the solar cell due to the bias of the solar cell junction with the light-generated current [33]. This is given by the expression,

$$V_{oc} = \frac{nkT}{q} \ln \left( \frac{I_L}{I_o} + 1 \right)$$

Equation 1. [33]

where  $I_L$  is the light generated current,  $I_o$  is the dark saturation current,  $n$  the ideality factor and  $kT/q$  is the thermal voltage. As it is shown by Equation 1,  $V_{oc}$  depends on the saturation current and light generated current.

Under normal conditions, the  $I_L$  usually has a small variation, thus the key variation to increase the  $V_{oc}$  is the diode saturation current.  $I_o$  depends on the recombination of the solar cell, which means, the more defects in a device, the higher  $I_o$ . So, looking at the Equation 1, in order to have a high value of  $V_{oc}$ , the value of  $I_o$  needs to be the smallest possible which in-turn requires the minimum number of defects. The principle of detailed balance can be used to determine the smallest values possible for  $I_o$  according to the next equation.

$$I_o = \frac{q}{k} \frac{15\sigma}{\pi^4} T^3 \int_u^\infty \frac{x^2}{e^x - 1} dx$$

Equation 2. [33]

where  $u$  is given by  $u = eg/kT$ . By solving the integral in Equation 2, the relationship between  $I_o$  and bandgap can be obtained and is plotted in Figure 50.

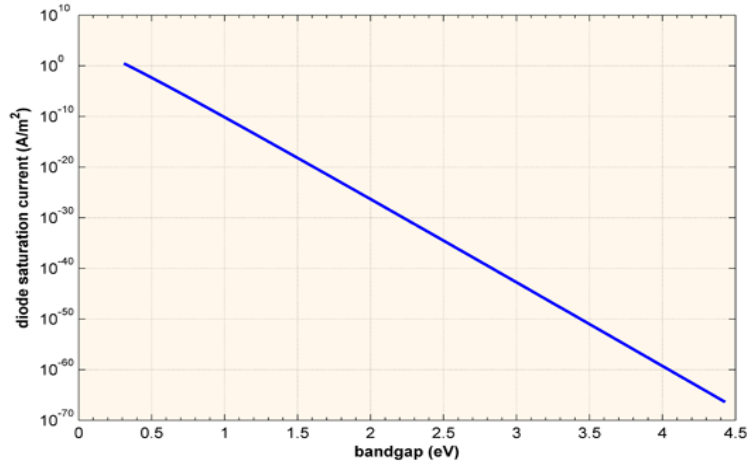


Figure 50. Diode saturation current vs. bandgap relationship. [33]

The relationship between  $V_{oc}$  and the energy band gap can be obtained by substituting  $I_o$  back into Equation 1. This relationship is graphically displayed in Figure 51. From this figure we are able to observe that a maximum possible  $V_{oc}$  value for CdTe solar cells (with a bandgap of 1.5 eV) is around 1V utilizing AM1.5. This thermodynamic analysis shows that under one sun at AM1.5, the  $V_{oc}$  will always be less than the energy band gap. This is important to note since several of the I-V measurements gave  $V_{oc}$ 's greater than the energy band gap.

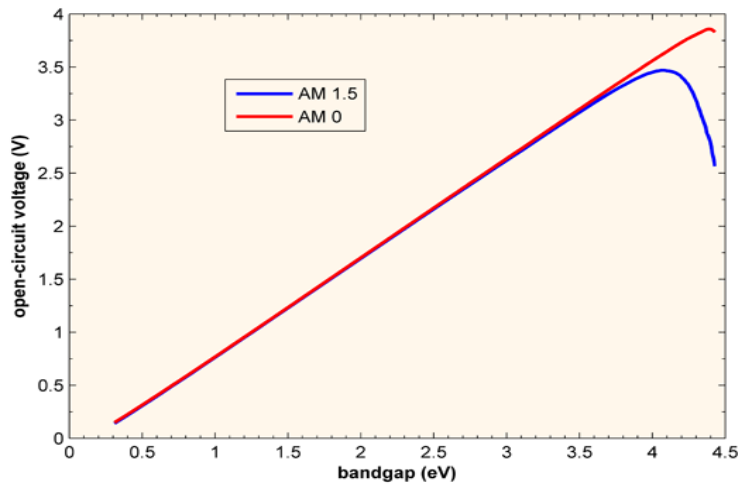


Figure 51.  $V_{oc}$  vs. bandgap relationship. [33]

Experimentally, researchers have shown a similar trend in the relationship between the  $V_{oc}$  and the band gap. For instance, Carmody [32] showed, (see Figure 52), the highest reported values of  $V_{oc}$  for different material systems. For all the material systems, the experimental  $V_{oc}$  was slightly below the  $V_{oc}$  based on thermodynamic analysis. Moreover, the CdTe cells showed the most deviation from the band gap compared to other photovoltaic materials. This alone can be taken as a motivation that further research is needed in this specific field. The difference between the  $V_{oc}$  and the energy band gap is called the “bandgap –  $V_{oc}$  offset”.

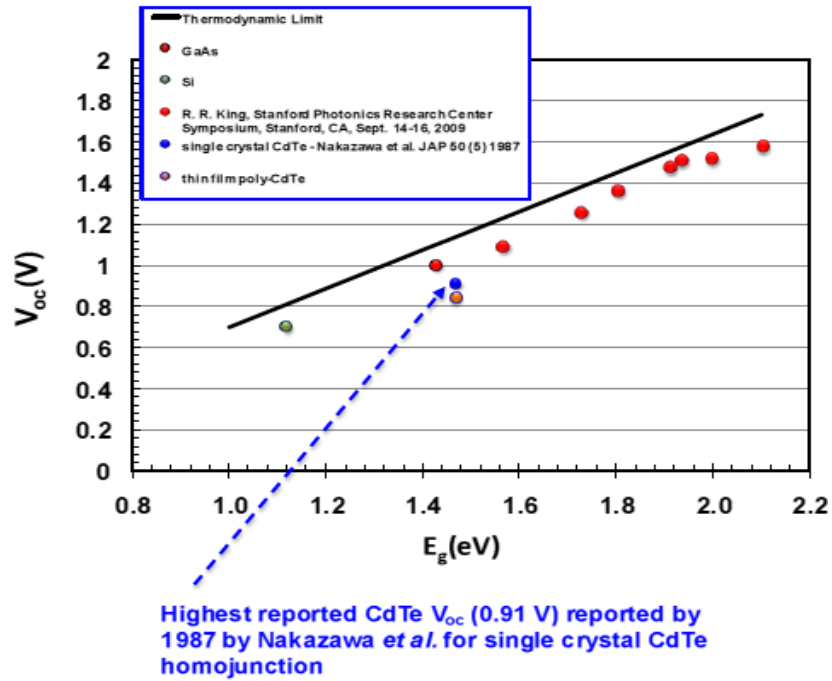


Figure 52.  $V_{oc}$  vs. bandgap relationship according to Carmody. [32]

### 6.3 Bandgap-voltage offset

Further work to determine the maximum  $V_{oc}$  a solar cell can obtain has been done utilizing bandgap-offset calculations, which also gives further explanations why the  $V_{oc}$  in a

semiconductor is limited. In this analysis, the equations for carrier concentration under thermal equilibrium (Equation 3)

$$n_i^2 = N_c N_v e^{-E_g/kT}$$

Equation 3. [34]

and non-equilibrium (Equation 4)

$$pn = n_i^2 e^{qV/kT}$$

Equation 4. [34]

are combined to give,

$$pn = N_c N_v e^{\frac{E_g - qV}{kT}} = N_c N_v e^{\frac{qW}{kT}}$$

Equation 5. [34]

Where  $W$  is the bandgap-voltage offset obtained from the difference between bandgap and voltage as mentioned above. This can also be written in the following manner,

$$W = \left( \frac{E_g}{q} \right) - V = \frac{kT}{q} \ln \left( \frac{N_c N_v}{pn} \right)$$

Equation 6. [34]

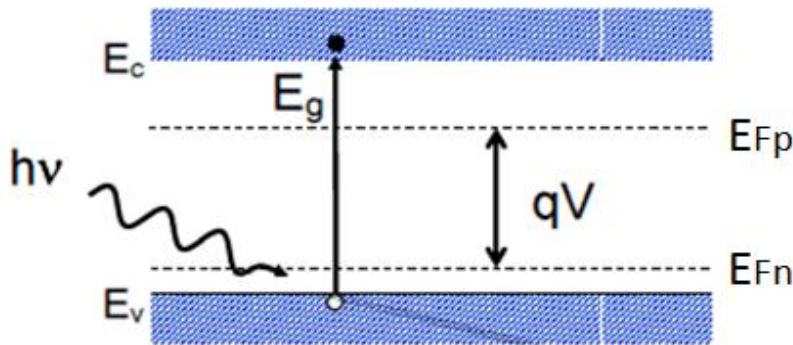


Figure 53. Schematic of possible maximum voltage in a semiconductor. [34]

King, explained that the maximum voltage available at the terminals of a semiconductor can be described by Figure 53. Using this relationship, the voltage in Equation 6 can be represented by quasi-Fermi levels shown in by Figure 53 and described by Equation 7.

$$qV = q(E_{FP} - E_{FN})$$

Equation 7. [34]

Thus, in order to increase the Voc in a semiconductor device, the concentration of holes and electrons need to be also increased (Equation 6). When the Voc is increased, the quasi-Fermi levels  $E_{FP}$  and  $E_{FN}$  get closer to the conduction band and valence band, respectively. The concentration of holes and electrons can be increased by increasing their respective lifetimes and increasing the electron-hole pair generation rate in the semiconductor.

In summary, this Chapter describes the direct relationship between the Voc and the bandgap value of a photovoltaic device. As it is explained, the maximum Voc that photovoltaic devices can reach is close to their bandgap. These explanations are based in the assumption that the solar cell is excited using 1 sun of illumination. In the next chapter a series of hypothesis and calculations are presented in order to explain the discrepancies that exist between the experimental values obtained and the theory presented in this chapter.

## CHAPTER 7: E-BEAM COLLISIONS IN CDTE SOLAR CELLS

### 7.1 Creation of electron-hole pairs via collision

The high-energy electrons from the SEM beam inject charge carriers into the semiconductor. Thus, beam electrons lose energy by promoting electrons from the valence band into the conduction band, leaving behind holes. Figure 54 represents an e-beam colliding with a CdTe crystal structure. Assuming that the e-beam collides either with a Cd or a Te particle, it is going to cause many collisions generating a lot of e-h pairs. In order to have a better understanding of these phenomena, a simulation software called CASINO was used.

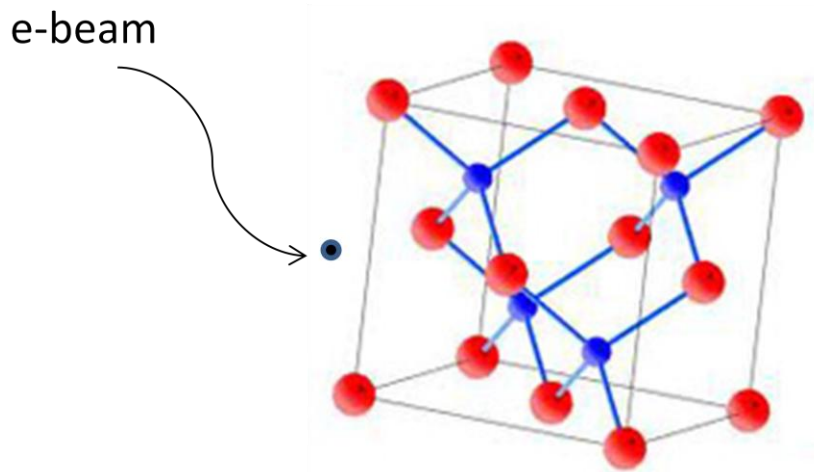


Figure 54. E-beam colliding with CdTe structure.

The CASINO acronym has been derived from the words "monte CARlo SIMulation of electroN trajectory in sOLids". This program is a Monte Carlo simulation of electron trajectory in solids and is specially designed for low beam interaction in a bulk and thin foil. [35] The main idea is to simulate enough electron trajectories to represent the condition used to image structures in an SEM.

Figure 55 is a Monte Carlo simulation that shows scattered electrons colliding in a CdTe structure. The electrons are represented by two colors; color yellow is when electrons are at high energies, while the blues ones are electrons with lower energy due loss through scattering. As we can appreciate from the picture, every time an e-beam collides it will lose energy and create e-h pairs. The small circles in the Figure indicate collisions.

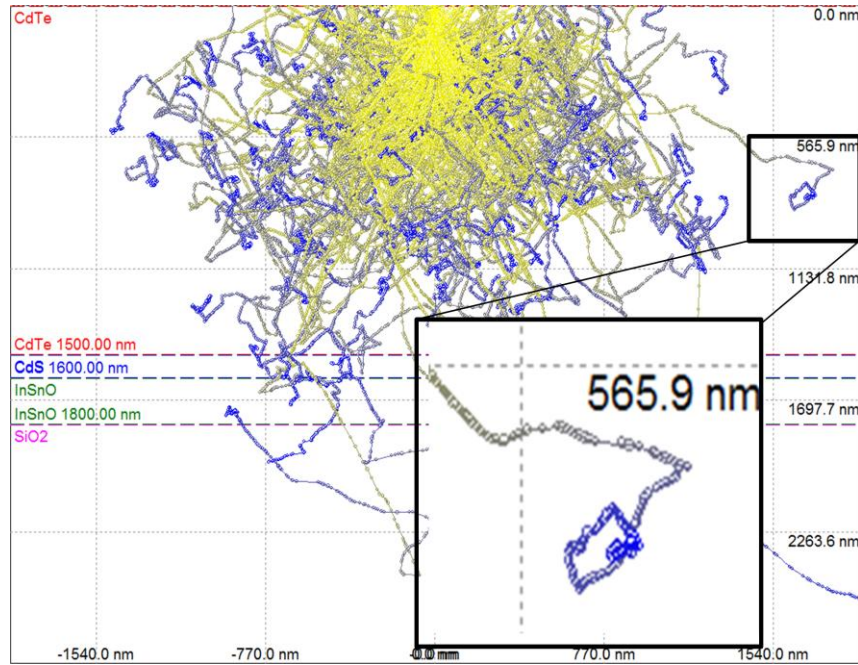


Figure 55. High energy electrons collision simulated in CASINO.

## 7.2 Electron-beam scattering in Nano-islands

A series of simulations were run in order to obtain the effect that the e-beam has on the Voc of patterned solar cells. First, a structure of the sample was designed in the program giving thickness specifications for every layer. For the nano-patterned sample the conditions for the CdTe thickness was 400 nm, 100 nm for CdS and 200 nm for the ITO layer. Secondly, the

simulation was run by setting up the value of accelerating voltage and number of electrons to be present. The accelerating voltages were 10.0, 15.0, 20.0 and 25.0 kV with 200 electrons.

From Figure 56 it is evident that the higher the accelerating voltage, the larger the volume and the deeper into the sample in which electrons will be scattered. This is important since optimally most of the electron-hole pair generation should occur near the depletion region of the solar cell.

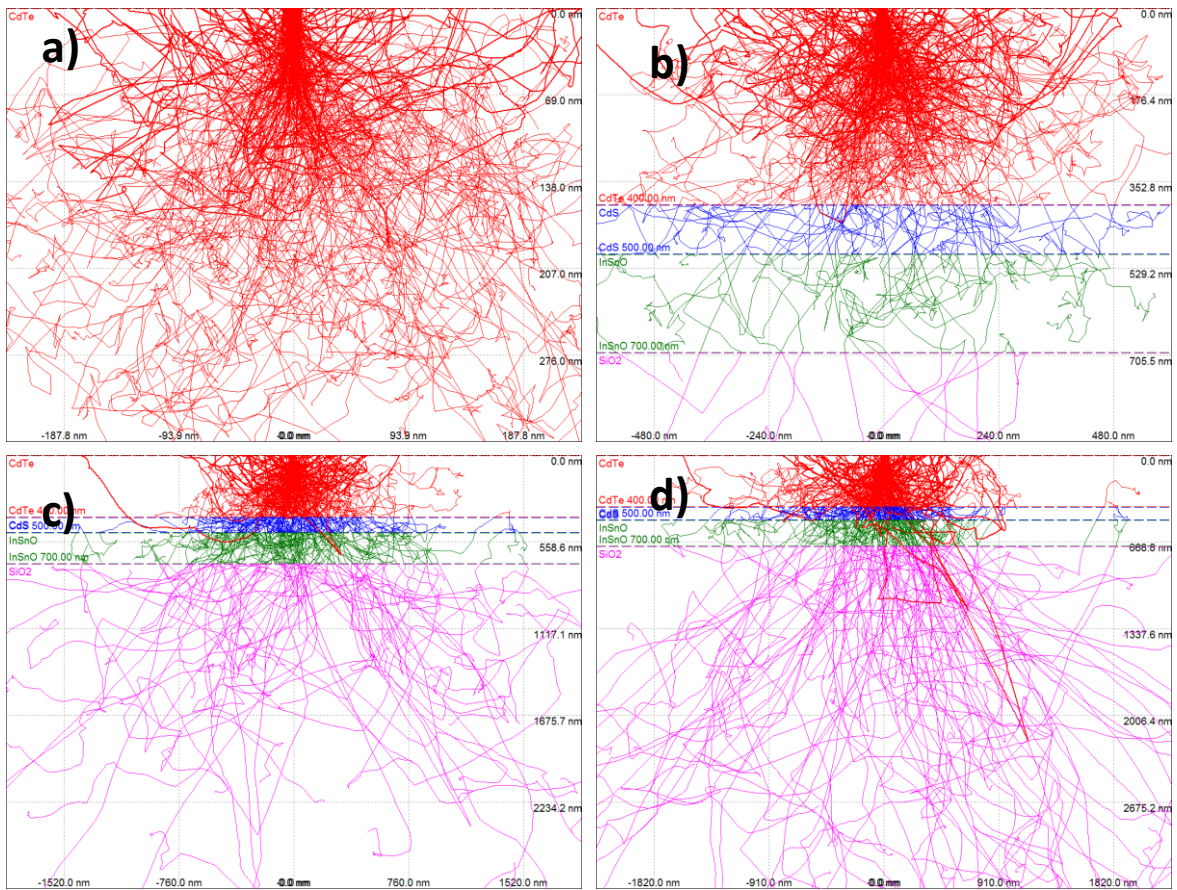


Figure 56. E-beam scattering in nano-pattern sample at different accelerating voltage values.  
a) 10.0kV b) 15.0kV c)20.0kV and d) 25.0kV

### 7.3 Electron-beam scattering in Micro-islands

In a similar way, a micro-structure of the CdTe was analyzed by following the same procedure. This time, the CdTe thickness was set up to 1500 nm. In contrast to the nano-structure, here we can observe that scattered electrons start to reach the other layers at higher accelerating voltage of 25.0kV due to the thicker CdTe.

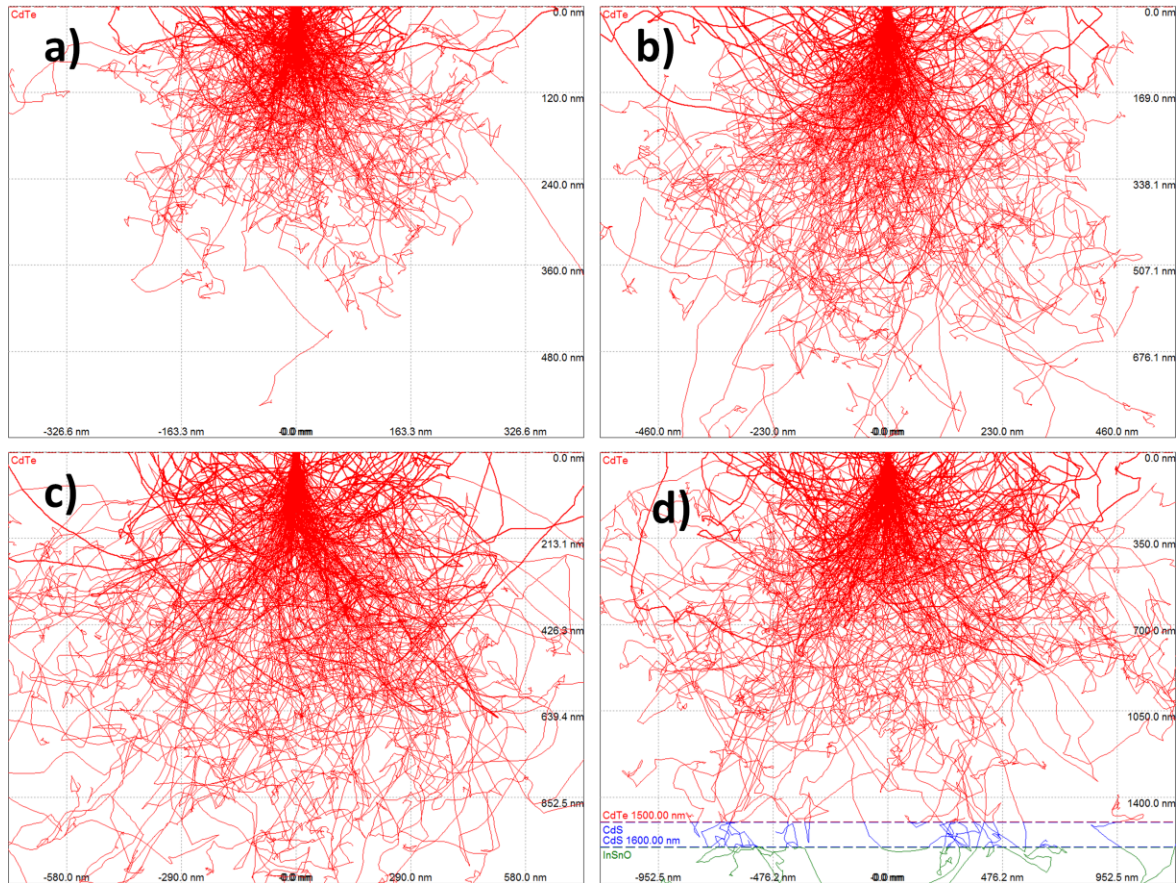


Figure 57. E-beam scattering in micro-pattern sample at different accelerating voltage values.  
a) 10.0kV b) 15.0kV c) 20.0kV and d) 25.0kV

#### 7.4 E-h pairs generation rate and Calculation of number of suns.

From the simulations and considering some assumptions we can calculate the generation rate and the equivalent number of suns stimulating the solar cells by the e-beam. The first calculation is to estimate the number of collisions. Assuming that each electron will lose 1.5 eV of energy per collision and an initial energy equal to the accelerating voltage, the number of collision is calculated as follows,

$$\frac{20,000 \text{ V (acc. voltage)}}{1.5 \text{ eV (CdTe energy)}} = 13,333 \text{ collisions}$$

Then, we calculate the number of electrons striking the sample per second,

$$\frac{0.5 \text{ nA (e - beam current)}}{1.6 \times 10^{-19} \text{ C (charge of electron)}} = 3.12 \times 10^9 \text{ e/s}$$

Now, the number of e-h pairs generated by the e-beam is given by,

$$\frac{3.12 \times 10^9}{13,333} = 4.16 \times 10^{13} \text{ e - h/s}$$

Considering a volume of the structure of  $1.4 \times 10^{-12} \text{ cm}^3$  the generation rate can be calculated by,

$$G = q \left( \frac{4.16 \times 10^{13} \text{ e - h/s}}{1.4 \times 10^{-12} \text{ cm}^3} \right) = 2.85 \times 10^{25} \text{ e - h/cm}^3 \text{ s}$$

In summary, this is the calculated generation rate due to the electron-beam assuming that each collision generates an e-h pair and that each collision loses 1.5 eV. The next step in the analysis is to estimate the photocurrent in the device. For this calculation it is assumed that;

$L_e + L_p + W = 2 \times 10^{-4} \text{ cm}$ . In other words the sum of the diffusion lengths and depletion widths is 2 microns. The photocurrent is then calculated as follows,

$$J_{L(simulated)} = qG(L_e + L_p + W) = \mathbf{888\ A/cm^2}$$

This is a very high photocurrent compared to typical photocurrents at AM1.5. A typical photo current at AM1.5 is approximately  $0.027\ A/cm^2$ . The actual experimental photocurrent measured in the solar cells can be obtained dividing the short-circuit current by the area of the CdTe grain. For the case of grain 1 of the  $1\ \mu m$  feature size, the photocurrent is,

$$J_{L(measured)} = \frac{I_{sc}}{A} = \frac{4 \times 10^{10}\ A}{7.85 \times 10^{-9}\ cm^2} = \mathbf{.046\ A/cm^2}$$

The number of suns can now be estimated by dividing the photocurrent by the typical photocurrent of a device under AM1.5 illumination. For the simulation data we have,

$$No.\ of\ suns_{(simulated)} = \frac{888\ A/cm^2}{.027\ A/cm^2} = \mathbf{32,888\ suns}$$

For the experimental data,

$$No.\ of\ suns_{(measured)} = \frac{.046\ A/cm^2}{.027\ A/cm^2} = \mathbf{1.7\ suns}$$

Using the number of suns, it is now possible to estimate the Voc of the device to determine whether a high degree of e-beam stimulation is responsible for the large Voc's measured during nanoprobng. In order to do this, the Voc' formula below takes into account the possibility of stimulation greater than one sun as follows,

$$V_{oc}' = \frac{nkT}{q} \ln\left(\frac{XI_{sc}}{I_o}\right) = \frac{nkT}{q} \left[ \ln\left(\frac{XI_{sc}}{I_o}\right) + \ln X \right] = V_{oc} + \frac{nkT}{q} \ln(X)$$

Equation 8. [33]

where  $V_{oc}$  is the ideal open-circuit voltage assumed to be .900 V and  $X$  is the concentration of light calculated.

Then we have for simulation results,

$$V_{oc}' = .900 + .026 \ln(32888) = \mathbf{1.17 \text{ V}}$$

And for experimental data,

$$V_{oc}' = .900 + .026 \ln(1.7) = \mathbf{0.913 \text{ V}}$$

We can summarize the calculations for both cases in Table 3.

Table 3. Measurements for simulation and experimental data.

<b>Type of Data</b>	<b>No. of suns</b>	<b>Voc' (V)</b>
<b>Simulated</b>	32,888	1.17
<b>Experimental</b>	1.7	.913

In conclusion this analysis shows that the high degree of stimulation by the e-beam does not explain the large  $V_{oc}$ 's observed during nanoprobeing. Although 32,888 suns were estimated due to the e-beam, the  $V_{oc}$  should only have increased to approximately 1.17 V. Therefore, something else caused a high measurement in the  $V_{oc}$ .

## CHAPTER 8: CONCLUSIONS

This thesis presented nanoprobe characterization of micro and nano-patterned CdTe based solar cells as well as additional explanations and analysis of the results collected. Nanoprobe is an interesting and very promising method for characterization of micro and nano-patterned solar cells, however, some issues were encountered that need to be addressed to improve the technique. The SEM accelerating voltage and condition of the condenser lenses influence the I-V response of the solar cells. Therefore selection of the accelerating voltage and condenser lenses is important since it determines how the sample is stimulated and its response to the stimulation. First the e-beam current was measured using a Faraday cup and a pico-ammeter as a function of accelerating voltage and condenser lens condition. Second, the I-V response was observed as a function of accelerating voltage and condition of the condenser lenses.

A second conclusion is that the use of an e-beam produced an effect similar to sun light however, the  $V_{oc}$  exceeded the maximum theoretical value possible for CdTe solar cells. It was estimated that a high level of current injection via the e-beam was occurring: ~33,000 suns maximum. However this high level of current injection did not explain the high  $V_{oc}$ 's observed. Combined simulated/theoretical analysis of the solar cell stimulation by the primary electron-beam suggested a very high electron-hole generation rate equivalent to ~33,000 suns. However, even this high degree of stimulation cannot explain  $V_{oc}$ 's above the band gap.

Also, it was suspected that the lack of a back-contact to the CdTe islands made it difficult to acquire a good I-V response due to high contact resistance. In order to overcome this issue, devices with ZnTe and Cu back-contacts were fabricated and nanoprobe. Measurements in which ZnTe was used as back-contact did not show any improvement in the I-V response. On the

other hand, by contacting the CdTe with a thin layer of Cu deposited on top, the I-V curve showed a great improvement mainly in the increase of the short circuit current and a noiseless signal. However a question remained as to the effective area of the Cu contact since it is likely that the area was much larger to due connecting several adjacent grains.

## CHAPTER 9: FUTURE WORK

After analyzing the results obtained from the various tests, it is necessary to make improvements in the procedures and equipment in order to obtain more accurate data. The first item recommended to further develop the nano-probe characterization on patterned solar cells is to utilize a light source that could be placed inside the SEM and capable of providing a light intensity of 1 sun instead using the SEM e-beam. Also, the design of a stage that makes possible to mount a sample without obstructing the light source, is another improvement that would facilitate the nano-probing technique.

Moreover, increasing the accuracy to 10.0 PLC in the Keithley software could help to obtain a low noise level in the I-V measurements. By having this option in the software, the speed setting is slower and so a more accurate reading can be performed.

Finally, the measurements can be calibrated by obtaining a contact resistance from a transmission line model. The transmission line model (TLM) is an original model proposed by Shockley which is used to determine the contact resistance for planar ohmic contacts. [36] In order to perform the experiment, a set of spaced contact pads need to be marked in the film. [37] An ohmmeter is then used to measure the resistance between the contact pads and then plotted as a function of the separation distance. [37] Figure 58 shows an example of the graph to be obtained by using this method.

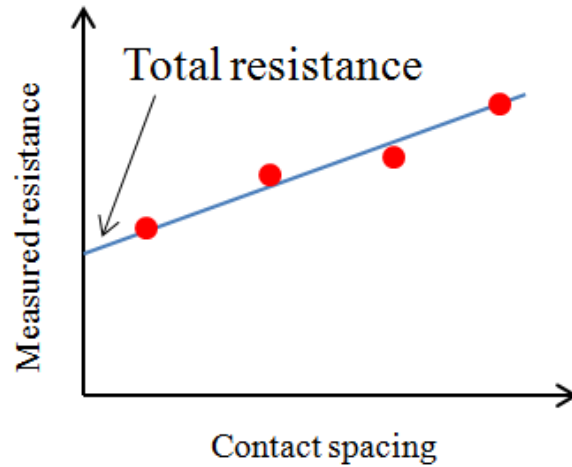


Figure 58. Total resistance measured as a function of contact spacing. [37]

The total resistance is the point where the linear is equal to zero contact spacing. This line is the connection between the measured resistances of the contact pads (red points) at different distances. [37] Thus, the use of this method will lead us know the resistance that exists between the tungsten probe and the CdTe surface. This procedure will provide a way of calibration for future measurements.

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## **CURRICULUM VITAE**

Heber Prieto was born on December 21<sup>st</sup> of 1987 in El Paso, Texas. He attended most of his school years in Ciudad Juárez, Mexico. Graduated from Preparatoria “El Chamizal” in 2006, he decided to continue his college studies at the University of Texas at El Paso. He enrolled in the Electrical Engineering program from which he was awarded with the Outstanding Senior Project award and graduated with Cum Laude Honors in 2010.

The following Fall semester, he started to work towards his Master of Science in Electrical Engineering, one semester later he joined the Nano-Materials Integration Laboratory (NanoMIL) group as a research assistant, under the mentoring of Dr. David Zubia. During his graduate studies, he worked in the patterned CdTe-based solar cells project and participated in two consecutive summer internships with Sandia National Laboratories in Albuquerque, NM.

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