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Low Power Design Techniques for Data Acquisition

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LOW POWER DESIGN TECHNIQUES FOR DATA ACQUISITION

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Dedication

I dedicate this dissertation to my parents, Rama Rao Palakurthi, father, and Lakshmi Palakurthi, mother, and to my brother, Raghavendra Rao Palakurthi.

LOW POWER DESIGN TECHNIQUES FOR DATA ACQUISITION

by

PRAVEEN KUMAR PALAKURTHI, M.S(EE)

DISSERTATION

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Abstract

Semiconductor technology advancement continues to lead to smaller device geometries. Digital circuits have benefited from the technology scaling whereas analog circuits often suffer in terms of performance and noise immunity. As functionality continues to be integrated onto systems-on-chips, analog circuits consume increasingly more power than digital circuits and the objective of this dissertation is to explore low power techniques in the context of both digital and analog circuits residing on the same silicon real estate.

As natural signals are in analog form, a necessity exists to convert these into digital form and then back again in order to exploit the advances of digital processing. As a part of this dissertation, a Digital-to-Analog Converter (DAC) is explored in the context of requirements of both low power consumption and high voltage and temporal resolution. On on-going collaboration with SPAWAR, Navy San Diego has provided guidance for challenging electronics applications - including magnetometers and biomedical sensors.

The proposed design implements subthreshold rad-hard level shifters and low power DACs for a NAVY patented sensor - serving as a showcase application. The DAC was designed for TSMC 0.25 μ m CMOS technology as captured in Virtuoso Cadence - providing a suite of silicon development and evaluation tools required to evaluate the circuits and chips designed and fabricated in the course of this research. The final implementation of the chip is demonstrated through layout and extracted simulation to provide high performance, while maintaining a reasonable footprint and operating with low power when compared to other reported commercial and research DACs.

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Chapter 1: Introduction

1.1 MOTIVATION

As described by Moore's law, the number of transistors on a typical chip has been growing exponentially for a given silicon area. Gordon Moore – an engineer and leader at Intel – noted elements of the growth of the semiconductor industry which included an increased factor of speed and functionality every 18 to 24 months based on the decreasing channel length of the transistor. With a smaller transistor sizes, circuits operate faster with less energy per operation and with a higher functional density. This advancement has manifested benefits such as reduced power consumption – for the same functionality - and improved performance; however, other challenges have arisen including temperature dependencies and static leakages that now begin to become dominant in the most recent sub nanometer technologies. Battery-operated applications such as battery-powered consumer electronics (e.g. digital watches, cell phones, gameboys, etc.),

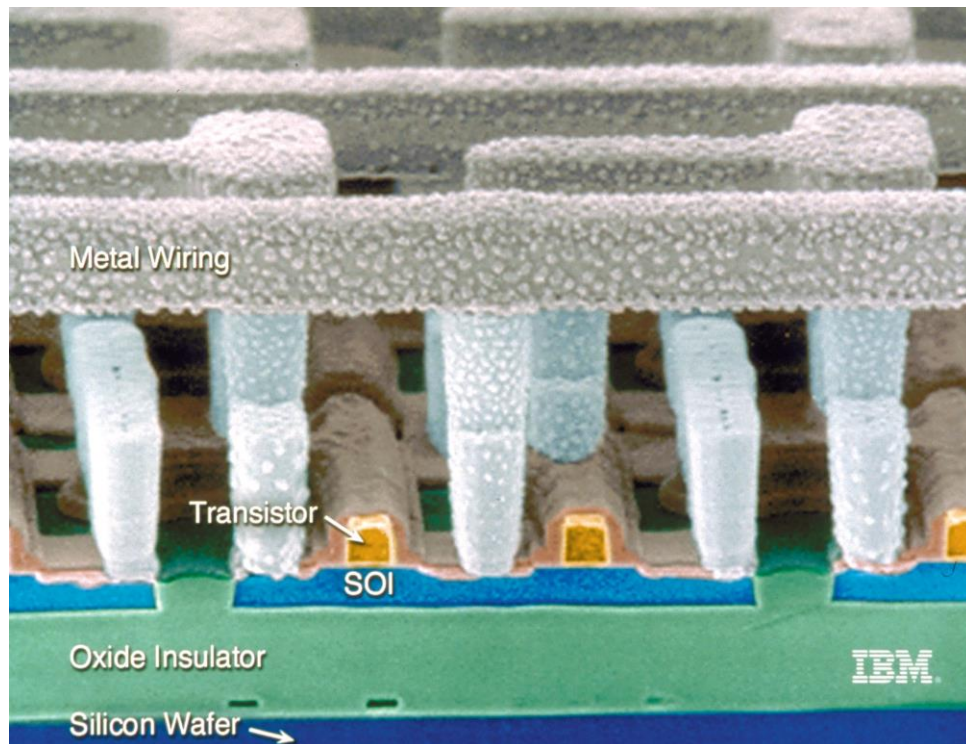


Figure 1.1 - CMOS technology from IBM – transistor level and wiring interconnect – both scaling as described by Moore's Law. [1]

unattended wireless sensors in networks, biomedical wearable and implantable devices, all demand a reduction of power consumption [2-3]. Over the years with each new technology node, operating voltages have scaled down to maintain the electric fields across the thinner oxide gate oxides. However, the scaling which has been mostly beneficial for the digital circuits has complicated the landscape of analog circuits. In mixed signal design, digital and analog circuits share the same silicon and the power consumption of analog circuits has become dominant in the overall chip power consumption – as these circuits often employ larger substantially large transistors as well as *always on* biasing currents / voltages. In the last decade, significant focus has been brought to bear to reduce the power consumption of analog circuits in the context of modern CMOS semiconductor technology.

The advancements in Integrated Circuit (IC) technology have led to the reduction in minimum photolithographical feature size, to sub nanometers, and operating voltage (V_{dd}), which results in a reduction of charge stored in a circuit node capacitance C_{node} ($Q = V_{dd} * C_{node}$) [3-4]. A small amount of charge is sufficient to alter the node voltage. Therefore, the operation of the circuits has become even more challenging in harsh environments such as in space where cosmic particles can result in electron-hole pair generation – adding or subtracting charge from nodes at unintended times of operation. This research addresses the requirements of low power consumption of analog circuits and hardware resilience in hardened environment. The proposed research combines (1) low power analog techniques, (2) subthreshold operation as an aggressive approach for reducing digital power and (3) radiation hardening. Although not mutually exclusive, garnering the benefits of any one tends to be at the odds of the other two with regards to the necessary engineering trade-offs – where the interwoven redundancy required to combat soft errors increases power for the same operation and the dramatic circuit dimensions of the analog circuits required to withstand radiation noise will overwhelm the power reduction gains of digital circuits in the most modern CMOS technologies.

1.1.1 Research Objective

The proposed research included the exploration of providing power efficient mixed signal circuits through an extreme reduction in supply voltage – quadratically related to the both dynamic and static power consumption – while not compromising the circuit performance and operation in terms of noise sensitivity. The objective of the research was to address power consumption in analog circuits while maintaining resilience to radiation and noisy environments given the susceptibility introduced by operating at very low voltages. The concept of the proposed research is that – where possible - the supply voltage is reduced below the threshold voltage of the unit transistor and although there is a corresponding drop in performance, circuits operate at a minimum energy per operation point and the performance degradation in many applications may not be an issue – such as implantable devices or low bandwidth unattended ground sensors. The proposed research involved the design, simulation and evaluation of analog circuits that are designed to operate as close to the threshold level as possible while continuing to function correctly and combined robust (rad-hard) subthreshold digital circuits when possible. Furthermore, the analog circuits were aggressively designed with as many low power design elements as possible to (1) take advantage of low power subthreshold digital operation when possible and (2) exploit and invent other opportunities for low power operation in the traditional analog sense – capacitive Digital to Analog Converters as opposed to constant-current resistor ladders for instance. Serving as a demonstration, an ultra-low power sensor was designed and will be fabricated for providing unprecedented sensitivity for unobtrusively collecting a multitude of biological signals assessing health, and cognitive performance of a subject. The sensor as a collaboration with SPAWAR Navy in San Diego employs non-linear dynamics to incorporate chaotic oscillators to provide picoamp level sensitivity on capacitive current sensors and with such sensitivity provides a well-suited showcase circuit for the design techniques explored in this dissertation.

1.2 DISSERTATION ORGANIZATION

This dissertation is organized as follows: Chapter 2 provides the background on low power consumption techniques, subthreshold, and radiation hardened (rad-hard) design techniques. Chapter 3 describes the subthreshold to super-threshold conversion process and circuits, which are used to interface between different voltage islands when employing subthreshold operation to reduce the average energy per operation. Chapter 4 analyzes the proposed design and architecture of an ultra-low power digital to analog converter, which uses the techniques discussed in chapter 2 and chapter 3. Chapter 5 describes the design and architecture of an ultra-low power non-linear sensor for sensing biological signals or other picoamp signals and is an on-going collaboration between the University of Texas at El Paso and SPAWAR, Navy San Diego, California and chapter 6 provides conclusions and future work.

Chapter 2: Background

2.1 Low power design

The number of active devices on a given area of silicon continues to increase with every technology introduced as photolithographical processes continue to improve. An exponential increase in device density improves functionality but is also responsible for an increase in design complexity – complicating testing and managing energy management. Design factors like performance and power consumption playing the prominent role in emerging applications. Few applications demand high performance for which clock must operate at a high frequency (over four GHz) or constantly – often with opportunities to disable the clock and garner significant power savings. As the clock frequency is proportional to the system power consumption – high frequency operation is not desirable for the portable devices that operate on battery and that do not have application requirements that force fast operation. Moreover, local hot spots on the die consume power several times higher than the average power density that is also not desirable for the battery operated devices and cause increased local leakage thermal gradients and the increased thermal management complexity. In the last few decades, along with the mentioned factors, the introduction of design reusability and Intellectual Property (IP) as a design practice also have increased the focus on low power design. Today, the power budget is one of the most important design considerations - along with cost - after addressing the required functionality that the final product must provide.

In the submicron technology, millions of gates can be implemented on given piece of silicon. This has led to an increase in the power consumption and cost for thermal management, which has also increased. Also, leakage currents have increased dramatically with each technology. In order to reduce the power consumption, the techniques can be applied at device level, gate level, circuit level, and system level during the product development.

The power consumption of a chip consists of a combination of both the dynamic and static power. The dynamic power is the result of transitions of each of the signals transitioning – charging and discharging of the parasitic capacitance of the node, whereas static power is the result

of leakages of the transistors that are not active and are operating in the subthreshold region. Dynamic power is mainly due to switching activity and is proportional to the clock frequency and activity factor (average probability of a transition on a data signal) and can include shoot through current if the both transistors are in the pull up and pull down circuits are activated simultaneously. However, if the ramp time of the average input signal is small, the switching activity dominates the dynamic power consumption relative to the shoot through current power. Ignoring shoot through power, Dynamic power consumption is given by equation 2.1.

$$P_{dyn} = C_{eff} * V_{dd}^2 * P_{trans} * f \quad (2.1)$$

Where, P_{dyn} is the dynamic power consumption, C_{eff} is the effective output load capacitance (number of nodes times the average node capacitance), V_{dd} is the supply voltage, f is the chip frequency, P_{trans} is the probability of an signal transition at any node [5]. There are several techniques to reduce the dynamic component of the total power consumption. The techniques mainly concentrate on supply voltage and frequency such as multi-voltage, voltage and frequency scaling, clock gating, etc.

Static power consumption is mainly due to the leakages in the device that includes Subthreshold Leakage, Gate Leakage, Gate Induced Drain Leakage, and Reverse Bias Junction Leakage and generally technology related and not related to the actual operations. In the latest technologies, Subthreshold and Gate leakages dominate among others as the channel lengths are driven in to the deep submicron region. In sub nanometer technologies, static power consumption can play an important role (large fraction) in the total power consumption. The major techniques involved in reducing the static power consumption are Multi- V_t and Power Gating. Multi- V_t uses high V_t for performance goals and low V_t for the gates included in the critical path of the logic that dictate that maximum frequency. Power gating is used to shut down the power to a block when it is not active – eliminating not only unnecessary dynamic power but also static power but suffocating the power supplies to a circuit – the outputs of which are not necessary during the power gating.

2.2 LOW POWER TECHNIQUES

Many of the design techniques that can be used to improve energy efficiency of integrated circuits are described in this section.

1) Gate level Power optimization

At the synthesis level of chip design, the logic can be manipulated to improve power from both static and dynamic power standpoint by manipulating the gate levels and architecture.

a) Gate Merging: The major component in dynamic power consumption is the wire capacitance. If the net can be dissolved into a gate then the dynamic power consumption can be reduced by reducing the overall number and average capacitance of the average net. One way to dissolve nets is by Gate Merging. Gate merging is achieved by using the design techniques like And-Or-Inverter (AOI) or Or-And-Inverter (OAI) and is demonstrated in Figure 2.1. Power consumption can be also be further reduced by properly choosing the gate sizing of the transistors – which depends on the output loading but which affects the input capacitance and dynamic power consumption.

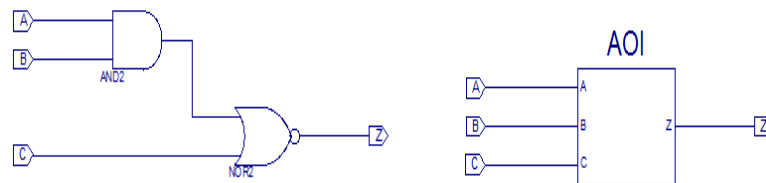


Figure 2.1: Gate Merging. AND – NOR merged into AOI

b) Slew (Transition) Optimization: The internal power of a gate depends on the slew of input signals. If the slew is too large, there will be a leakage between power supply and ground of a gate. If the gate is not in the critical path, a buffer can be used to improve the slew that reduces the leakage. This technique is illustrated in Figure 2.2.

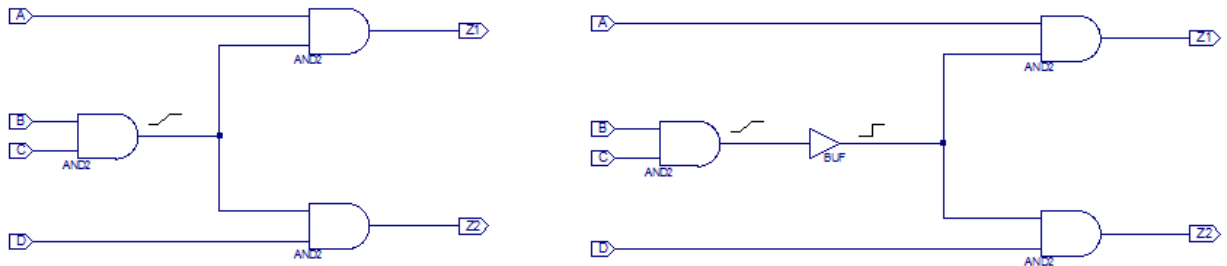


Figure 2.2: Reducing Slew by adding buffer

c) Input Reordering: Reordering of inputs can reduce the charging and discharging of the intermediate capacitances. The pin reordering technique is demonstrated in Figure 2.3 where the timing can be exploited to ensure that gate intermediate nodes are not unnecessarily charged and discharged – resulting in inadvertent power consumption. As described in the Figure 2.3, introducing the high activity input to a higher fan-in input reduced the switching activity of the intermediate capacitance.

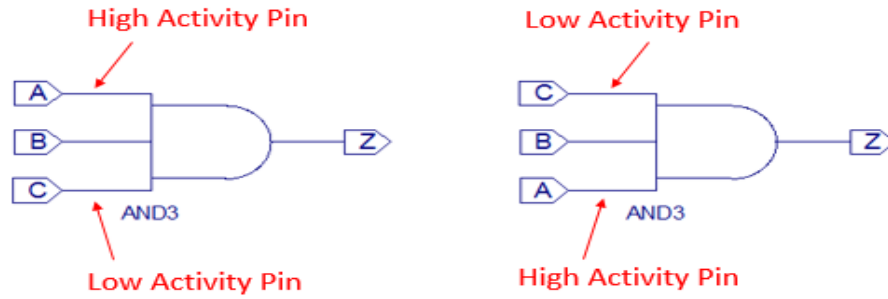


Figure 2.3: Input Reordering

2) Multi-V_{DD}

From equation 2.1, dynamic power is proportional to V_{dd}^2 . Careful reduction of the power supply in circuits where performance is not critical can be exploited to reduce the power consumption dramatically. With the development of SOC design, multiple power supplies are made possible and can be implemented with automation where different sections of the chip can be supplied with different power rings and stripes. However, multi- V_{dd} techniques introduce complexity in the design such as increase in IO pins for the additional power supply levels, level shifters to convert between the different island and a complex power grid in which thermal management and IR drop become substantially more complex to model and address. Figure 2.4 illustrates the multi- V_{dd} technique in which different regions of the die are assigned to different voltage regions – 1.8 V could be used for high performance sections but this would also result in high power areas in both dynamic and static perspective; 1.2 V could be assigned to all other areas as long as static timing requirements could be met with the library files describing the standard cells at this much lower performance point. The large fraction of the circuits would be set to this 1.2 V and only the circuits with the highest requirements would be set to 1.8 V.

3) Multi-Threshold

As feature size has reduced with each technology node, the threshold voltage of a transistor also reduced; however not at the same rate as the supply voltage as there is a decade increase in leakage for approximately every 70-80 mV of V_t drop. This reduction is required given the $(V_{gs} - V_t)$ difference requires both V_{dd} and the V_t to reduce more or less with to a proportional level. Therefore, using multiple threshold transistors, where required, can ensure the reduction in power consumption for low performance circuits while providing a boost for cherry-picked circuits along the critical path [1]. The dual threshold approach necessitates a second library of identical standard cells with a single difference in layout of the additional implant – which primarily affects timing and leakages in the db files. The second implant does add to the fabrication cost of the entire chip by a fixed amount regardless if there is one low V_t gate is added or if 100% are substituted.

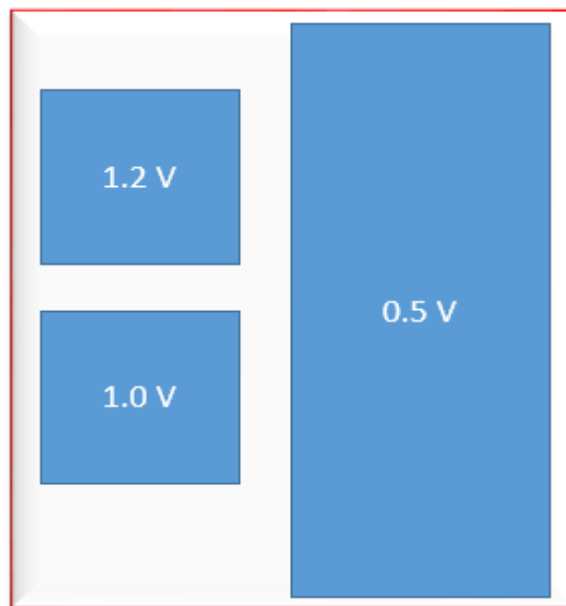


Figure 2.4: Multi-Voltage Architecture using Voltage Islands

4) Clock Gating

The clock is the most important signal in any sequential circuit. Clock trees consumes approximately 30% of the dynamic power consumption of the entire chip as the clock signal oscillates at twice the frequency of the fastest data signal and all sequential and combinatorial transitions are generated by the clock rising edge. Consequently, reducing the power consumption caused by the clock is critically important and is based reducing the activity of unused clock tree – referred to as a technique called *clock gating*. Clock gating can be implemented in two different ways: Latch-based and Latch-free. The techniques are described in Figures 2.5 and 2.6. By using latches, glitches can be avoided and static timing analysis tools can be used to ensure that no enable to clock transitions can cause short clock pulses that may be too short to ensure proper flip-flop operation. By simply using a logic gate like a AND gate, an enable can gate the clock but much more care must be taken to ensure no glitching. Glitching can that propagates to a group of flip-flops can be seen as a cycle by some and not by others in almost a random statistical decision.

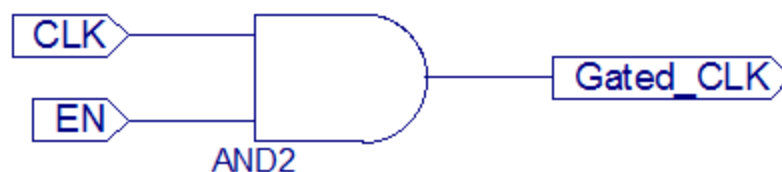


Figure 2.5: Latch – Free Clock Gating

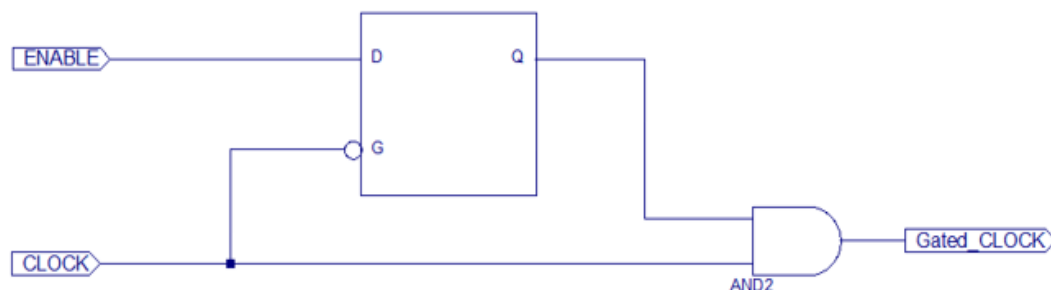


Figure 2.6: Latch Based Clock Gating

5) Power Gating

Power gating is an advanced technique in reducing power consumption by adding large low resistance switches to the V_{dd} and ground supplies to large sections of the integrated circuit. Clock gating ensures the reduction of power supply in clock network, but not outside the clock network. Power gating is used to turn off the power supply to all inactive blocks in a chip. Power gating reduces stand-by and leakage power by completely eliminating the path of the current through the transistors that are operating in the subthreshold operating mode. The main drawbacks of the technique are twofold: (1) the switching transistors that gate the power supplies are required to be very large (wide) to ensure a low resistance path, thus increasing area of the circuit and cost, (2) the resistance that is introduced causes IR drop when large currents are drawn during high performance operation. The IR voltage drop must be accounted for during worst case timing and thus results in reduced timing in the critical path the maximum frequency.

2.3 SUBTHRESHOLD LOGIC

CMOS circuits essentially operate on transistors running in one of two states – the *on* state (saturation) and *off* state (subthreshold). The transistor is said to be in the *on* state if the supply voltage exceeds the threshold voltage and in *off* state if the supply voltage is less than the threshold voltage. Subthreshold circuits operate far below traditional voltage supply levels and the transistor essentially operates on leakage. Operating below the threshold voltage results in indolent performance, however this penalty is acceptable if confined to low performance functions and applications. Figure 2.7 illustrates the I_{ds} vs. V_{gs} for both NFET and PFET devices in logarithmic format and clarifies how although the devices are never fully on in subthreshold mode, but that a sufficient difference in drive current exists between the *on* and *off* state to allow for logical function. As power is related quadratically to the supply voltage, reducing the voltage to these ultra-low levels results in a dramatic reduction in both power and energy consumption in digital systems in terms of logical operation.

Circuits running at these low voltages are less robust to noise and radiation, which can unintentionally alter the circuit operation as the amount of charge at each node is reduced. With each new technology, the sensitivity to radiation in subthreshold region became more pronounced as critical charge (Q_{crit}) is decreasing with the supply voltage and node capacitance. The Q_{crit} value is the metric for robustness – the higher the value the more difficult to corrupt stored data. The Q_{crit} is proportional to the supply voltage and node capacitance and in subthreshold the value is significantly degraded as supply voltage is driven to such dramatically low values.

Significant work has been performed on understanding which CMOS circuit styles are most suitable for digital subthreshold circuits with an emphasis on combinatorial and sequential elements, level shifters (without attention paid to radiation and noise) and charge pumps [7-10]. Pedestrian traditional CMOS circuits – used for over 30 years in the majority of digital integrated circuits – have been shown to still be the best general choice for most applications operated at ultra-low voltage. CMOS provides the best noise margin and highest performance and can be dynamically scaled to higher voltages if significant performance is required temporarily. Flip-flops have been explored and novel circuits have been proposed that are not only optimized for subthreshold operation but that simultaneously provide radiation hardening [11-14]. Other peripheral circuits, which will be particularly important in light of subthreshold operation include level shifters – required for translating low voltage signals to usable levels by the outside world – and charge pumps – required to provide super-thresholds when only subthreshold supplies are available (e.g. energy harvesting generally provides only subthreshold levels). For level shifters, several designs have been explored that can translate from sub-to-super-threshold levels [15-16]; however the proposed work will investigate subthreshold level shifters in terms of radiation as well as these circuits include a latching mechanism that can be flipped by radiation or noise. Finally, charge pumps have been explored in the context of subthreshold as often a higher voltage is required and a subthreshold charge pump can provide a temporary low power voltage from subthreshold values – many of which are well-suited for generation from energy harvesting. The effects of radiation have not been explored in this context but would likely only result in a slight

degradation in performance based on lost charge due to electron hole pair generation of a strike that would work potentially against the charge pumping process. The proposed work will not explore radiation in charge pumps due to the lack of relative importance.

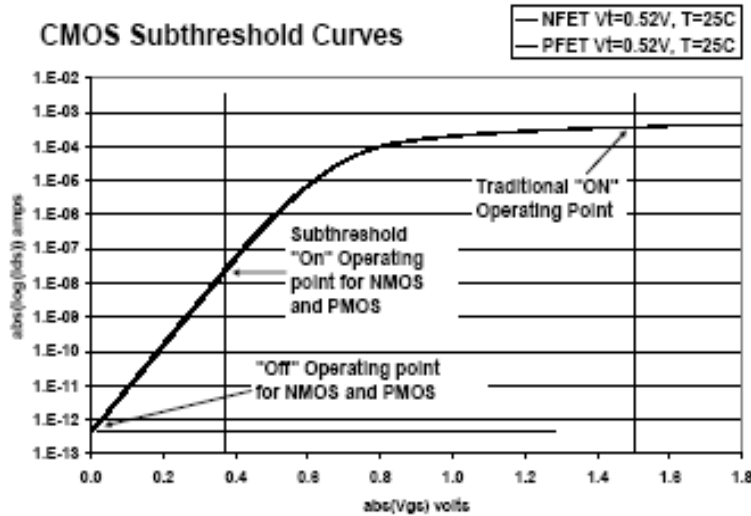


Figure 2.7: Subthreshold Operation.

2.4 RADIATION HARDENING DESIGN

As CMOS technology relentlessly scales to smaller geometries, operating voltages and parasitic capacitances are also reduced, which has led to another challenge for electronics: soft errors in sequential circuits. Traditionally, soft errors were confined to space applications as in this environment there exist the radiation but these errors are now considered possible in many terrestrial applications such as bio-medical devices due to high reliability requirements of devices that can be operated within the body and often exposed to intentional sources of radiation. When radiation strikes an active device fabricated on silicon, many of the elements such as memory, latches and flip-flops can have the contents of held data become corrupted if the collected charge from an ionizing strike exceeds the critical node charge - Q_{crit} . This threshold amount of charge required to alter the value at a node (flipping the bit, causing data corruption, yet leaving the cell full functional) depends on the node capacitance and supply voltage $Q_{node} = V_{dd} * C_{node}$. With each

new CMOS technology, the operating voltage is generally decreased, which increases the sensitivity of the effect of radiation. Additionally, applications requiring low power operation are more susceptible to radiation as the supply voltage may be lowered further to improve energy efficiency per operation.

As described before, subthreshold circuits are more suitable for low power applications that can deliver minimum energy per operation [17]. Consequently, fault tolerant sequential elements will be necessary for subthreshold operation as highlighted in a radiation experiment described in [18]. These robust circuits generally rely on interwoven redundancy in the sequential elements and as a result an increase in circuit area and power consumption as well as a decrease in performance is incurred.

[19] is the first paper to ever forecast the Single Event Upset (SEU) in microelectronics due to cosmic rays. In this paper, authors discuss the limitations on device size and packaging due to the radiation effect. The authors describe that the influence of cosmic rays creates excess electron-hole pairs and decay the normal lifetime of carriers in the device. Also, if the lifetime is larger than the minimum operating time, a false signal will be resulted. However, [20] simply predicts the effects but not enough errors were observed to prove this theory. In 1975, Binder et al. [21] reported that anomalies in communication satellites are due to the unexpected triggering in digital circuits that are caused by the interactions with galactic cosmic rays. This paper proposed that 40 flip-flops caused the four events that were observed in 17 satellite years of operation. The calculation of the cosmic ray event rate required the determination of transistor parameters, charge collection efficiencies and the number of sensitive transistors. The authors used the scanning electron microscope to determine the number of sensitive transistors. The observed rate was 1.5×10^{-3} transistors per year. The authors proposed that this rate agrees reasonably well with the calculated value of 3×10^{-3} transistors per year. All of these papers dealt with the SEU in space. However, [22] proposed that the SEU is not in just a problem in space but primarily at the ground level and is caused due to alpha-particle contaminants in packaging material. Radioactive Uranium contaminants in the water used by the factory were contaminating the ceramic packages.

[23] proposed that SEUs are caused not only due to ionization by heavy ions but also due to proton and neutron indirect ionization effects. This has changed the approach towards SEUs because of the number of protons are much higher than the heavy ions in the space. Much of the research in this field has focused towards the memories, latches, flip-flops for successful military and space operations [24-32].

The implementation and irradiation of the design described in [33] was completed and this design was the inspiration for the radiation-hardened level shifter that was fully conceived in the course of this research. The level shifter was a key element in one of the two DACs explored as part of this dissertation. This section discusses the contributions made in a radiation experiment of a flip-flop.

Ameet Chavan's Rad-hard Flip-Flop

Based on the dissertation of Ameet Chavan completed at the University of Texas at El Paso and a resulting design of a rad-hard flip-flop, the design was implemented in layout, fabricated and irradiated with metal ions at the Texas A&M's Cyclotron Institute in the Spring of 2011. Fig 2.8 shows the radiation chamber. The circuit proved to be effective and unprotected circuits – included on the silicon for comparison as a baseline and operating at both traditional and subthreshold supply voltage levels - were shown to have an exponential increase in sensitivity to radiation at subthreshold levels [34]. The flip-flop was not developed in this dissertation but the implementation and radiation evaluation were done in the course of this research. The resulting design has inspired other radiation hardened aspects of this work and is used in the digital sections to provide sequential elements for chips designed with the goal of eventually irradiating the designs to measure robustness.



Figure 2.8: Ameet Chavan and Praveen Palakurthi in Radiation Chamber

Circuits operating at low voltage are more susceptible to harsh environments such as though including radiation that can unintentionally change the circuit operation. This effect is more severe in sequential circuits such as flip-flops, latches, and memories as the radiation can remove or introduce additional charge held at a critical node – resulting in a transient voltage pulse. As preliminary research, the subthreshold rad-hard flip-flop proposed in the dissertation [35] along with a traditional (unprotected) flip-flop, a Sense-Amplifier-based Rad-hard Flip-Flop (RSAFF) and a Dual Interlocked storage Cell (DICE) flip-flop were implemented in Lincoln Lab’s XLP 0.15 μm SOI technologies. Additionally, all four flip-flops were irradiated with heavy ions at the Texas A&M’s Cyclotron Institute. The subthreshold flip-flop is demonstrated in Figure 2.9.

The flip-flop is based on master-slave that constitutes two rad-hard latches. Both latches are designed with redundancy stored at two different nets. These two nets form a feedback to restore data after a SEU. The proposed design is fine-tuned for subthreshold operation by keeping transistor stacking to less than two transistors as stacked transistors reduce the drive strength more than in subthreshold. Figure 2.9 illustrates the basic latch. Redundant nets are interwoven while

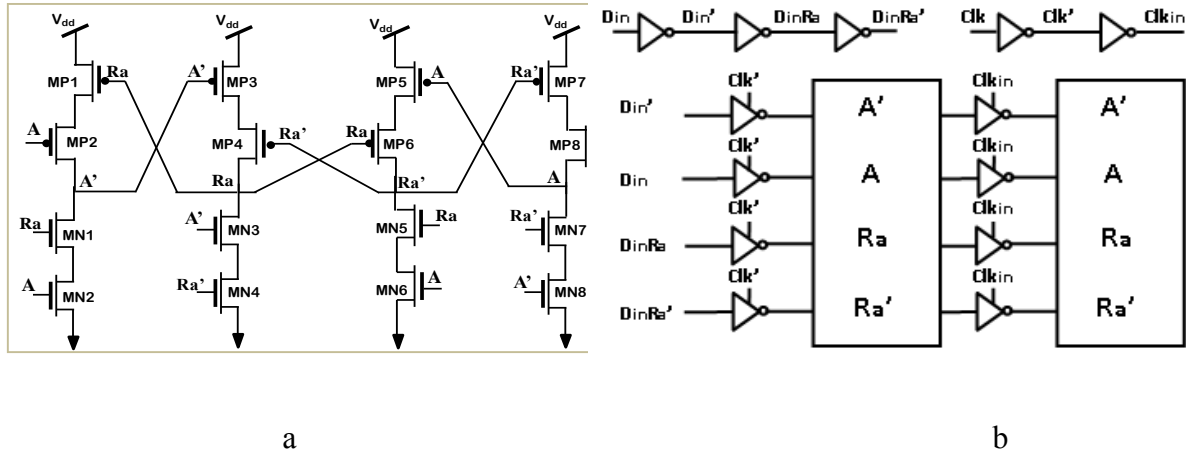
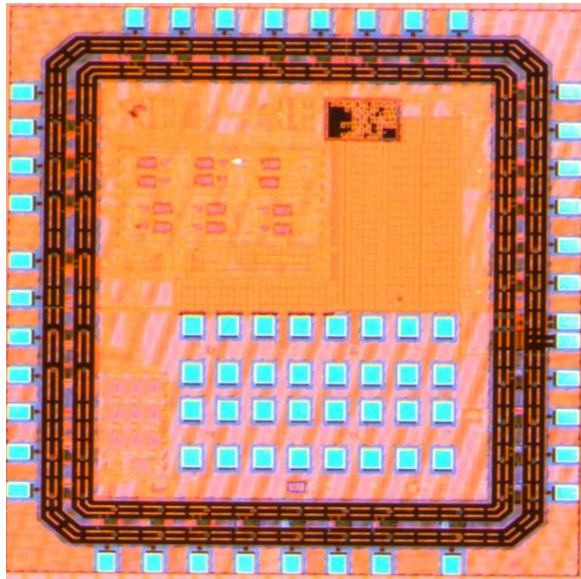


Figure 2.9: Proposed rad-hard design (a) transistor – level latch and (b) full flip-flop design

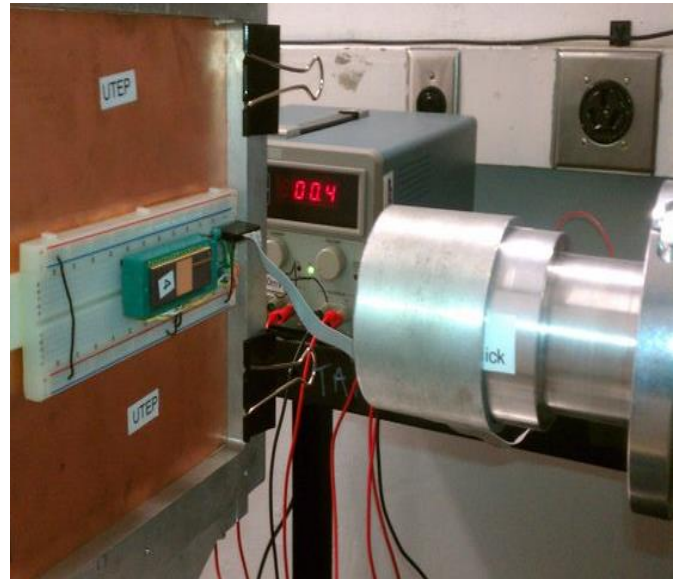
keeping the least amount of stacking. Although the Sense Amp provides the minimal clock capacitance compared to the proposed design, the limited stacking shown in figure 2.9(a) provides a subthreshold advantage relative to the RSAFF, which includes three transistors stacks. The DICE has two transistors stack also, but is affected by the Transient Fault Window of Vulnerability (TFWOV).

Fabricated Hardware and Heavy Ion Characterization

All four flip-flops were fabricated with the Lincoln Labs process and Figure 2.10(a) illustrates the dice photo. A test setup was developed and built that writes and reads alternating data and reports an error when a mismatch is found. The setup was run for several days continuously for reliability prior to traveling to the A&M to show correct operation in the absence of radiation. A serial connection was used to report data in real time to a control computer located in the data room above the radiation chamber – a significant distance to provide safety measure given the dangerous health aspects of the heavy ion generator. The traditional and DICE flip-flops failed whereas the proposed never failed during the radiation study. The proposed design operating in subthreshold (250 mV) showed an improvement in performance by 31% and reduction in energy consumption by 27%.



(a)



(b)

Figure 2.10: (a) Test chip fabricated for soft error characterization and (b) Cyclotron setup

2.5 CONCLUSIONS

This chapter presented an overview of low power techniques, subthreshold operation and implementation and the irradiation of Ameet Chavan's proposed rad-hard design. The topics covered in this chapter form a basis for the discussion of the dissertation work. The proposed work uses low power techniques and uses rad-hard circuits described in this chapter. The rad-hard flip-flop designed by Ameet Chavan was implemented by Praveen Palakurthi and along with Dr. Eric MacDonald – all flops were evaluated at Texas A&M's Cyclotron Institute.

Chapter 3: Subthreshold Level Shifters

3.1 INTRODUCTION

With the proliferation of battery-powered electronics, power consumption has become one of the most important considerations in circuit design. Of the many techniques to reduce the energy per operation, one common technique is to leverage multiple voltage supplies and isolate circuits that are required to operate with high performance. Applications benefit by operating the non-critical circuits at a low supply voltage, while the high performance circuits run at a higher voltage. Recently, subthreshold operation ($V_{dd} < V_{th}$) has become a popular method of achieving extremely low power operation [36-38]. Operating below the threshold voltage results in lethargic performance, however this is acceptable if confined to low performance functions. The intersection of subthreshold operation and voltage island methodologies is a particularly efficient operating domain; however, to interface subthreshold voltage to high voltage circuits, unique level shifters are required that can shift between extreme voltages [39]. Beyond voltage islands, sub to super-threshold level shifters are also required to interface circuits running at subthreshold voltages with IO pads that communicate with the outside world at traditional levels.

Circuits running at these low voltages are less robust to noise and radiation, which can unintentionally alter the circuit operation. The effect is more severe in sequential circuits such as flip-flops, latches and memories as the radiation can remove or introduce additional charge held at a node – resulting in a transient voltage pulse – which can flip a stored bit. The stored data is corrupted if the charge exceeds the node critical charge (Q_{crit}). The Q_{crit} value is the metric for robustness - cells with higher values are more difficult to corrupt. The amount of intentional charge stored on a node depends on the node capacitance and the supply voltage and is given by $Q_{crit} = C_{node} \times V_{dd}$. Therefore with each new CMOS technology, the sensitivity to radiation in the subthreshold region become more pronounced as the critical charge decreases with both the supply voltage and node capacitance.

Conventional level shifter circuits include a half-latch design as shown in Figure 3.1 (a). The signals V_{sub} and V_{sub_b} are provided to the gates of NMOS transistors MNz1 and MNz2

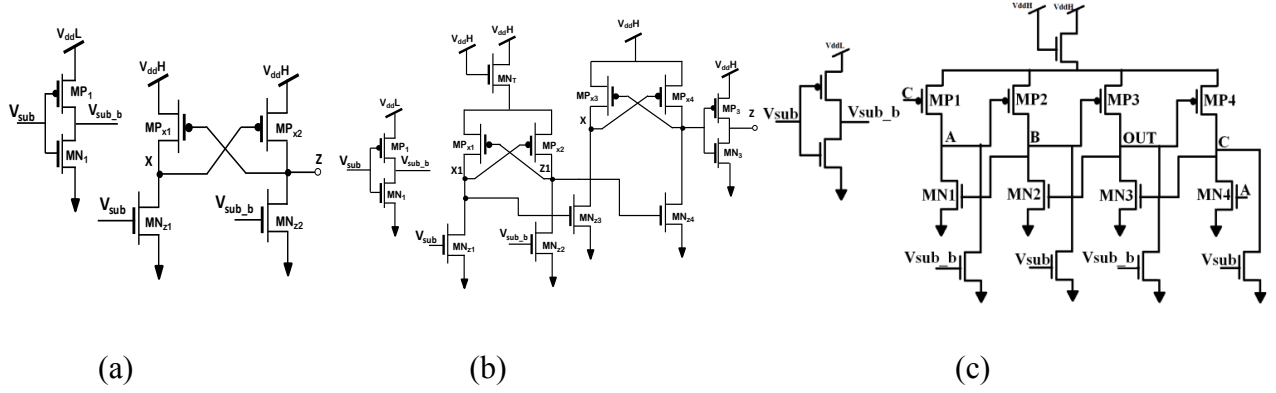


Figure 3.1 (a) Traditional Half-Latch based level converter (THL) (b) Traditional Two-Stage level converter (TTS) and (c) Proposed Rad-Hard level converter

respectively. In the design PMOS transistors MPx1 and MPx2 form a half-latch circuit. Therefore, the design is known as the Traditional Half-Latch based level converter (THL). The below subthreshold, the pull down network - weakened in drive strength in subthreshold - is incapable of over-driving the pull-up half-latch PMOS network operating in super-threshold.

The traditional half-latch level converter does not operate with a subthreshold input with regular transistor sizing. In order to function properly, the NMOS to PMOS ratio should be increased substantially to allow the crippled subthreshold transistors to overdrive the latch with little more than leakage. However, such transistor sizing is impractical often requiring exponentially increased sizings and several solutions have been proposed to address the transistor ratio issue. One of the solutions is to weaken the half-latch PMOS pull-up network rather than increasing the NMOS transistor widths.

[40] proposed a design that consists of two stages as shown in Figure 3.1(b) – a Traditional Two Stage level converter (TTS). A diode connected NMOS is added to degrade first stage supply voltage. Therefore, the voltage supply provided to the PMOS pull-up network of the first stage is changed from V_{DD} to $V_{DD} - V_T$. The second stage is a simple converter to restore the output to full voltage swing. For proper operation at stage one of the TTS level converter, [41] combined multi-threshold devices and subthreshold circuit methodologies. High V_T devices are used to reduce dynamic power consumption and leakage current for off devices whereas low V_T devices

are used to increase drive current of subthreshold devices as required to over-drive the super-threshold transistors. Moreover, size of the transistors in a device operating at subthreshold are adjusted modestly to overcome any further current imbalance. Additionally, a NMOS diode is used to weaken the PMOS pull-up network.

Many other level shifter circuits have been reported [42-46], but none are discussed in terms of radiation sensitivity. The traditional level converters use a half-latch design. In this proposed design the popular rad-hard design Dual Interlocked storage Cell (DICE) [47] is adopted. The DICE design operates on the principle dual node feedback control to achieve upset immunity. The design contains four nodes and the logic state is controlled by two feedback nodes located on previous stages.

3.2 PROPOSED RAD-HARD LEVEL CONVERTER

The primary challenge of the wide voltage level converters is the difference in drive strengths between the pull-up PMOS transistors and pull-down NMOS transistors. Several solutions have been proposed to address this issue either by weakening the pull-up PMOS transistor drive strength or increasing the drive strength of the pull-down NMOS transistor. In this design, the traditional two-stage level converter that weakens the pull-up PMOS transistor drive strength is adopted. In addition, only the first stage of the two stage traditional level converter is considered and the DICE rad-hard design is implemented on this design to provide upset immunity. The design is shown in Figure 3.1(c).

The proposed design consists of two cross-coupled inverter latches. Transistors MN1-MN4 and MP1-MP4 forms the cross-coupled inverter latches. The feedback is given from the previous node to the redundant node. The input to each of the four storage nodes is provided through the NMOS pull-down network. Transistors MN1-MN4 provides a discharge path necessary to eliminate charge collected at each node due to a radiation strike.

3.3 SIMULATION RESULTS

The proposed and traditional level converters were simulated in 250nm TSMC CMOS technology for consistency. The level converter circuits are simulated using HSPICE and subthreshold input supply voltage of 450 mV (V_{ddL}) is used for testing. The high supply voltage (V_{ddH}) of 1.5 V was chosen. All circuits were simulated with the same stimulus and the delay and energy consumption was measured. All circuits were loaded with a 100 fF capacitor and inputs were interfaced with a buffer with identical sizing to get some realistic inputs and to provide a fair comparison. Table I shows the performance of the existing and proposed level converters in terms of transistor count, energy consumption and delay at 450 mV low and 1.5 V high voltages. The traditional level shifters and proposed rad-hard level converters are operated at 100 KHz.

The traditional level converters with typical transistor sizings failed to function with subthreshold inputs. The output was at logic '0' regardless of the subthreshold input; however, by sizing the NMOS pull-down transistors sufficiently strong enough, the traditional level shifter could be designed to work. However, increasing the size of the pull-down network not only increases the energy consumption and circuit area, but also degrades the performance by overloading subthreshold inputs and was considered unrealistic.

As circuit become more susceptible to soft errors with each new generation of CMOS technology, if the amount of charge stored at the node exceeds the Critical charge (Q_{crit}) then soft errors will occur. To measure the Q_{crit} of a circuit a current source is inserted between each sensitive node and ground. Particle strikes create a current spike and hence in simulation a current source with peak for the charge collection and a slow decaying tail representing the charge diffusion was simulated. [48] Describes the impact with a double exponential current pulse as shown in Eq. 3.1.

$$I(t) = \frac{Q_{total}}{\tau_f - \tau_r} \cdot (e^{t/\tau_f} - e^{-t/\tau_r}) \quad (3.1)$$

The simulated results of the traditional two stage level shifter and proposed rad-hard level shifter is shown in Figure 3.2. From the simulated results, the two-stage level shifter value is corrupted at a 10 pC Q_{crit} value whereas the proposed design showed correct operation injected charge as high as 120 pC. However, the DICE cell exhibited vulnerability as discussed in [49], which was observed in the proposed rad-hard level converter as well. The proposed design exhibited approximately twelve times improvement in Q_{crit} values; however, this improvement comes at the price of degradation in energy and delay. The Energy-Delay Product (EDP) provides the better comparison between the designs. From Table 3.1, the proposed design has better EDP values than the THL (due to the unreasonable sizings required) and increased six times when compared to the TTS. Although the TTS performed better in EDP, the circuit is susceptible to failure due to radiation.

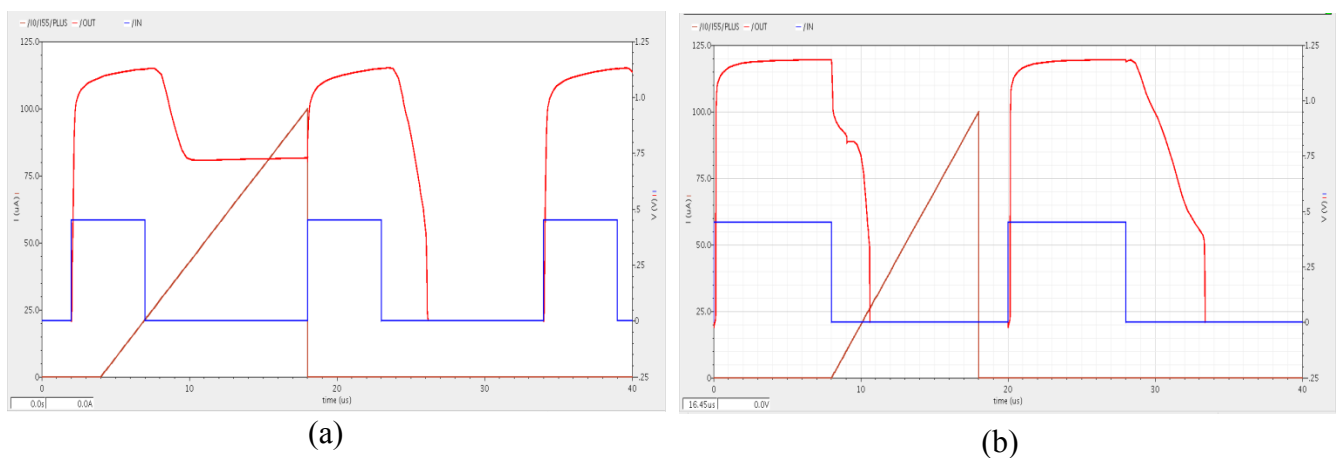


Figure 3.2: Transient simulation of (a) Traditional Two stage level converter (b) Proposed Rad-Hard Level Converter

Table 3.1: Level Converter Circuits Comparison

| $V_{DDL} = 450 \text{ mV}$, $V_{DDH} = 1.5 \text{ V}$ Subthreshold input signal frequency – 100 KHz without Radiation | | | | |
|--|-----------------------|-------------------|-----------------|---------------|
| Circuit | Number of Transistors | Total energy (pJ) | Avg. delay (us) | EDP (pj)*(ns) |
| THL | 6 | 123.7 | 4.756 | 0.588 |
| TTS | 13 | 13.35 | 2.406 | 0.032 |
| Rad-Hard | 15 | 60 | 3.212 | 0.192 |

3.4 CONCLUSIONS

In this report rad-hard level converter circuit is proposed, which is optimized for subthreshold operation for input levels of 450 mV. In contrast to existing subthreshold circuits the proposed design is less sensitive to radiation effects. The proposed level converter has been assessed for critical charge, power consumption and delay using HSPICE. From the simulation results at 450 mV the proposed design maintained typical transistors sizing and had approximately twelve times improved Q_{crit} values. This improvement however, comes at the expense of a six fold increase in EDP compared to TTS due to the addition of feedback paths.

Chapter 4: Digital-to-Analog Converter

4.1 DATA CONVERTERS

Signals in nature are in analog form [53]. As the scaling of submicron CMOS technologies has been beneficial to digital circuits, processing of signals in digital form reduces the overall power consumption of the chip and has resulted in increased insensitivity to noise. Therefore, a motivation exists to process analog signals in the digital domain as early as possible in the signal chain requiring digital to analog conversion. Similarly, the digital signals are eventually required to be converted into analog form for reintroduction to the outside world (analog audio to speakers for example). The devices that convert analog to digital and digital to analog are Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) respectively. The ADCs / DACs are required at the front and back end of most signal processing chains. For example, in a Digital Signal Processor (DSP), a requirement exists for processing analog signals initially prior to conversion to the digital domain. Recently, biomedical applications have begun to demand the inclusion of low power data converters to process the analog biomedical signals that describe the natural function of the body. These wearable or implantable devices detect, monitor and evaluate these signals. Biomedical devices or related unattended wireless sensors generally operate on battery power and battery lifetime depends primarily on the power consumption of the IC, the largest component of which is often due to the data converters.

The present work is, therefore, has focused on studying the data converter architectures suitable for high resolution, low power applications. Also, the effect of accuracy, layout, speed, power supply noise and PVT variations is also studied. Accuracy and matching have become important as the transistor size is decreasing rapidly for new CMOS technologies and the need for faster analog circuits has increased. The layout techniques are studied carefully to reduce the mismatching between the circuit elements [54]. Moreover, while process variation does not impact digital circuits significantly, analog circuits are designed to a specific technology and even

variations across the die can result in incorrect operation. Furthermore, any change in threshold voltage or capacitance can result in a change of bias current (drain current) exponentially in ultra-low voltage operation. Finally, beyond the focus on the analog circuits, maintaining or improving the robustness of the required digital sections will be explored as well.

4.2 THE IDEAL DIGITAL-TO-ANALOG CONVERTER

The general operation of DACs is to convert digital numbers into series of pulses with frequency depending on the input digital number. DAC uses a reconstruction block at the output to convert the pulse stream to analog form. Figure 4.1 describes a general case of a DAC with reconstruction and includes their inputs and outputs. For example, in Delta Sigma DAC the filter and in Charge sharing DAC the sample and hold circuit behaves as reconstruction block. In both cases, the reconstruction block is used to obtain smooth analog output.

The analog output of a DAC could be a voltage or current. The most preferable output in

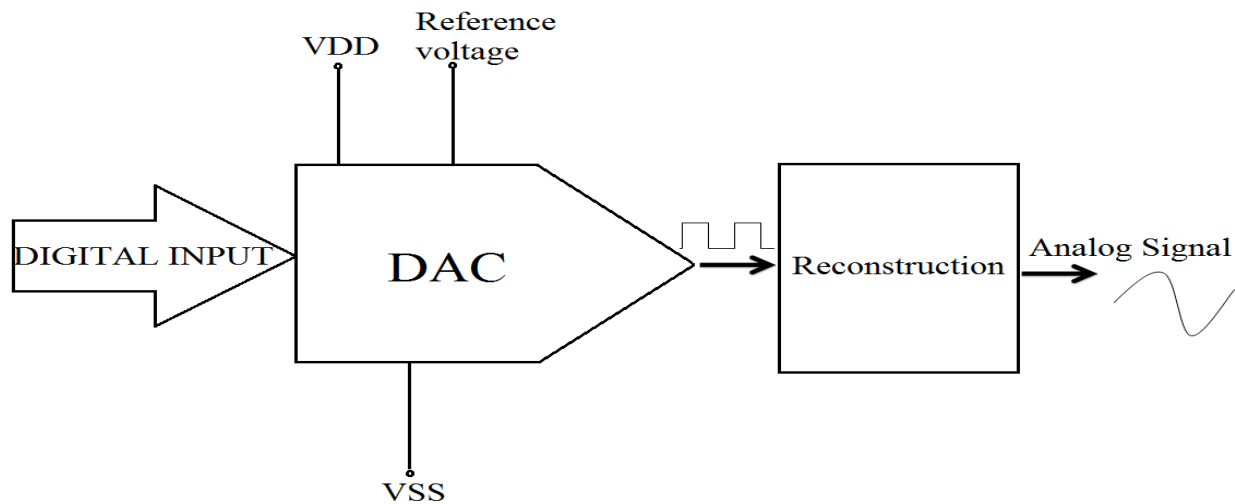


Figure 4.1: Ideal DAC

industry is in voltage form and the analog voltage output of a DAC is represented as a fraction of reference voltage (V_{ref}) and is defined as

$$v_{out} = \alpha * V_{ref} \quad (4.1)$$

where α is the fraction of V_{ref} to be seen at the output calculated as

$$\alpha = [b_0 2^{-1} + b_1 2^{-2} + \dots + b_{n-2} 2^{-n-1} + b_{n-1} 2^{-n}] \quad (4.2)$$

In Eq. (2.2) b_0 is the MSB and b_{n-1} is the LSB and all the elements are 0 or 1.

4.3 TERMINOLOGY

Resolution is the basic parameter in a data converter, which is specified by n the number of bits in the digital input. The resolution is defined as “the number of analog levels corresponding to the different digital words [51].” The resolution of an ideal DAC indicates the number of uniform quantized steps. The N bit resolution indicates that the DAC represents 2^N different analog levels. The value of a single step is the unit of measure for data converters, which is defined as LSB. The weight of an LSB equals the full scale range of a converter divided by 2^N , where N is the resolution and is define as

$$LSB = \frac{V_{ref}}{2^n} \quad (4.3)$$

According to Eq. (4.2) α cannot be equal to one. An infinite number of bits would be necessary for α to be 1. Therefore, a measure of how close the analog output can be to V_{ref} is needed. In ideal DAC V_{ref} is the full-scale. The relationship is called the full scale range (FSR) and is given by

$$FSR = V_{ref} - LSB \quad (4.4)$$

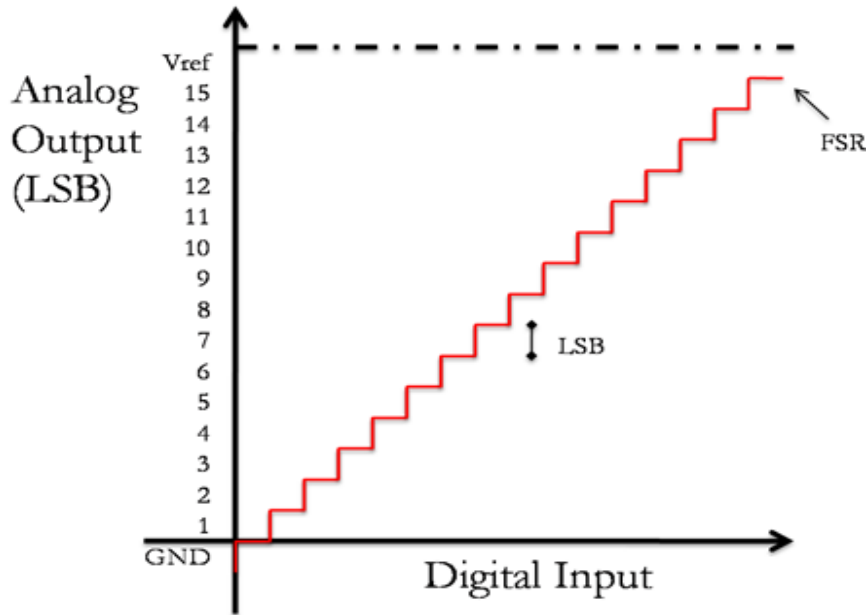


Figure 4.2: Ideal Input vs Output of a 4 bit DAC with a vertical shift of $\frac{1}{2}$ LSB [55]

Figure 4.2 is a plot of the input-output characteristic of 4-bit DAC. 4 bit digital input results in 16 uniform steps and that each binary word corresponds to a unique analog output value. FSR in Eq. 4.4 represents that each step is off by 1 LSB. The difference between the actual analog value and the measured analog value results in a concept called quantization error or quantization noise. The separation is never greater than $1LSB$ and can be designed to be $\pm 1/2LSB$ as a result of shifting vertically the input-output behavior of the converter. The quantization noise can be expressed as

$$Q_{noise} = \frac{LSB}{\sqrt{12}} rms \quad (4.5)$$

The other common terminologies used are zero scale, full scale, and midscale. Zero scale is represented by all zeros (00...0000) whereas full scale is represented by all ones

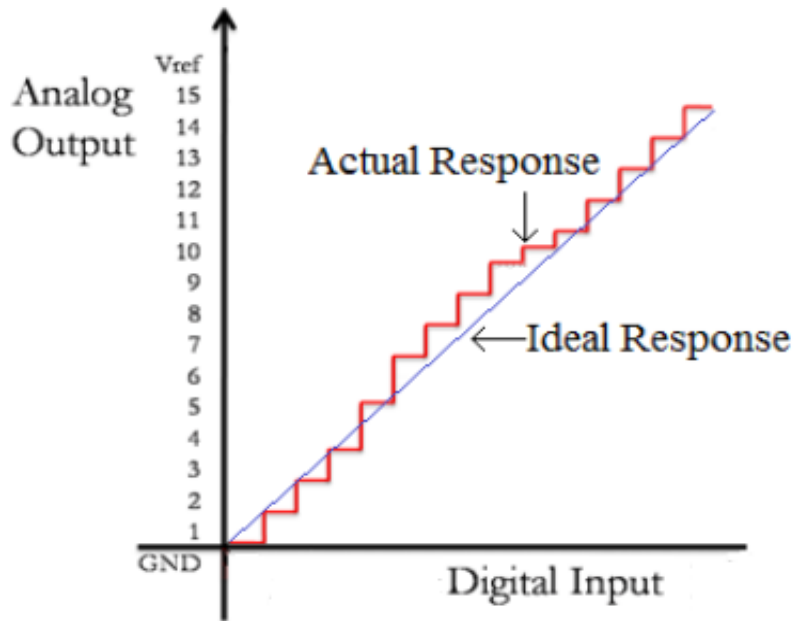


Figure 4.3: DAC Static Errors

(11...1111). Midscale is represented by one (the MSB) and followed by all zeros (10....0000). These terms are used in calculating the sampling rate of the DAC.

4.4 STATIC PARAMETERS

Practical DACs deviate from Ideal DACs. The static parameters represent the deviation at a fixed value [55] and the ideal response is usually a straight line whereas the practical response is a step stair form. Figure 4.3 represents the ideal and practical responses. The difference in the responses gives the static error.

4.4.1 Offset Error

The offset error, or zero scale error, is the difference between the ideal analog output and the actual analog output of a DAC at zero scale

$$E_{offset} = \frac{\tilde{v}_{out}}{LSB} \Big|_{b_{n-1}} \quad (4.6)$$

The offset error describes how well the actual DAC matches the ideal DAC at zero scale.

4.4.2 Full Scale Error

The full scale error is the difference between the actual full scale value and the ideal analog full scale value. The full scale error is similar to E_{offset} but this parameter is commonly evaluated at the MSB. Full scale error is the sum of offset error + gain error.

4.4.3 Full Scale Gain Error

The full scale gain error is the difference between the actual out span and ideal out span. The actual output span is the difference between the output when all inputs are set to 1s and output when all inputs are set to 0s. The Full scale gain error changes with changes in reference voltage V_{ref} .

4.4.4 Gain Error

The gain error shows how close the practical and ideal DACs match. Gain error measures the error on the slope of an actual transfer function of the converter and can be defined as:

$$E_{gain} = \frac{\tilde{v}_{out}}{LSB} \Big|_{b_0} - \frac{\tilde{v}_{out}}{LSB} \Big|_{b_{n-1}} - 2^n - 1 \quad (4.7)$$

Or more conveniently as:

$$E_{gain} = E_{full-scale} - E_{offset} \quad (4.8)$$

4.4.5 Differential nonlinearity error

Differential nonlinearity (*DNL*) error is the difference between the ideal and actual responses for successive input codes. In other words, DNL describes the uniformity of the step size through the entire combination of the digital inputs. A *DNL* value can be computed as:

$$DNL_k = \tilde{v}_{out}|_{k+1} - \tilde{v}_{out}|_k - LSB \quad (4.9)$$

where k is the index of the digital input applied.

4.4.6 Integral nonlinearity error

Integral nonlinearity (*INL*) error describes the deviation of actual analog output to the ideal analog output. The calculation of *INL* for the k digital input is:

$$INL_k = \tilde{v}_{out}|_k - v_{out}|_k \quad (4.10)$$

The above expression yields an absolute value of *INL*. However, the standard practice is to compensate the offset and gain errors before calculating *INL*. Compensation is done with a best-fit line or an end-point line.

4.4.7 Monotonic

Monotonicity is defined as how every change in the digital input ought to result in a change in the analog output in the same direction. A DAC is monotonic if the output increases with the increase in DAC code. Monotonicity is ensured if the relative *INL* can be confined to:

$$|INL_k| \leq \frac{1}{2} LSB \text{ for all } k \quad (4.11)$$

4.4.8 Dynamic Parameters

Dynamic parameters describe the deviation of measured analog output from the ideal analog output with varying time [16]. Dynamic conversion errors are as important and are mostly dependent on the signal frequency.

4.4.9 Settling time

This is the amount of time the DAC takes to settle to within $\frac{1}{2}$ LSB of the final analog output value as a result of a change of the digital input value. The maximum settling time occurs at half scale when the MSB changes. Also, to calculate the maximum sampling rate of a DAC from the settling time the following equation is used:

$$samplingrate (max) = \frac{1}{settlingtime} \quad (4.12)$$

4.4.10 Glitch Energy

During transitions of the digital input a short impulse may appear momentarily at the analog output. The impulse is caused by a time mismatch in the bit transitions. The glitch energy represents the area under the inducted pulse and is measured at half scale in units of volts-second

4.4.11 Signal-to-Noise Ratio

The Signal-to-Noise Ratio (SNR) is the ratio of the root-mean-square (*rms*) value of the output signal to the rms value of the quantization noise. The SNR is expressed as:

$$SNR = \frac{v_{out}rms}{Q_{noise}rms} \quad (4.13)$$

For the reconstruction of sine wave the maximum *SNR* is defined in decibels (dB) as:

$$SNR_{max}dB = 6.02n + 1.76 \quad (4.14)$$

If the reconstructed signal is a triangle wave then:

$$SNR_{max}dB = 6.02n \quad (4.15)$$

4.4.12 Total Harmonic Distortion

The Total Harmonic Distortion (THD) is calculated by taking the ratio between the root-mean-square of the signal and the root-mean-square of the harmonics [17]. THD represents the distortion of a signal other than noise.

4.4.13 Signal-to-Noise-and-Distortion Ratio

The Signal-to-Noise-and-Distortion Ratio (*SNDR*) is the ratio of the root-mean-square (rms) value of the output signal to the root-sum-square value of the quantization noise including AC harmonics. The SNDR depends on the input frequency of the intended signal.

4.4.14 Dynamic Range

The Dynamic Range (*DR*) is the value of the analog output at which *SNR* and *SNDR* equal to 0 dB. The expression to calculate *DR* is:

$$DR_{dB} = 6.02n \quad (4.16)$$

4.4.15 Effective Number of Bits

For a full scale sinusoidal reconstruction *ENOB* is determined by:

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02} \quad (4.17)$$

The *ENOB* value provides a valuable metric to directly compare DAC implementations.

4.4.16 Spurious Free Dynamic Range

The Spurious Free Dynamic Range (*SFDR*), measured in dB, is the difference in power between the output signal and the largest spur present in the frequency spectrum.

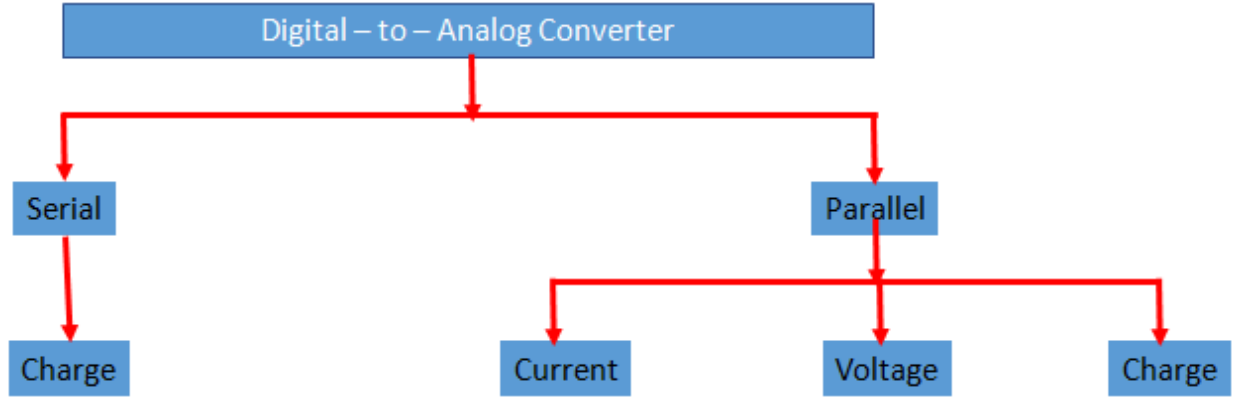


Figure 4.4: Classification of Digital-to-Analog Converters

4.5 DAC ARCHITECTURES

In this chapter the basic DAC architectures are reviewed. DACs are categorized based on how long it takes to perform the conversion [57]. DACs are basically classified into a dichotomy between serial and parallel architectures. Serial DACs convert the analog output one bit at a time. Parallel DACs convert all bits at the same time. Further, DACs are classified by the scaling methods, which include current scaling, voltage scaling, and charge scaling.

4.5.1 DAC Performance

Selecting a DAC for a specific application depends on the requirements of the application. $\Delta\Sigma$ DACs contain more digital circuitry, which can be operated at subthreshold levels and thus improve power efficiency at the expense of performance. However, $\Delta\Sigma$ DACs require a low pass filter at the output to convert the pulse train into a smooth analog form. Even though some part of the $\Delta\Sigma$ DAC is implemented at subthreshold the total power still remains approximately same as the analog backend dominates the total consumption. Moreover, the $\Delta\Sigma$ DAC has a low data rate particularly when running at low voltage. The charge redistribution DAC architecture was chosen in this proposed work because of its overall low power consumption, high resolution and high speed. The comparison between the DAC architectures is shown in Table 4.1 [2-3].

Table 4.1: DACs Performance Comparison

| Parameters | $\Delta\Sigma$ DAC | Voltage Scaling | Charge Sharing | Current Steering |
|-----------------------------|--------------------|-----------------|----------------|------------------|
| Linearity | High | High | High | Low |
| Speed | Low | Medium | High | High |
| Power | Low | Low | Low | High |
| Noise | Very Low | Low | High | Medium |
| Digital Elements Density | High | Low | Low | Low |

4.5.2 Charge Redistribution

A charge DAC is constructed with a capacitor bank. Charge scaling DACs operate by logarithmically dividing the total charge on a capacitor array. The charge scaling DACs are popular for low power designs because the static power consumption is close to zero – with only static power from the very low capacitor leakage. Another advantage of this architecture is that it is compatible with switched capacitor circuits.

A binary weighted array of capacitors is used to attenuate the output voltage by distributing the charge present at each capacitor. A 4-bit implementation is shown in Figure 4.5. The switching logic is typically done with NMOS pass transistors with complementary input signals. The Nonlinearity of a charge DAC is caused by three sources: capacitor mismatch, inherent capacitor nonlinearity, and parasitic junction capacitance from any MOS switch connected at the output node. A buffer is connected to the output of Figure 4.5

The architecture represented in Figure 4.5 has a floating capacitor ‘C’. After a few minutes, the capacitor array starts unintentionally discharging which in turn increases the nonlinearity of the DAC. Therefore, reducing the leakages in the capacitor array is important and the charge state of the capacitor needs to be calibrated periodically. Furthermore, increases in

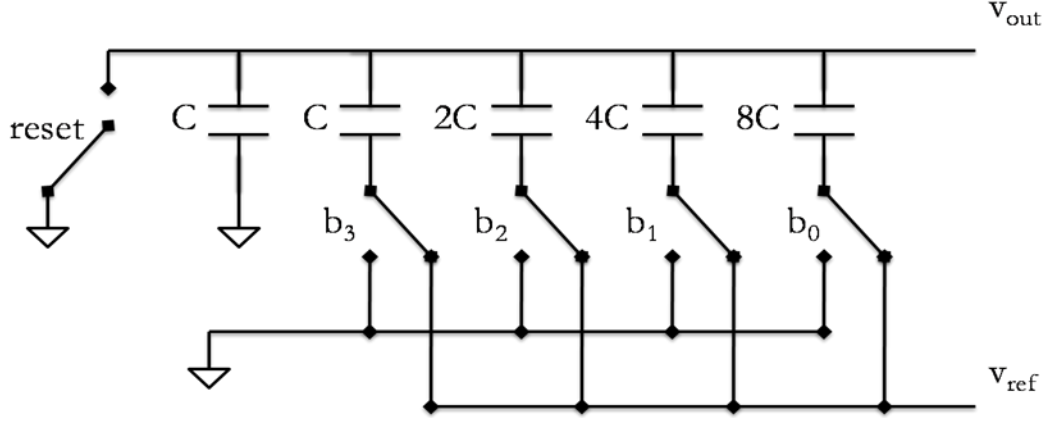


Figure 4.5: Charge Redistribution Architecture

this type of DAC resolution increase the DAC area. For example, for 12-bit charge redistribution DAC the maximum capacitor value is 2048 times the minimum capacitor. Also, an increase in resolution (and consequently capacitor sizes) increases mismatches between the capacitors.

Several solutions were proposed to reduce the mismatches by reducing the MSB to LSB capacitor ratio. One of the solutions is to combine DACs using similar scaling methods. Figure 4.6 shows a 12-bit charge scaling DAC by combining two 6-bit charge scaling subDACs. This DAC reduces the MSB to LSB component capacitor ratio. The scaling of the LSB subDAC is achieved through the capacitor C_s . The series combination of scaling capacitor C_s and the LSB array must terminate the MSB array as shown in Eq 4.18.

The accuracy of C_s influences the MSB array as well as the LSB array. However, the accuracy of C_s is hard to achieve if the equation 4.18 solves the value of C_s to a fraction. Therefore, a new charge distribution DAC is proposed to reduce the capacitor array leakages, reduce the area that in turn reduces the mismatches and reduce the power. The proposed design is described in the next chapter. Several layout architectures were studied to reduce the mismatches and improve the accuracy.

$$\frac{C}{8} = \frac{1}{\frac{1}{C_s} + \frac{1}{2C}} \quad (4.18)$$

4.5.3 Proposed Chip with two novel low power DACs

The design submitted to fabrication in late 2011 contains a Serial-to-Parallel (S2P) converter, 8-bit Delta-Sigma DAC and 12-bit Charge Redistribution DAC. The S2P block is included because of the restriction on IO pins and its main purpose is to convert serial input to parallel to drive two parallel DACs. The supply voltage is isolated from each design for power measurement. The block diagram is shown in Figure 4.7.

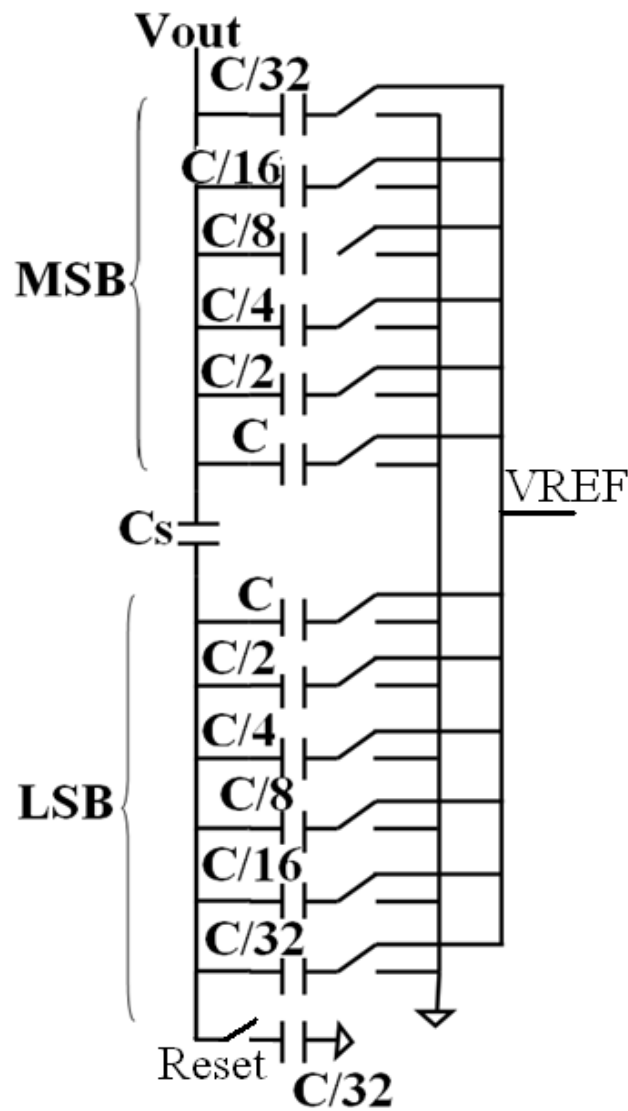


Figure 4.6: Combination of two, 6-bit Charge Scaling subDACs to form a 12 bit Charge Scaling DAC

Subthreshold operation of electronics offers significant advantages over traditional approaches for applications in which energy per operation is paramount. However, the majority of recent attention has been focused on digital circuits in which functionality is limited to simple Boolean switching, and although subthreshold voltage levels reduce performance, functionality can be provided with a dramatic improvement in energy efficiency. Analog circuits are more difficult to implement at subthreshold voltage levels due to a generally more complicated dependency on parameters such as process, temperature and voltage. One potential solution is to target analog systems, which are primarily constructed with digital circuits. As described in background section, the majority of Delta Sigma DAC is digital. Therefore, the 8 bit Delta-Sigma module was considered and designed at subthreshold levels.

4.5.4 Low Power DACs

This section describes the two low power DACs: Sigma Delta and Charge Scaling. This section also compares the results of proposed with traditional level shifters.

Low Power Delta Sigma DAC

The Delta Sigma converter consists of 3 main blocks: $\Delta\Sigma$ digital modulator, level shifter and reconstruction low pass filter. The DAC takes an 8-bits input in order to obtain a corresponding analog output; however, the voltage of the inputs as well as voltage supply for the $\Delta\Sigma$ digital modulator operates at subthreshold levels in order to conserve energy. The level shifter is used to amplify the bit stream voltage of the $\Delta\Sigma$ Modulator to superthreshold levels and a subsequent low pass filter is used to acquire analog output by averaging the digital output signal. The proposed block diagram is shown in Figure 4.7.

The digital section was designed with a contemporary ASIC-style design methodology and with an open source standard cell library targeting TSMC 0.25u CMOS technology. The ASIC digital layout including several hundred transistors was then extracted and simulated with HSpice in order to provide high fidelity simulation. Traditional static timing analysis was insufficient

given the exponential dependence of the drive current in the subthreshold domain and also because the provided library rules were only valid for traditional voltages (2.5 V). Two level shifters were then evaluated in order to provide a graceful transition from sub- to super-threshold levels. One design – a traditional current-mirror level shifter -provided strong performance at traditional voltage levels as well as a stable current driving capability. However, this architecture resulted in high power consumption because of inherent leakage paths during normal operation -particularly at subthreshold levels. Furthermore, as the inputs were driven weakly by subthreshold inputs, the circuit struggled to switch at the output, thus resulting in performance degradation. Alternatively, a second novel design was evaluated that was optimized for sub- to super-threshold operation. As the output current on both levels shifters is not sufficient to drive the large output load, buffers were implemented in order to boost the current capability of the output signal.

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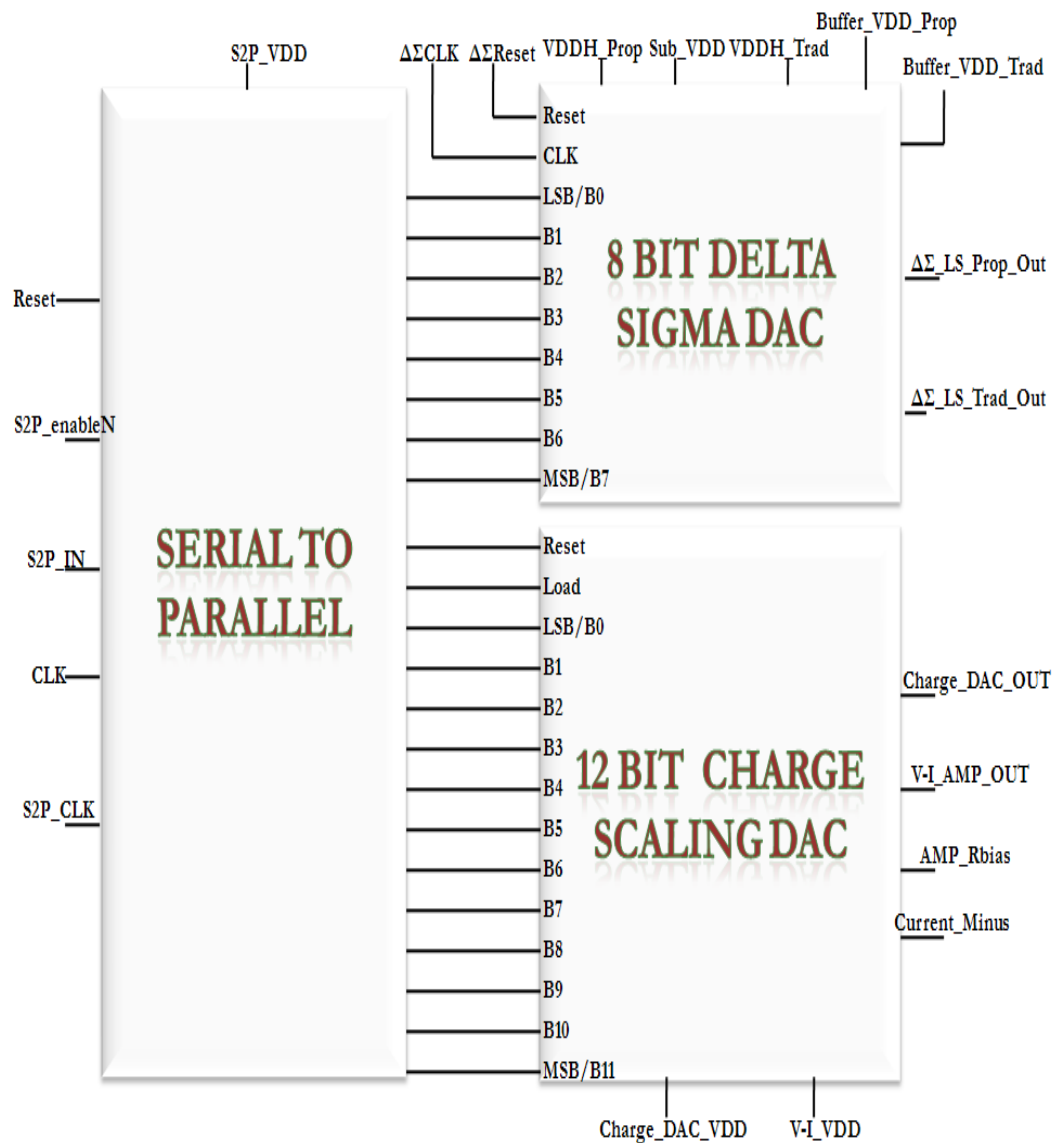


Figure 4.7 – Digital to Analog Converters Block Diagram

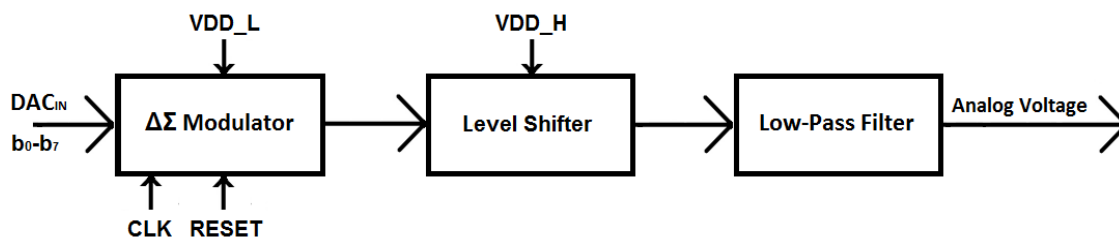


Figure 4.8 – Delta Sigma DAC Block Diagram

DIGITAL DELTA SIGMA MODULATOR

The digital $\Delta\Sigma$ modulator is the core of the $\Delta\Sigma$ DAC. The Digital $\Delta\Sigma$ Modulator is designed in Verilog, which contains an algorithm that executes the fundamental operations of the modulator. Such operations are the delta adder (Δ) and the sigma adder or sigma integrator (Σ), all of which is required in order to obtain the output bit stream the average of which (DC value) provides the analog output. The $\Delta\Sigma$ Modulator is illustrated in Figure 4.9.

The input of the $\Delta\Sigma$ Modulator should be signed. However, the input bit number N is unsigned. Therefore, an extra two bits are added to achieve the input bit number as a signed number. The Δ adder function is to obtain the difference between the DAC input and $\Delta\Sigma$ output; therefore, the Δ feedback to Δ adder is related to the $\Delta\Sigma$ output, which is either 1 or 0. The Δ feedback is an $N + 2$ bit number with all in 0 if the $\Delta\Sigma$ output is 0; the Δ feedback is the 1's complement of the highest N bit number, sign extended to $N + 2$ bit if the $\Delta\Sigma$ output is 1.

Simultaneously the Σ adder operates as an integrator, which accumulates the input at a rate proportional to the magnitude of the input. The Σ adder sums the output of the Δ adder (Δ out) and the current $N + 2$ bit number content in the Σ register, then the output of the Σ adder (Σ out) is stored in Σ register; the $\Delta\Sigma$ output is the MSB of the $N + 2$ bit number stored in the Σ register.

Fig. 4.7 compares the logarithmic power consumption from simulation with respect to the low side supply voltage for the $\Delta\Sigma$ modulator as well as the two alternative level shifters. The

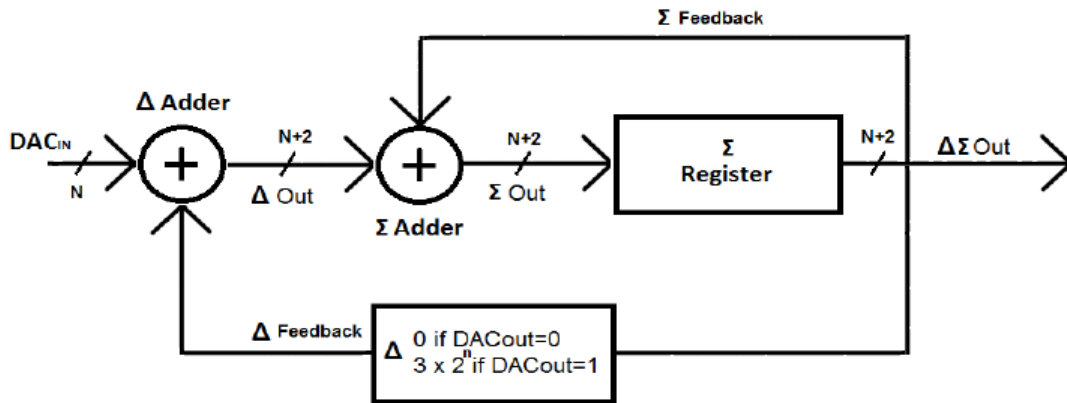


Figure 4.9 – Delta Sigma Modulator Block Diagram

modulator benefits dramatically in terms of energy efficiency (quadratic with supply voltage) due to the subthreshold operation and represents only a small fraction of the total DAC power. Of the two level shifters – one of which is required for providing the superthreshold output – both consume significantly higher power, although at subthreshold levels, the proposed level shifter provided an improvement in both power and performance but failed to operate at superthreshold levels above 700 mV. The traditional level shifter operated across a wider voltage range, which may be necessary for applications that implement dynamic voltage scaling. However, for applications that run exclusively in subthreshold, the proposed level shifter provided substantial energy delay product improvements. The proposed rad-hard subthreshold to superthreshold level shifter is described in next chapter.

Low Power Charge Scaling DAC

As mentioned in the background chapter, the capacitor array charge redistribution DAC area, leakages, and power increases with increase in resolution. Therefore, a new DAC architecture is required to overcome these issues. In this section the proposed design is described to overcome these issues and is shown in Figure 4.14.

Switches are connected to each node to discharge the capacitors before the conversion started. From Figure 4.11, C-2C DAC occupies less area than binary-weighted DAC. The capacitor sizes are fixed therefore the matching problems are reduced. The disadvantage of this architecture is its parasitic capacitance at the intermediate node that changes the capacitor ratios. Therefore, with this change in capacitor ratio reduces the resolution of the DAC. Therefore, a new design is required to improve the resolution.

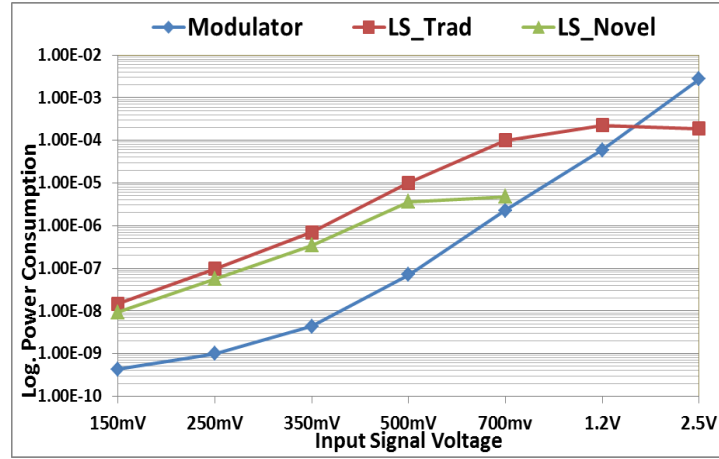


Figure 4.10: Power Consumption

A new DAC is proposed by combining C-2C and Binary weighted DAC, which is shown in Figure 4.14. The binary weighted DAC is connected as the MSB to improve the resolution. Initially, all switches are ON to reset the intermediate nodes and DAC output. In other words all the capacitors were discharged and the outputs were set to zero. After reset, all switches are turned OFF and capacitors are connected either to V_{ref} or to ground depending on the bit. Capacitor is connected to V_{REF} if the bit is 1 and is connected to GND if the bit is 0. However, the improvement in resolution came with the expense in DAC area. The DAC area is increased because of the addition of binary weighted DAC.

A typical layout of a capacitor consists of the overlap of metal-over-metal cap forming a capacitor. In all of these capacitors, the bigger the area of the overlap, the bigger the capacitance is. However, a problem arises when two different capacitors must be matched. Irregular gradients and random errors during the fabrication process reduce ENOB if these issues are not addressed properly. In order to minimize the above effect the layout of matched capacitors is done using common centroid geometries. The unit Capacitor is shown in Figure 4.12. Figure 4.13 shows the layout of complete chip including serial-to-parallel, Sigma Delta DAC, and Charge Sharing DAC.

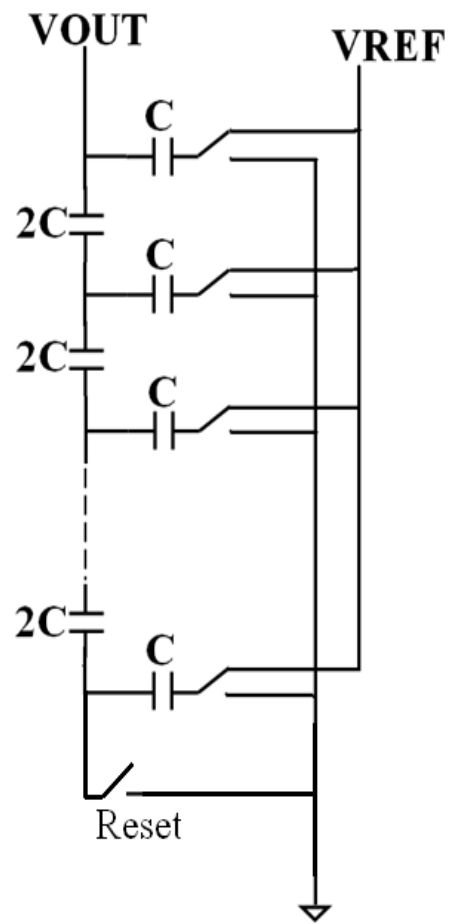


Figure 4.11: C-2C Digital to Analog Converter Architecture

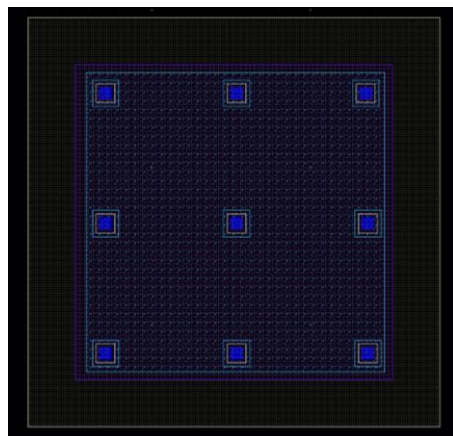
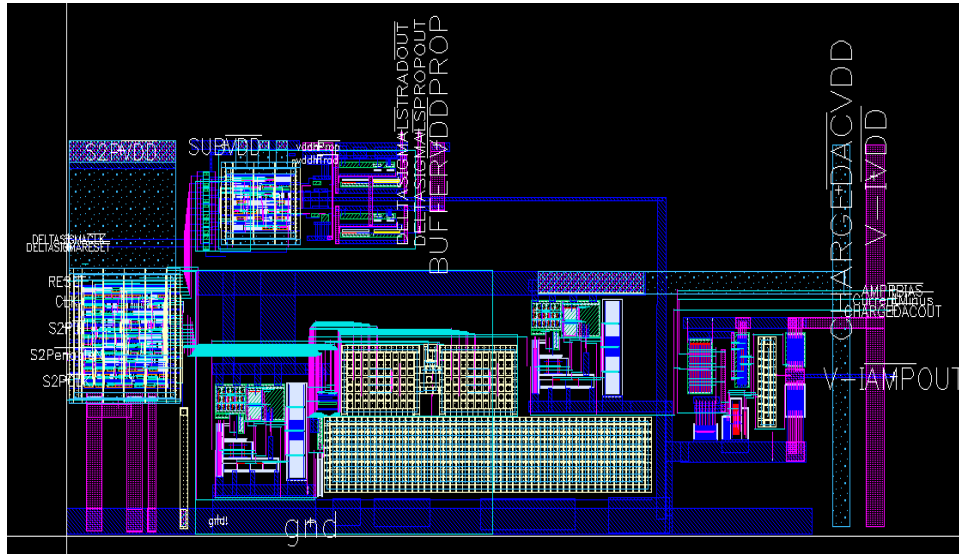


Figure 4.12: Unit Capacitor with 100fF capacitance



4.6 COMPARISON OF PROPOSED DACs WITH EXISTING RESEARCH

4.6 COMPARISON OF PROPOSED DACs WITH EXISTING RESEARCH

Comparison between different DACs is provided in Table 4.2. However, the capacitor leakage issue still is required to be addressed. The future work is to functionally verify the DAC hardware and address the leakage issue with a new DAC design.



Table 4.2: DAC Comparison

| | Current | Miguel [49] | [59] | [60] | [61] | [62] | [63] | [64] | AD7390 [65] | LTC2641 [66] |
|----------------------------|-------------------------------|-------------------|---------------------|---------------------|----------------|----------------------|--------------------------|--------------------------|-----------------------------------|------------------------------------|
| architecture | Improved Charge Scaling | Charge scaling | current steering | current steering | R-2R ladder | Resistor ladder | Resistor String | Current steering | R-2R Voltage DAC | R-2R Voltage DAC |
| bits | 12 | 12 | 10 | 10 | 10 | 10 | 10 | 10 | 12 | 12 |
| Technology | 0.25 μ m | 0.35 μ m | 0.35 μ m | 0.18 μ m | 0.18 μ m | 0.35 μ m | 0.13 μ m | 0.35 μ m | Not Specified | Not Specified |
| Volt. supply | 2.5 | 3 | 2.7 | 1.8 | 1.4 | 3.3 | 1.5 | 3.3 | 3 | 3 |
| Power | 152 μ W | <0.6 mW | \leq 7.8 mW | <22 mW | 4 mW | n/a | 0.5 mW | \leq 0.6 mW | 300 μ W | 0.36 mW |
| Area (mm ²) | 0.5 | 1.5 | 0.23 | 0.35 | 0.01 | 0.022 | 0.18 | 0.18 | Not Specified | Not Specified |
| Speed | 2 μ s | 2 μ s | 30Ms/s | 250M/s | Low freq | 3 μ s/10pf | 2Ms/s | 2 μ s | 70 μ s (\pm 0.1% FS) | 1 μ s (\pm 0.5LSB FS) |
| Output (min– max) | 20mV– 2.49V | 20mV– 2.85 | \leq 2.25mA | \leq 10mA | <2.2mA | Voltage no buffer | Voltage high swing | Voltage high swing | 0to2.4994 | Voltage high swing |

Chapter 5: Data Acquisition Sensor

5.1 BACKGROUND

With the continual geometric scaling semiconductor technology, the energy efficiency of electronics is now sufficient to enable battery-powered, wearable biomedical devices that can serve to monitor crucial physiological signals from our bodies. Recent research has demonstrated wearable portability of various devices for assessing individual psychobiological traits supporting Warfighter performance – with obvious benefits in commercial health monitoring applications as well. However, integration remains a difficult challenge for a system capable of sensing multiple disparate signals into an operational form-factor that is simultaneously sufficiently robust and lightweight while maintaining low cost. A patented [67], revolutionary approach for detecting extremely small electrical signals has emerged from Navy research lab at SSC-PAC - *the Microscale Universal Sensor System* (MUSS) - capable of serving as a platform providing unprecedented sensitivity for unobtrusively collecting a multitude of biological signals required for assessing health, cognitive performance and stress resiliency of a subject.

Traditionally, sensing of physiologic signals has been restricted to non-ambulatory scenarios such as in clinical or hospital environments. Although recent work has demonstrated wearable portability for various individual psychobiological traits [67], it remains a difficult challenge to integrate an entire system capable of sensing and processing multiple signals into a form-factor that is suitable for soldiers in the field. In particular, the relatively large power consumption of the requisite sensing electronics often necessitates physically large and obtrusive batteries for reasonable system operational duration, limiting the usefulness in such applications.

The proposed system will overcome restrictions of size and energy — by implementing sensing functionality via compact microchips that have sufficient precision, scalability and energy efficiency to enable long-term and robust operation from limited energy supplies by exploiting the dynamical properties of nonlinear circuits in a novel and revolutionary manner. Specifically, the sensing system will be comprised of a common integration point using recently filed patent on MUSS technology [68] and an array of specialized non-contact sensing interfaces tailored to

measure heart rate, breathing rate, skin temperature and hydration status through skin conductance (the Electrodermal Response - EDR) in one compact package. Additionally, the same system will be self-configured to measure the Electroencephalogram (EEG) in the frontal lobe area when applied to the forehead area. The individual data will be transmitted wirelessly to a central processing node such as smart devices, (i.e., iPhones and DROID systems), for processing the multi-variable signals and information fusion to assess the individual's health and performance status in real-time

In order to enable seamless and unobtrusive integration of sensing elements into a wearable system, non-contact sensing of bio-potential-based signals (such as Electrocardiogram (ECG) and EEG) will be employed. As opposed to dry or wet electrode sensing, non-contact sensing permits comfortable and flexible electrode placement that can be worn continuously over extended periods of time with little-to-no skin irritation or other complications. Additional benefit to the usage of non-contact sensing is the entire package will be sealed from the environment enabling it to operate in any condition. Although previous work has investigated the electronics design of non-contact sensing [67], there remain challenges in achieving stable and robust physiologic recordings in the presence of subject motion. The proposed design will overcome such restrictions through a number of breakthrough data acquisition techniques, including: (1) coupling capacitance estimation and compensation; (2) differential signal acquisition over wide dynamic ranges; and (3) intelligent back-end digital signal processing and artifact removal.

Signal acquisition itself will be performed by a multi-purpose instrumentation circuit based on the MUSS technology that has sufficient precision and bandwidth to monitor many different vital signs. Specifically, the sensing instrumentation circuits will be composed of N -element nonlinear oscillators (where N is an odd number) that have an intrinsic bi-stable (double-well potential) property which can be tuned, via programmable parameters built into the nonlinear microcircuits, to respond to various signal input characteristics such as varying signal frequencies and amplitudes. Due to the compact nature of the system, many channels (10s to 100s) can be implemented within the millimeter-sized footprint of a single IC, thereby permitting the acquisition

of a large number of physiologic signals in a small form factor sensor interface. An additional benefit of employing this nonlinear circuit is that it provides extensive noise suppression where needed, particularly when assessing bio-signals in a noisy environment, as is the case when collecting data for EEG, ECG, and EDR applications. Furthermore, the sensitivity of the sensing instrumentation circuit can be enhanced by incorporating larger numbers of nonlinear oscillators into the coupling network beyond the minimum required number of $N = 3$ to meet the application requirements. Additional integration into the sensing IC beyond the functionality of the MUSS will be the analog-to-digital converter (ADC) and data compression method to minimize data packet size and transmission time.

Due to the multi-variable measurements and the compact nature of the sensor system, transmission of the pre-processed and compressed physiologic data will be directed to a single common point for processing and will initially be achieved using standard low power protocols (Bluetooth Low Energy or Bluetooth Smart) and eventually adapted to a custom protocol, more appropriate to the transmission scales used here (approximately 1.0 meter or less). Although the communication distance is small, careful link budget optimizations must be considered in the presence of significant fading due to tissue absorption of radiated RF energy. Fortunately, since the typical frequencies of biological signals (1 to 500 Hz) are small compared to available instantaneous radio bandwidths (0.1 to 1 MHz) and RF carrier frequencies (400 to 5400 MHz), energy can be saved by aggressive duty cycling between active transmissions mode and ultra-low power sleep mode. In particular, sending data to the central processor only when meaningful changes occur can save significant additional energy. For example, heart rate monitoring with microsecond accuracy may not be necessary if no significant changes to health status are indicated.

An integrated software/hardware system will manage, decipher and compress the data from biological signals for long-term monitoring over multiple levels of hosts. Locally, the system will clear motion and environment noises via digital signal processing. Vital signs such as the heartbeat and excitation of sympathetic and mental status of the subject will be extracted. The details of the information will be sent to a regional operating system by demand or in convenience, as described

above. One challenge is to distill the data from artifacts caused by muscle, eye motion and surrounding instruments. Therefore, it is essential that we use high density sensors with wide frequency range to provide sufficient data for the nonlinear-based signal processing system to learn and recover the information.

Power for the sensor system will initially be provided by individual batteries included in the sensor packaging. The target operating voltage for the sensor package is 1.5 Volts, which is determined by the largest component in the entire system - the communication link using Bluetooth Low Energy. Ideally the sensor system can operate from a power source of a single compact battery, but this will require a much lower power beyond what is currently required by Bluetooth Low Energy system. The use of “smart” sensor nodes (which only leave low-power mode when collecting data and transmitting to the central processor) will greatly extend battery life.

5.2 MUSS DESIGN

Careful design of overdamped bistable systems can exhibit desirable oscillatory behavior when certain parameters pass a threshold value. The behavior of these oscillations is particularly interesting when external DC and/or AC signals are introduced to the circuit. Depending on the magnitude of the incoming the signal, the circuit will operate in one of three different regions; with the regions of interest for this research are being the synchronization regions [68].

This behavior can be used to detect low-level electric filed signals, which affect the frequency and duty cycle of the natural oscillation of the system. Previous work on such a system employed bipolar junction transistors (BJT's) in order to achieve the nonlinear features and coupling terms modeled by hyperbolic tangent nonlinearities [68]. For a proof a concept and high power applications it was acceptable to design such a system, but for biomedical applications such a system would consume too much power making the device impractical for the use in mobile medical and bio-sensing applications.

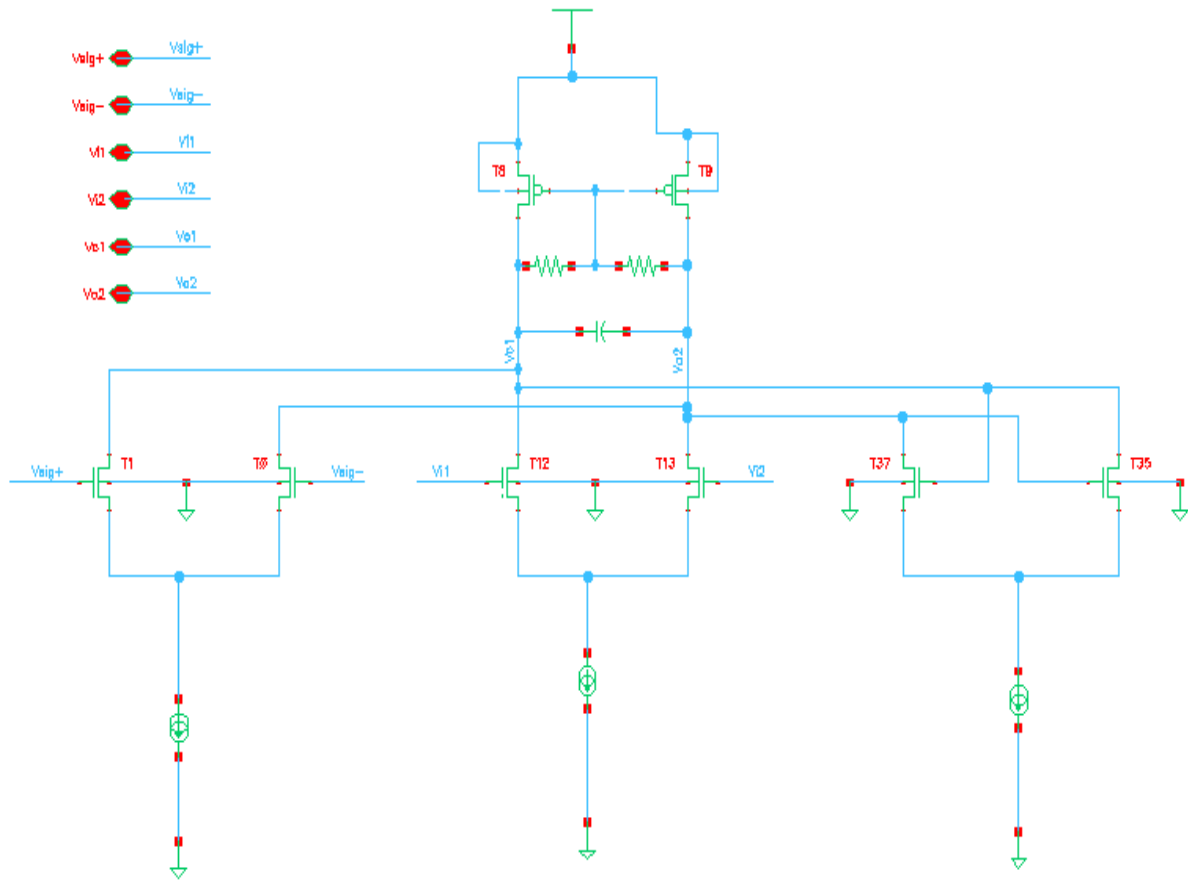


Figure 5.1: MUSS Single element containing differential pair oscillator circuitry, differential pair input signal circuitry and cross coupled pair.

The current work is designed MUSS in IBM's 130nm PDK using Cadence Virtuoso software. In order to design a system to be low power and a system that exhibited the desired nonlinearities it was an obvious choice to implement the design with the same basic architecture of the BJT design, but instead of using BJT devices, using sub-threshold PMOS and NMOS devices. In the sub-threshold mode of operation these devices in an OTA configuration exhibit the same hyperbolic tangent characteristics as the BJT's do, but with different constants associated with the devices due to the process.

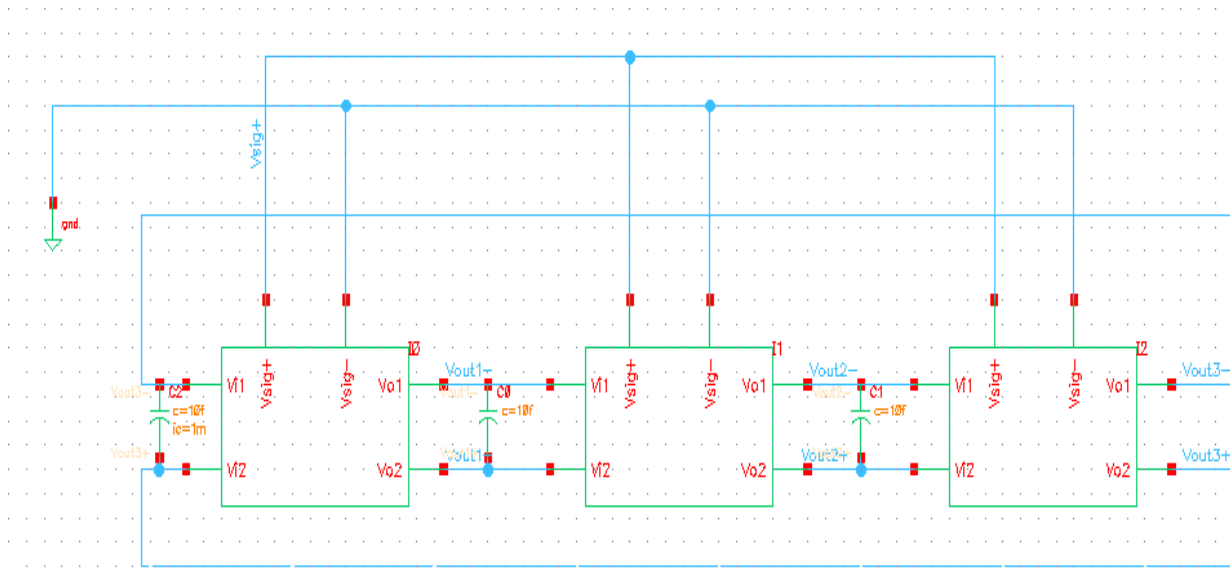


Figure 5.2: Full Circuit Diagram of a Channel

The principal operation of the MUSS is based on a 3 element, unidirectional differential pair ring oscillator architecture. Each element is comprised of three OTA structures with each OTA being controlled by specific control parameters as seen in Figure 5.1. These control parameters are the bias currents I_C , I_S and I_G . The bias current I_C , associated with the differential pair controls the oscillatory behavior of the circuit and the bias current I_S , associated with the crossed coupled OTA sets the low limit of I_C and controls the amplitude of oscillation. One of the main design challenges was determining the values of I_C and I_S and then sizing the OTA transistors to remain in sub-threshold over a range of bias currents.

The entire channel can be constructed by connecting three single element OTAs. Figure 5.2 shows the full circuit diagram connecting three OTAs. The differential outputs of each element connect to the input of next element. The output of each channel is the differential output from each element. The three differential outputs are summed together to obtain the biological signals. ADC is used to convert the summed output into digital bits.

5.3 SIMULATION RESULTS

MUSS is designed at transistor level and then layout has been implemented. The analog design, implementation and simulations has accomplished using Virtuoso Cadence ICFB design environment. The digital block was designed using Verilog Hardware Description Language. Digital layout is performed using Cadence SOC Encounter tool and ARM standard cells has been used. Cadence is an Electronic Design Automation tool that supports the entire design flow from behavioral modeling to post-layout simulations. The design is targeted for IBM 130nm process node.

The implementation of each component is described as follows: each component is implemented at transistor level in the schematic editor and a symbol is created. The symbol is instantiated in a test bench, which provides the stimulus to the component. The component is simulated using ADE through the test bench. The results are viewed in the Waveform Editor and when required, the results are exported to a text file.

The reference voltage of 1.2 V is supplied to the design. ECG signal is provided as the analog input signal. The input electrodes are noncontact and small in size. Therefore, the output signal from the electrodes is in order of 10 pA. MUSS is a sensitive sensor and is designed to detect low strength signals even in the order of picoamperes. The bias currents are calculated and the values are given in Table 5.1.

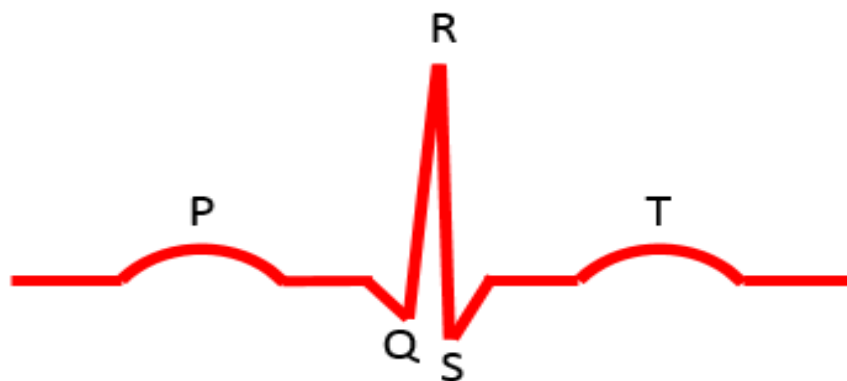


Figure 5.3: A Normal ECG signal showing P, Q, R, S, T, and U

Table 5.1: MUSS Bias Currents

| Bias Currents | In uA |
|---------------|-------|
| I_g | 0.8 |
| I_c | 1 |
| I_s | 1 |

Where I_c determines the natural frequency, I_s determines the amplitude of the signal and I_g is used to lock the input biological signal frequency.

MUSS with ECG input

ECG signal gives the information of electrical activity of the heart. A normal ECG signal consists of events P, Q, R, S, T, and U in a single heartbeat shown in Figure 5.3. The output of a single electrode is in the order of picoamperes. For this design, the input signal is 10 pA peak to peak. The supply voltage for the design is 1.2 V. Figure 5.4 shows the differential output of the channel, sum signal. Figure 5.5 shows the filtered signal.

MUSS with Sine input

In this section, the behavior of MUSS is discussed when sinusoidal signal of 4 Hz and 7 pA peak-to-peak is applied. The sinusoidal signal represents breathing information of a human body. The waveforms are shown in Figure 5.6.

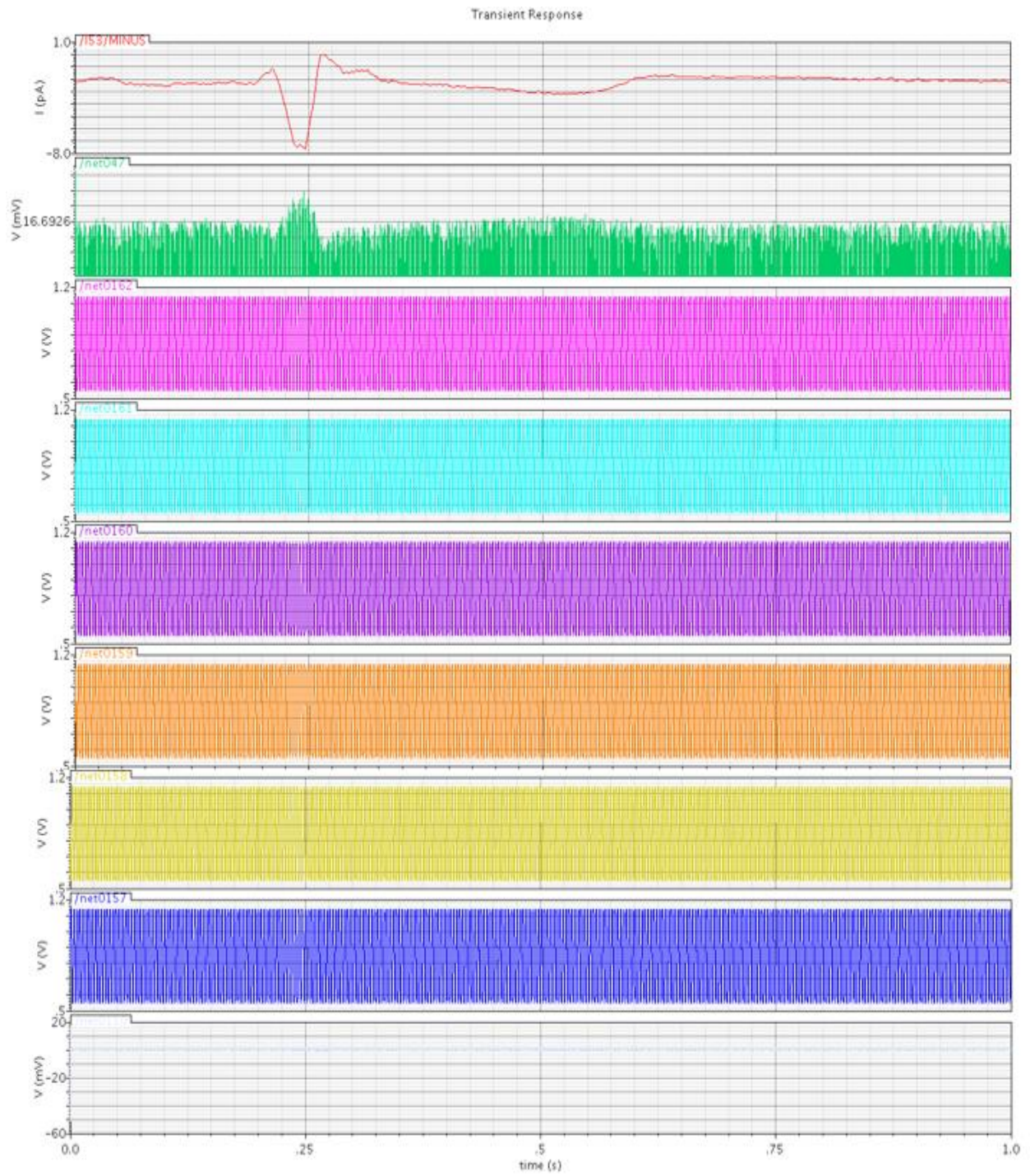


Figure 5.4: ECG signal Output

Figure 5.5: Filtered ECG Output

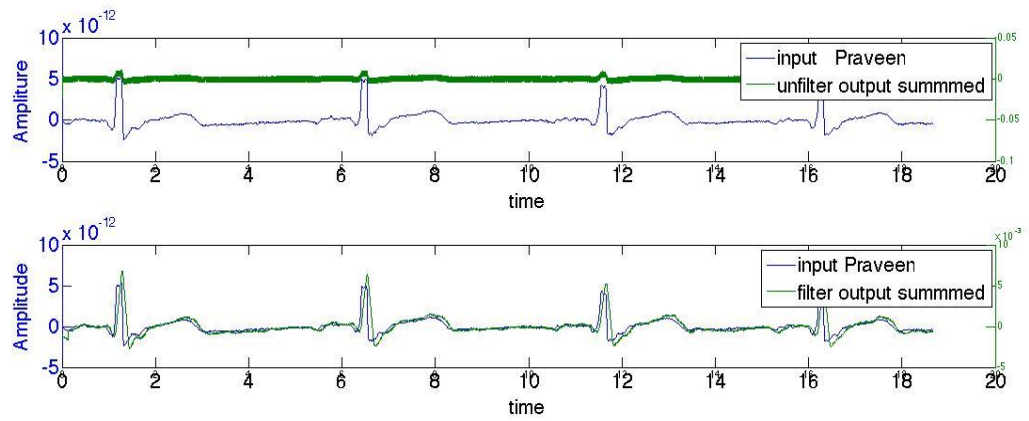
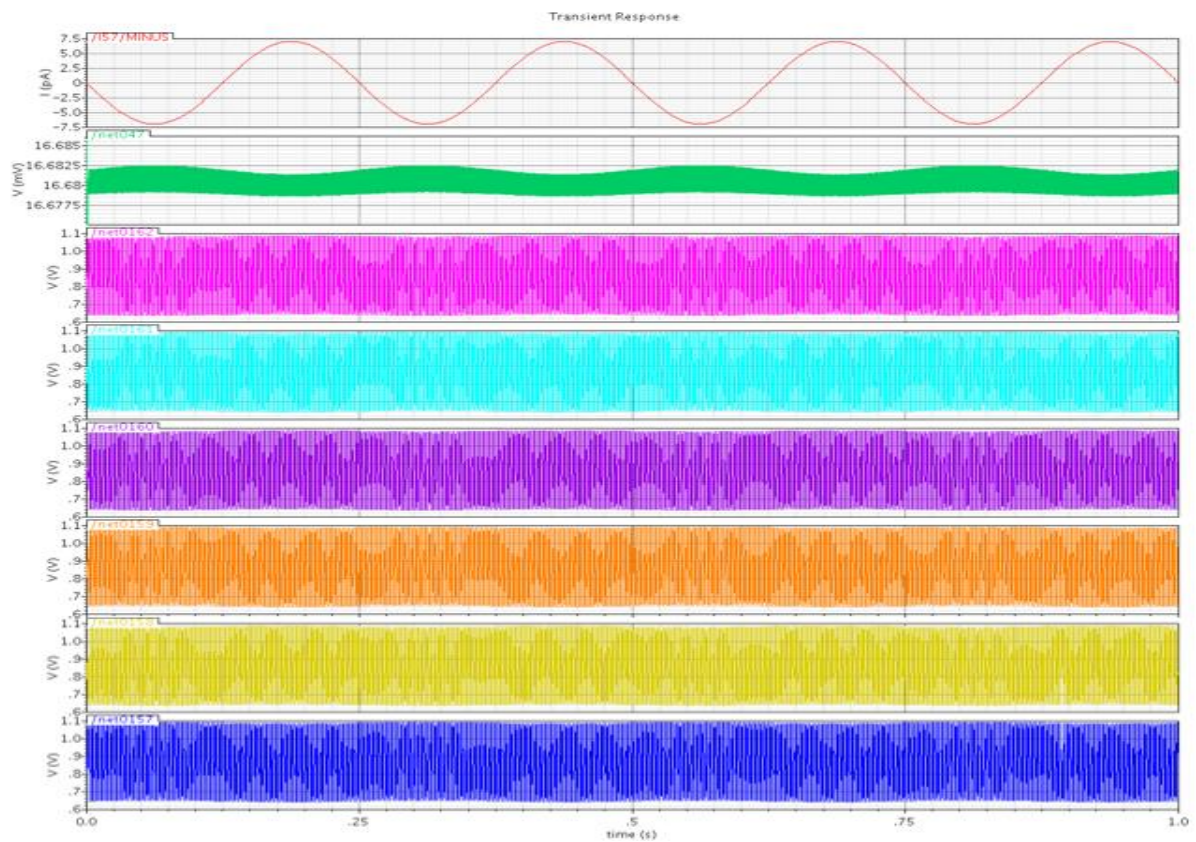


Figure 5.6: Sinusoidal signal Output



Chapter 6: Conclusions and Future Work

6.1 CONCLUSIONS

This dissertation research implemented energy efficient analog and digital circuits, which are used in designing non-linear ultra-sensitive patented sensor. The goal is accomplished with design and implementation of the novel rad-hard level shifter, DAC, and MUSS are implemented at the transistor level and its behavior is verified using simulations. Layout was also done for these cells in IBM 130nm CMOS technology.

6.2 FUTURE WORK

The dissertation is evaluated with Spectre simulations. The tape-out of the MUSS is failed in November with MOSIS. The chip will be resubmitted in January to comprehensively evaluate the data acquisition of biological signals. Also, the silicon fabrication is essential to test the radiation hardness of the level shifters. In this research, only five channels have been implemented with a single ADC. The future work would be extending the number of channels for measuring various biological signals. Further, an ADC is assigned to each channel for comprehensive power analysis and reducing the usage of MUX. Further, the future work upon receiving the silicon, the Bluetooth module must be developed to send the biological signal information to any Bluetooth enabled device.

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Appendix A

1. 2X1 Multiplexer

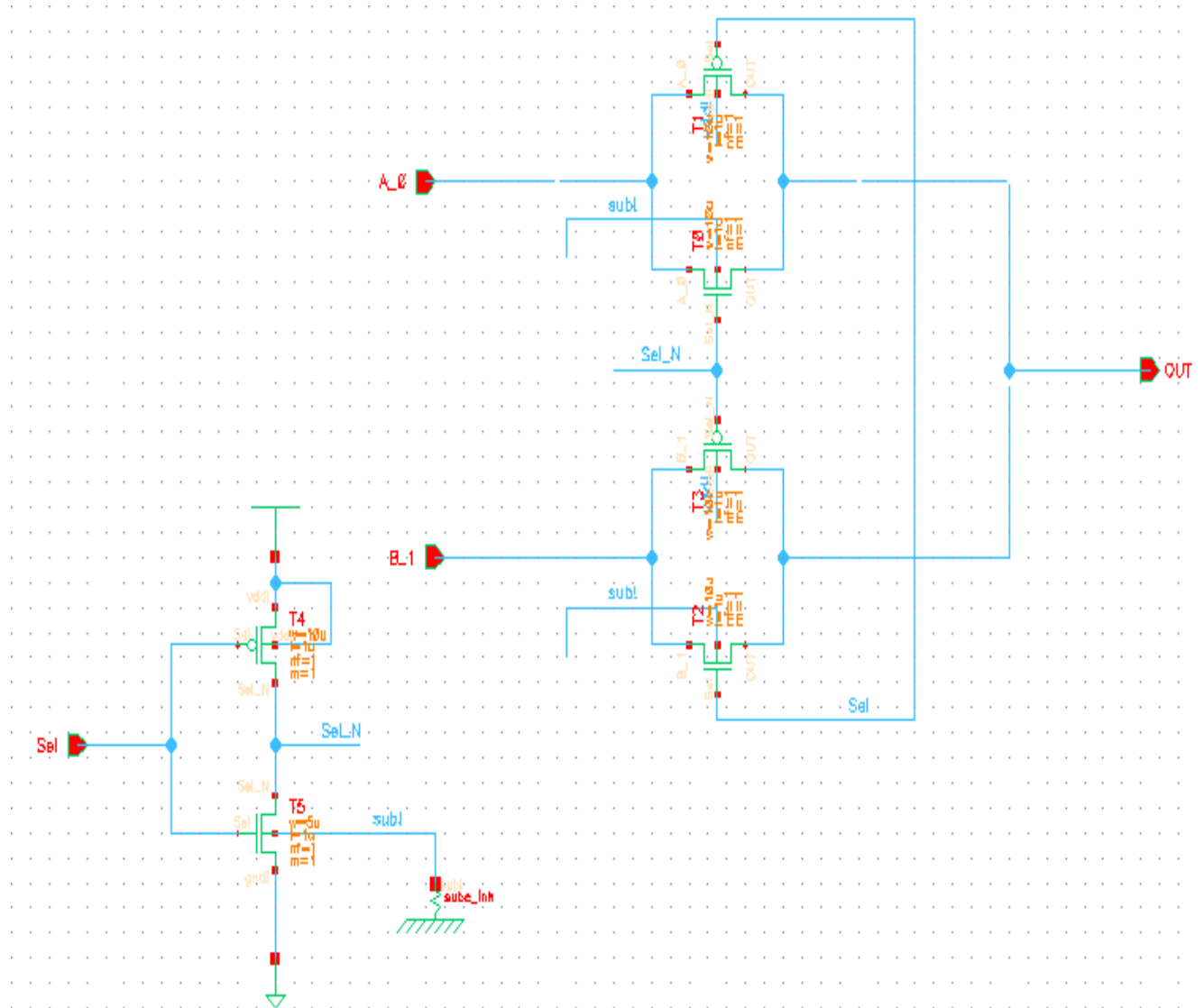


Figure A.1: Multiplexer

2. Operational Amplifier

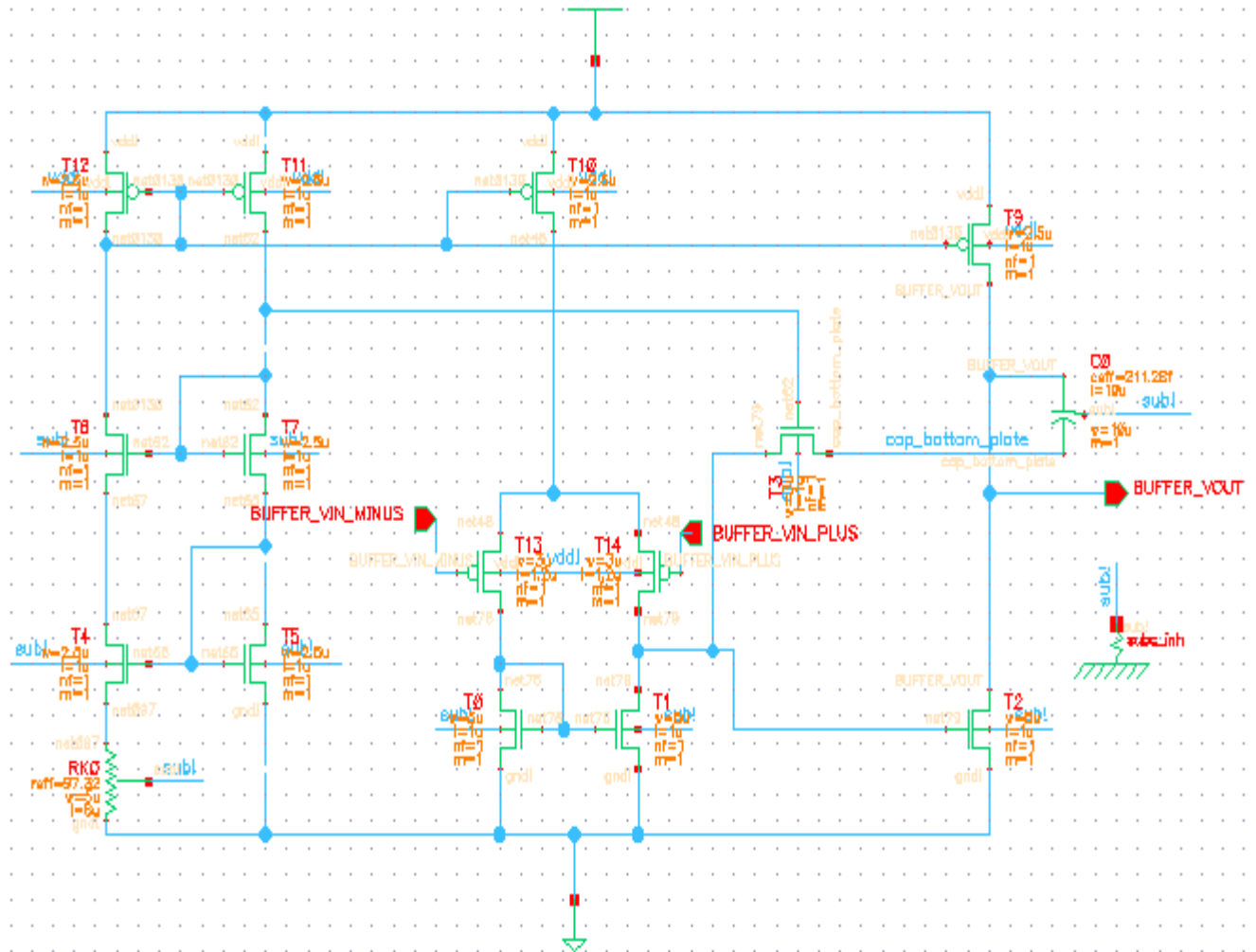


Figure A.2: Operational Amplifier

3. Summing Circuit

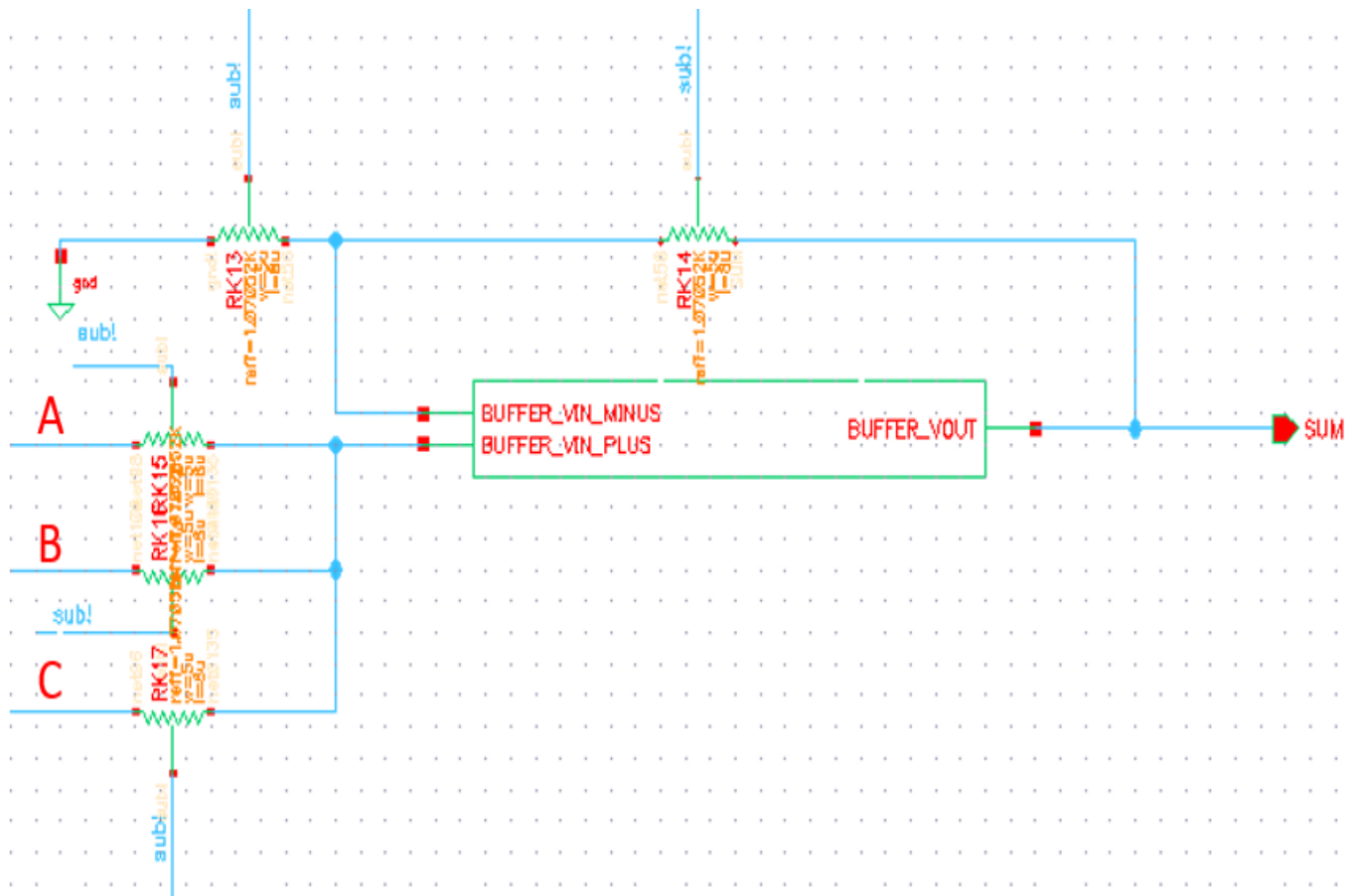
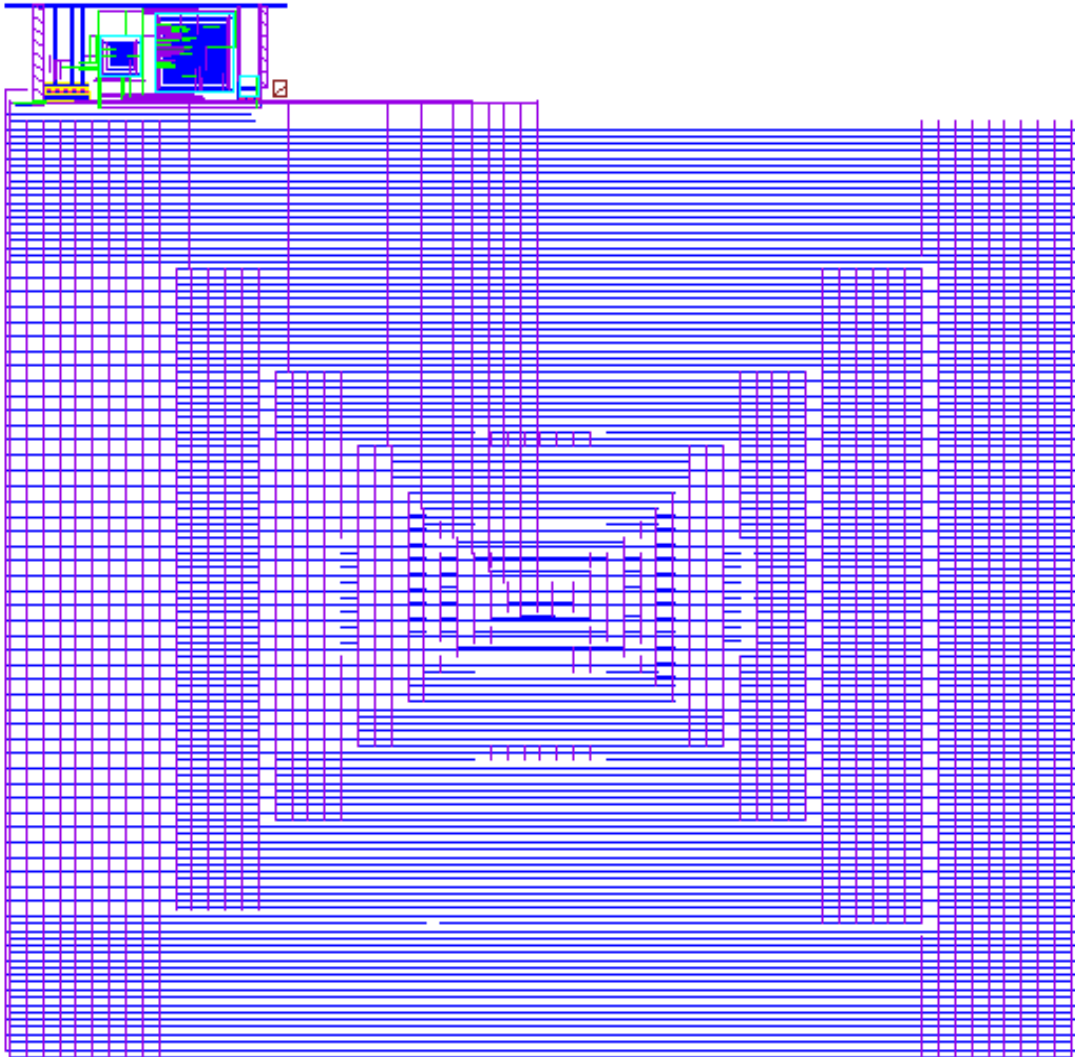


Figure A.3: Summing Circuit

4. ADC Layout

Figure A.4: ADC Layout



5. Unit Capacitor

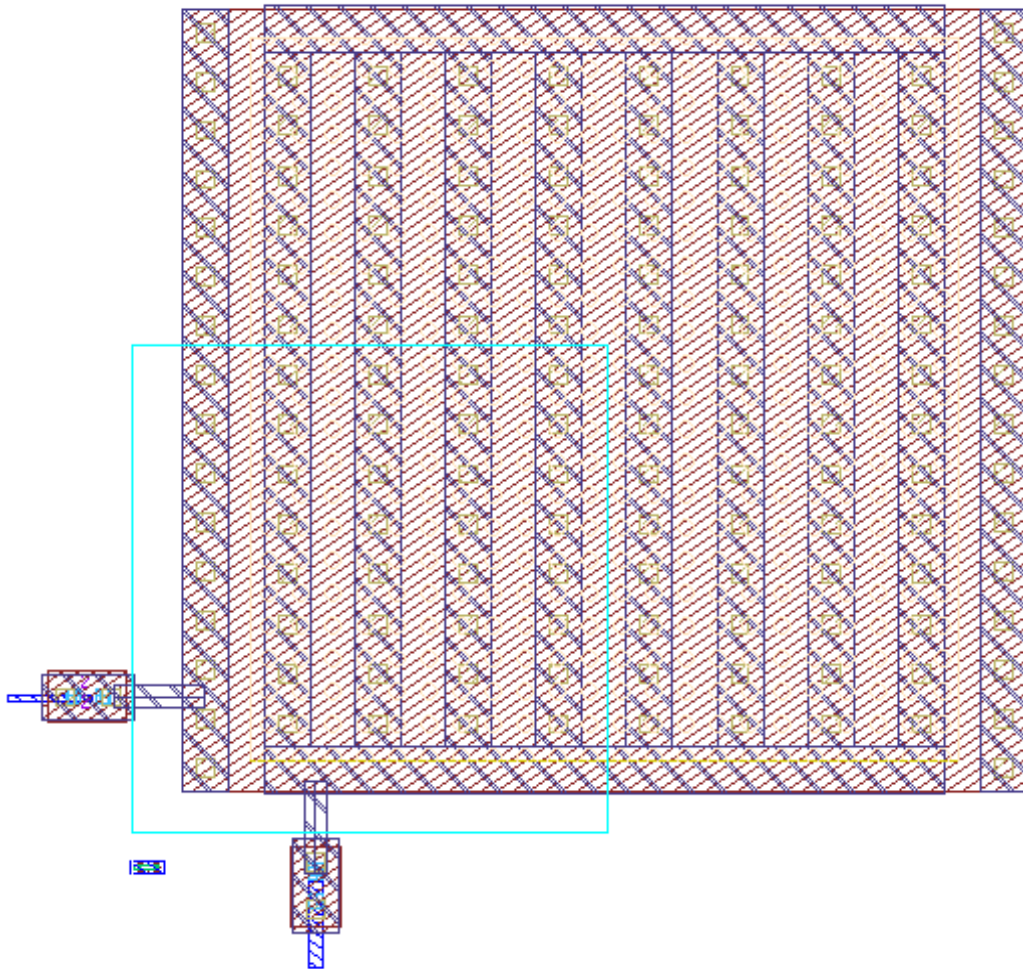


Figure A.5: Unit Capacitor Layout

6. Single Element

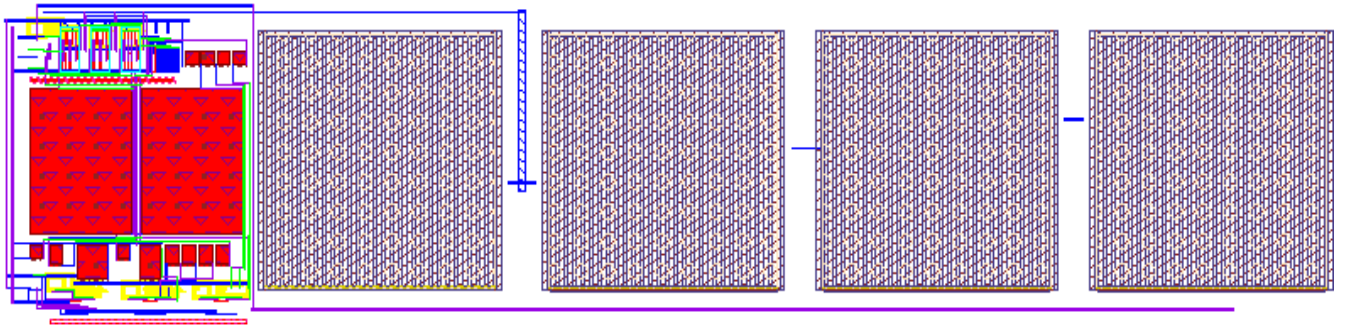


Figure A.6: Single Element Layout

7. Single Channel Layout

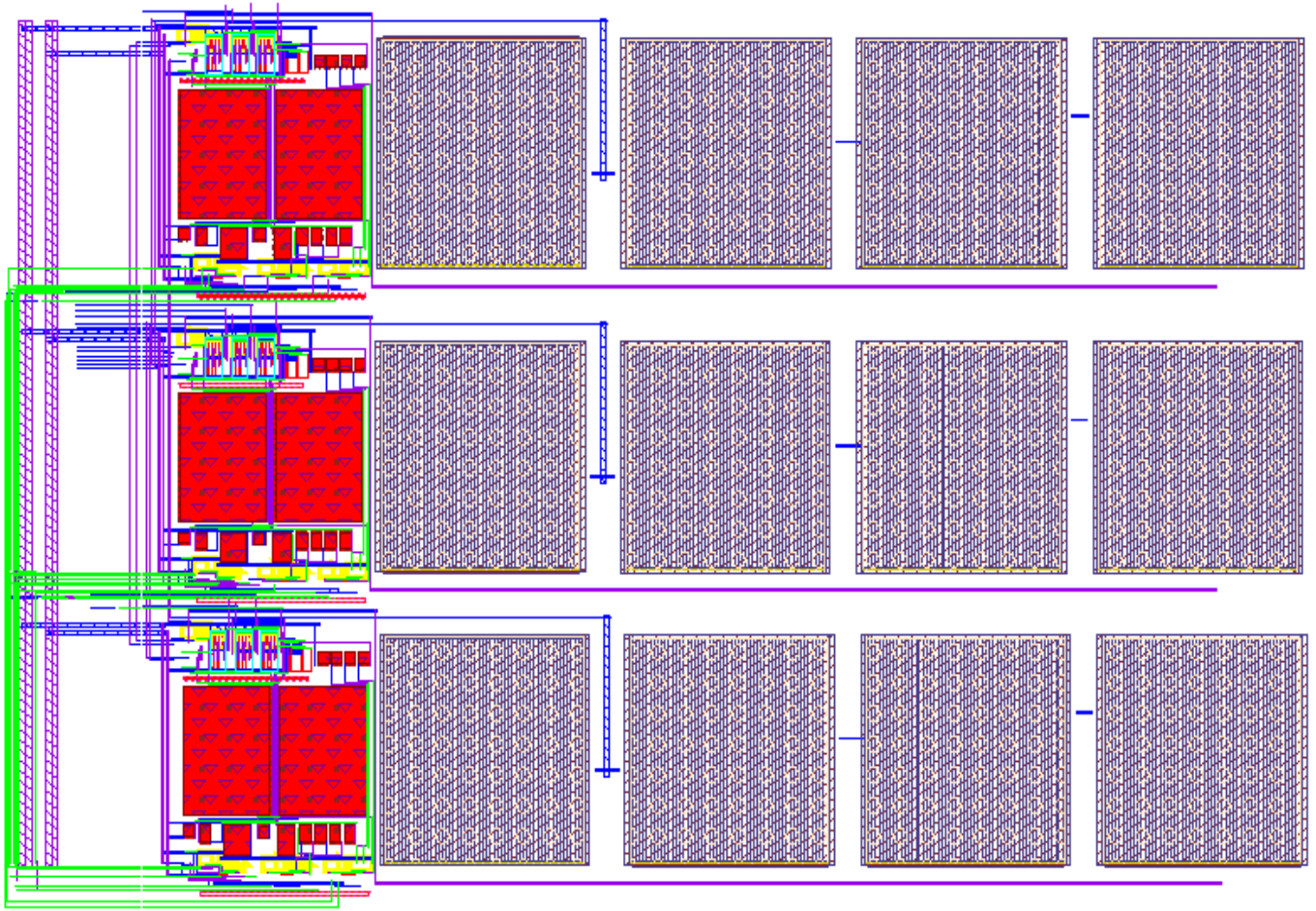


Figure A.7: Single Channel Layout

8. Five Channels and Summing Circuit Layout

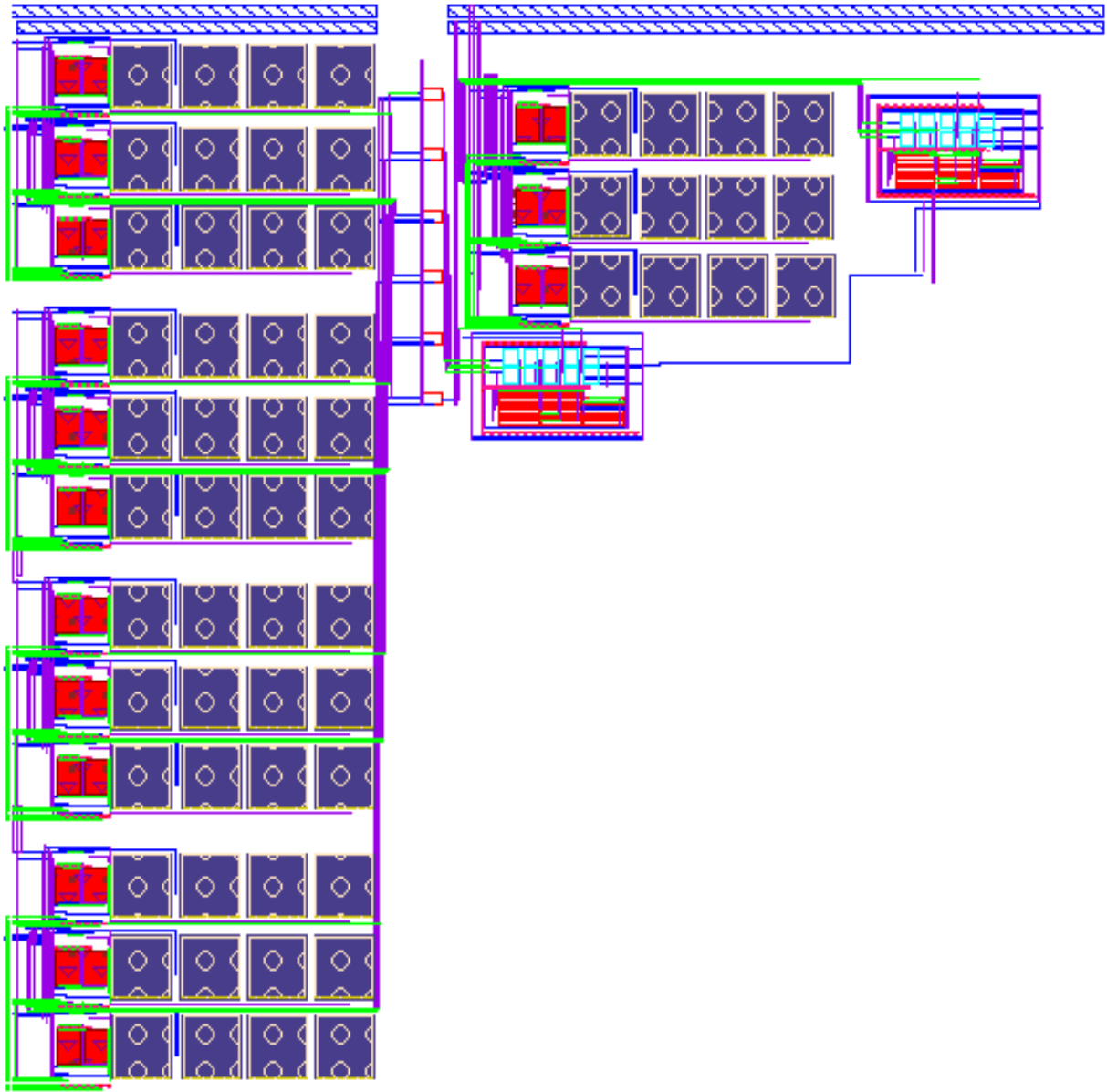


Figure A.8: Five Channels and Summing Circuit Layout

9. Operational Amplifier Layout

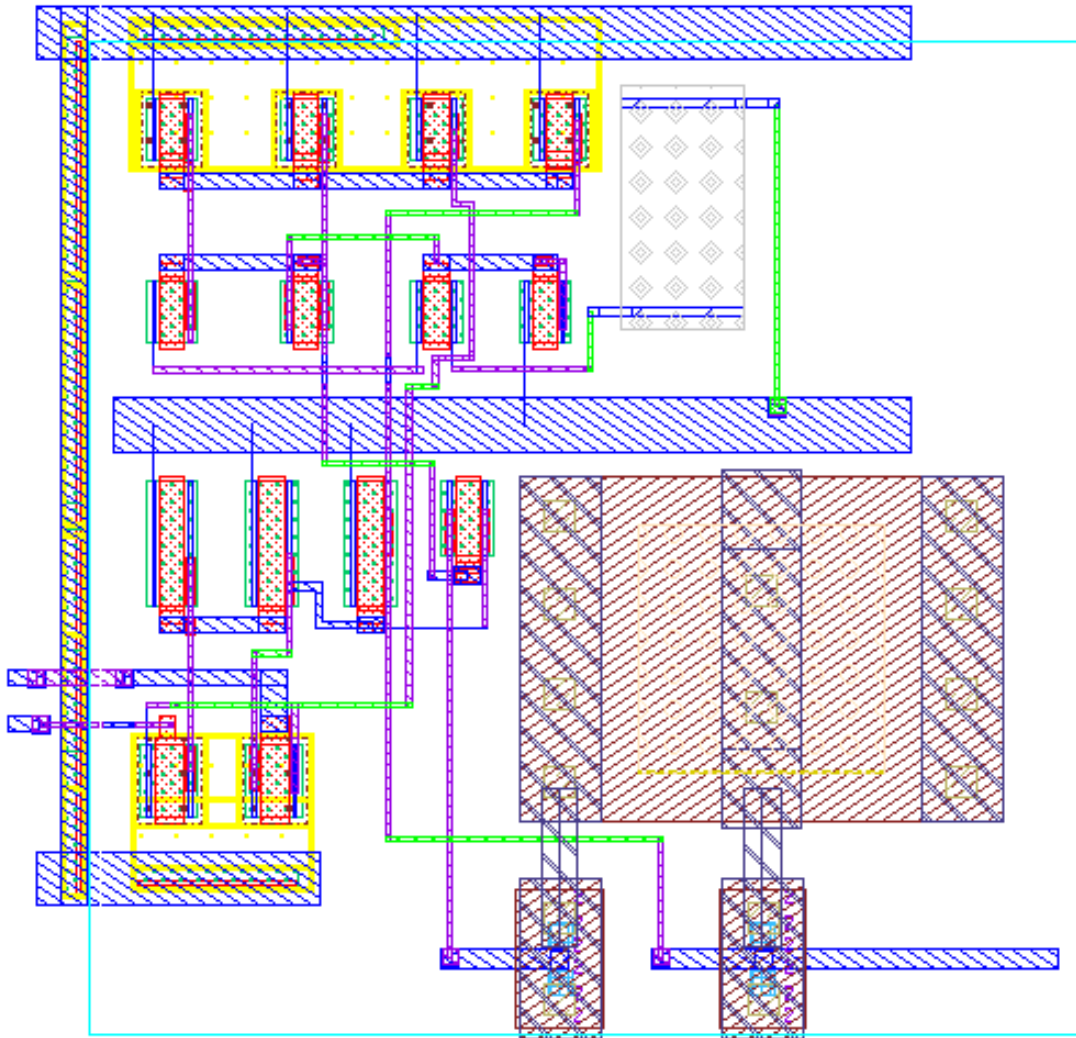


Figure A.9: Operational Amplifier Layout

10. Sample and Hold

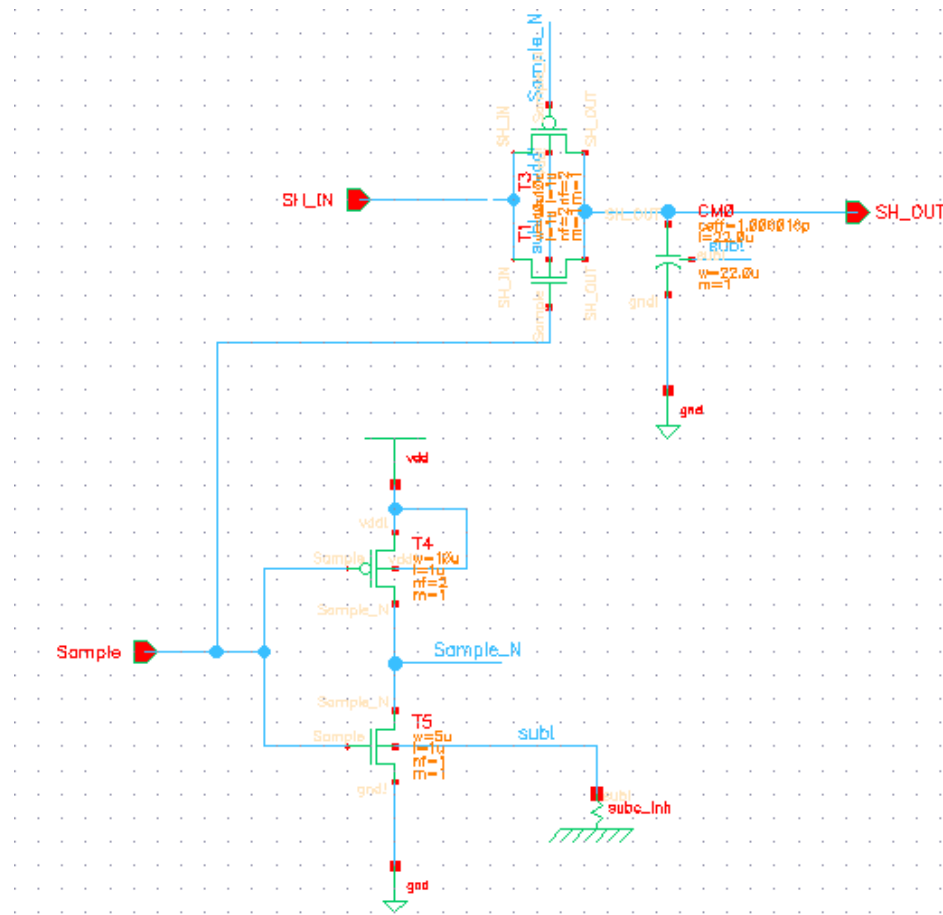


Figure A.10: Sample and Hold Circuit

11. Sample and Hold Layout

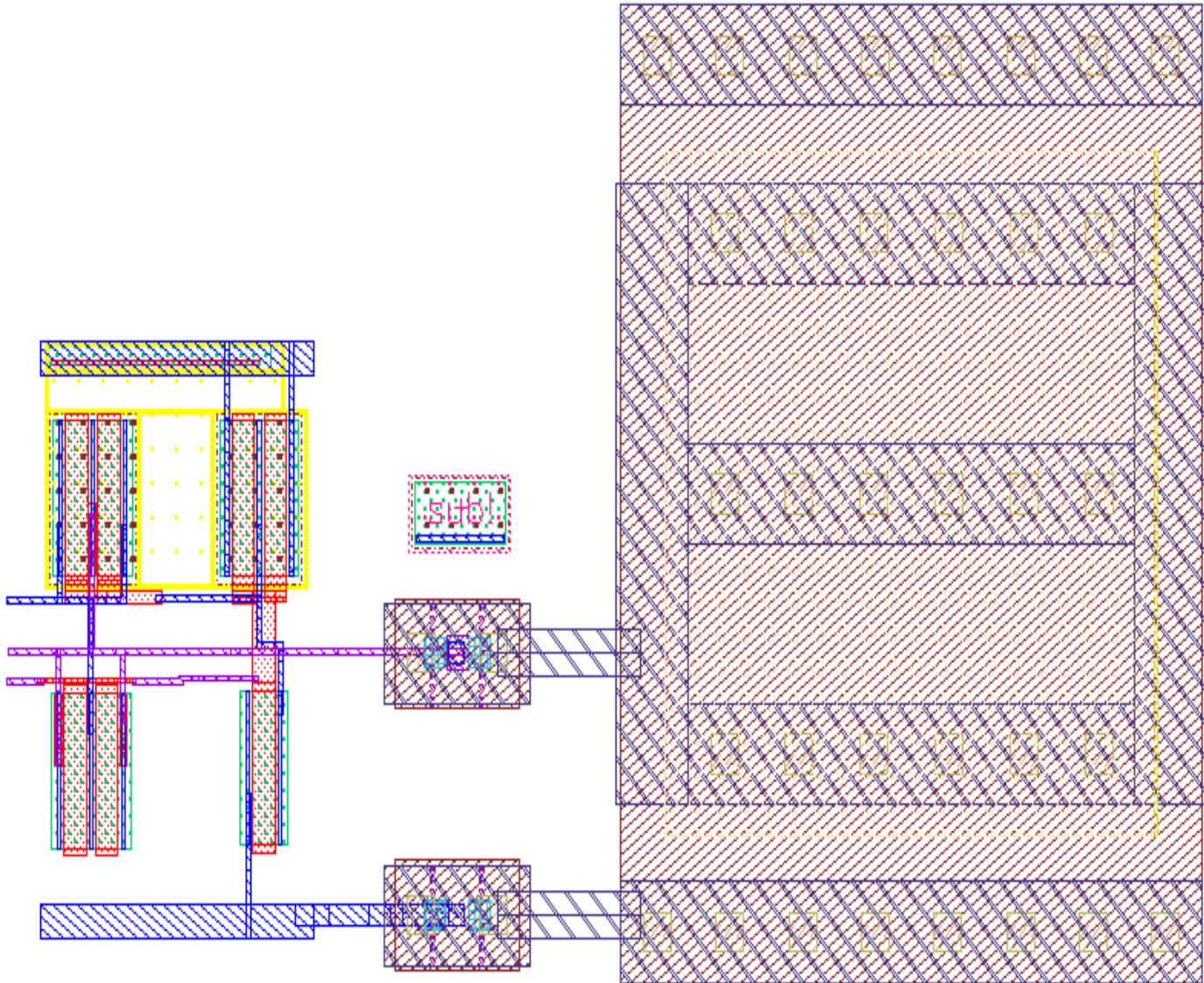


Figure A.11: Sample and Hold Layout

12. Final Chip with Pad Ring Layout

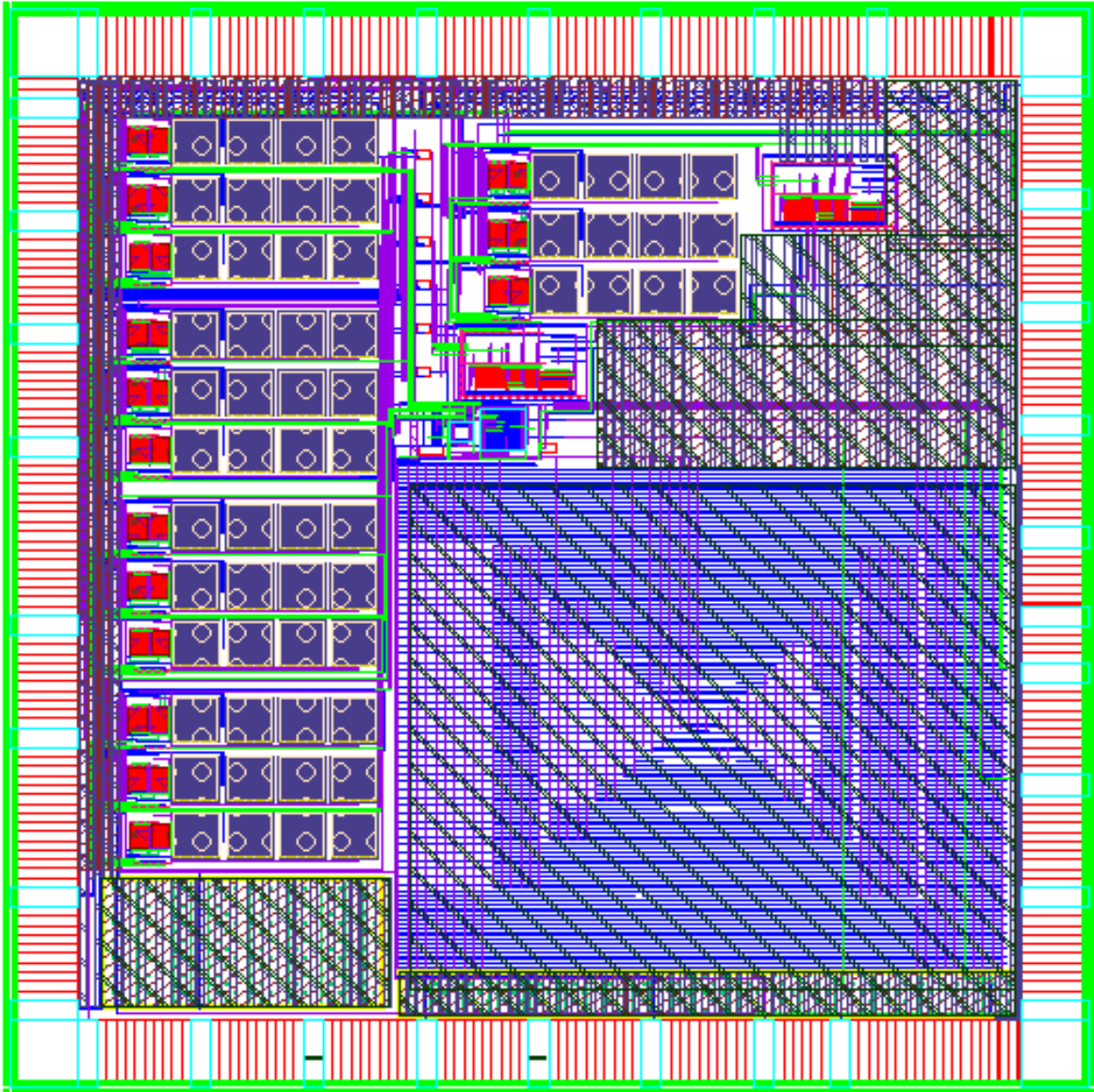


Figure A.12: Final Chip with Pad Ring Layout

13. Successive Approximation Register

```
module SAR_SR_1ADC ( clk,  
                    Start,  
                    Done,  
                    Sample,  
                    Value,  
                    Comparator);  
  
input clk;          // Clock  
input Start;        // Start = 1 to start conversion  
input Comparator;   // Comparator Output  
  
output Sample;      // to Sample and hold  
output Done;        // Done = 1 when conversion is done  
output [11:0] Value; // to Digital-to-Analog Converter  
  
reg [1:0] State;    // Current State  
reg [11:0] Result;  
reg [11:0] mask;  
  
parameter Wait_state = 0, Sample_state = 1, Conv_state = 2, Done_state = 3;  
  
always @(posedge clk) begin  
  
    if (!Start) State <= Wait_state;  
    else case (State)  
        Wait_state : State <= Sample_state;  

```

```

Sample_state : begin
    State <= Conv_state;
    mask <= 12'b100000000000;
    Result <= 12'b0;
end

Conv_state : begin
    //If Comparator output is 1 then set bit else clear
    if (Comparator) Result <= Result | mask;
    //shift mask for next bit in next Clock cycle
    mask <= mask >> 1;
    //Finish converting once LSB is 1
    if (mask[0]) State <= Done_state;
end

Done_state :;

endcase

end

assign Sample = State==Sample_state;
assign Value = Result | mask;
assign Done = State==Done_state;

endmodule

```

14. MATLAB Code

```
% load out.csv file

clear, clc

close all

warning off


[FileName,PathName,FilterIndex] = uigetfile('*.csv');

A = csvread([PathName FileName]);

%A=dlmread('out.txt');

t = (A(:,1)-min(A(:,1)));

%t = linspace(min(t),max(t),length(t));

dt = t(2)

Fs = 2048;

%Fs = 32765.4;

%Fs = 1/dt,

t = (1:length(t))/Fs;

x1 = A(:,2);

x2 = A(:,3);

x3 = A(:,4);

xIn = A(:,5);

xSum = A(:,6);


figure(1);

plot(t,x1,t,x2,t,x3,t,xSum,'k','LineWidth',2);

xlabel('time (s)');

ylabel('V');
```

```

figure(2)

plot(t,xSum,'k','LineWidth',2);

xlabel('time (s)');

ylabel('Sum (V)');


N = length(xSum);


xD = detrend(xSum);

h = spectrum.periodogram; % Instantiate a periodogram object.

out = msspectrum(h,xD,'Fs',Fs,'Nfft',N,'SpectrumType','onesided'); % PSD

mag = out.Data(1:N/2); % power output

out_in = msspectrum(h,xIn,'Fs',Fs,'Nfft',N,'SpectrumType','onesided'); % PSD

mag_in = out_in.Data(1:N/2); % power output

f = out.Frequencies(1:N/2); % frequency output


mx_ix]=max(mag); fx = f(ix),

NS = round(N/ix)


for j=1

    xf = filter(ones(1,NS)/NS,1,xD);

    xD = xf;

    out = msspectrum(h,xf,'Fs',Fs,'Nfft',N,'SpectrumType','onesided'); % PSD

    magF = out.Data(1:N/2);

end


figure(5); [ax hh1,hh2]=plotyy(t,detrend(xIn),t,detrend(xf));

```

```
xlabel('time'); ylabel('V')  
legend([hh1,hh2],'input','filter output summmed')  
linkaxes(ax,'x');
```

Appendix B

Verilog is a Hardware Description Language (HDL) developed to model electronics systems and used to describe behavioral model of digital circuits.

////////////////////////////////// $\Delta\Sigma$ Modulator Verilog Code//

```
`timescale 100 ps / 10 ps

module deltasigma8b(data_output, data_input, clk, reset);
    output data_output;
    input [7:0] data_input;
    input clk;
    input reset;
    reg data_output;
    wire [9:0] delta_add;
    wire [9:0] sigma_add;
    reg [9:0] sigma_reg;
    wire [9:0] delta_b;
    assign delta_b = {sigma_reg[9], sigma_reg[9], 8'b0} ;
    assign delta_add = data_input + delta_b;
    assign sigma_add = delta_add + sigma_reg;
    always @(posedge clk)
        if(reset) data_output <= 1'b0;
        else data_output <= sigma_reg[9];
    always @(posedge clk)
        if(reset) sigma_reg <= 9'b1_0000_0000;
        else sigma_reg <= sigma_add;
endmodule
```

```

////////////////Testbench used to stimulate the Verilog Code of the  $\Delta\Sigma$  Modulator////////////////
timescale 1ns / 1ps

module dstb();

reg clk;

reg reset;

reg [11:0] data_input;

////////////////////////////////////

// clock stimulus

////////////////////////////////////

initial clk = 0;

initial forever #20 clk = ~clk;

reg [7:0] sample_counter;

always @(posedge clk)

if(reset) sample_counter = 0;

else sample_counter = sample_counter + 1;

wire sample_clk = sample_counter[7];

////////////////////////////////////

// Reset and completion logic

////////////////////////////////////

initial

begin

reset <= 1;

data_input <= 0;

#10000 reset <= 0;

$display("resetN de-asserted");

@(posedge sample_clk) data_input <= 1;

@(posedge sample_clk) data_input <= 2;

```

```
@(posedge sample_clk) data_input <= 3;
@(posedge sample_clk) data_input <= 4;
@(posedge sample_clk) data_input <= 5;
@(posedge sample_clk) data_input <= 6;
@(posedge sample_clk) data_input <= 7;
@(posedge sample_clk) data_input <= 8;
@(posedge sample_clk) data_input <= 9;
@(posedge sample_clk) data_input <= 10;
@(posedge sample_clk) data_input <= 11;
@(posedge sample_clk) data_input <= 12;
@(posedge sample_clk) data_input <= 13;
@(posedge sample_clk) data_input <= 14;
@(posedge sample_clk) data_input <= 15;
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@(posedge sample_clk) data_input <= 30;
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@(posedge sample_clk) data_input <= 42;
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```

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@(posedge sample_clk) data_input <= 57;
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@(posedge sample_clk) data_input <= 61;
@(posedge sample_clk) data_input <= 62;
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@(posedge sample_clk) data_input <= 66;
@(posedge sample_clk) data_input <= 67;
@(posedge sample_clk) data_input <= 68;
@(posedge sample_clk) data_input <= 69;
@(posedge sample_clk) data_input <= 70;
@(posedge sample_clk) data_input <= 71;
@(posedge sample_clk) data_input <= 72;
@(posedge sample_clk) data_input <= 73;
@(posedge sample_clk) data_input <= 74;
@(posedge sample_clk) data_input <= 75;
@(posedge sample_clk) data_input <= 76;
@(posedge sample_clk) data_input <= 77;
@(posedge sample_clk) data_input <= 78;
@(posedge sample_clk) data_input <= 79;
@(posedge sample_clk) data_input <= 80;
@(posedge sample_clk) data_input <= 81;
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@(posedge sample_clk) data_input <= 83;
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@(posedge sample_clk) data_input <= 84;
@(posedge sample_clk) data_input <= 85;
@(posedge sample_clk) data_input <= 86;
@(posedge sample_clk) data_input <= 87;
@(posedge sample_clk) data_input <= 88;
@(posedge sample_clk) data_input <= 89;
@(posedge sample_clk) data_input <= 90;
@(posedge sample_clk) data_input <= 91;
@(posedge sample_clk) data_input <= 92;
@(posedge sample_clk) data_input <= 93;
@(posedge sample_clk) data_input <= 94;
@(posedge sample_clk) data_input <= 95;
@(posedge sample_clk) data_input <= 96;
@(posedge sample_clk) data_input <= 97;
@(posedge sample_clk) data_input <= 98;
@(posedge sample_clk) data_input <= 99;
@(posedge sample_clk) data_input <= 100;
#100000000000 $finish;
end

deltasigma deltasigma
(.clk ( clk ),
.reset ( reset ),
.data_input ( data_input ),
.data_output ( ouptut ));

////////////////////////////////////

// Waveform Generation

////////////////////////////////////

```

```
initial $dumpfile("verilog.vcd");  
initial $dumpvars();  
endmodule
```

Appendix C HSPICE

HSPICE (Hailey Simulation Program with Integrated Circuit Emphasis) is used in industry for accurate circuit simulation and offers foundry-certified MOS device models with state of the art simulation and analysis algorithms.

* Hspice netlist to calculate the power and delay of the $\Delta\Sigma$ DAC

* Top Cell Name: deltasigma8b

* View Name: schematic

*.BIPOLAR

*.RESI = 2000

*.RESVAL

*.CAPVAL

*.DIOPERI

*.DIOAREA

*.EQUATION

*.SCALE METER

*.MEGA

*.PARAM

*.GLOBAL Gnd

+ VddMod

*.PIN Gnd

*+ VddMod60

* Library Name: ricardo_deltasigma1

* View Name: schematic

* Sources Modulator150mv

vddM VddMod 0 dc vddpam

vddls1 VddLS1H 0 dc vddsup

vddls2 VddLS2H 0 dc vddsup

vddbuls1 Vddbufls1 0 dc vddsup

vddbuls2 Vddbufls2 0 dc vddsup

vdd4 VddLS1L 0 dc vddpam

vdd5 VddLS2L 0 dc vddpam

v0 Gnd 0 dc 0

vcclk clk 0 PULSE(0 150m 166.667u 16.666u 16.666u 166.667u 333.333u)

v1 data_input<0> 0 PULSE(0 150m 721.81m 16.666u 16.666u 720m 3.6)

v2 data_input<1> 0 PULSE(0 150m 721.81m 16.666u 16.666u 720m 3.6)

v3 data_input<2> 0 PULSE(0 150m 721.81m 16.666u 16.666u 720m 3.6)

v4 data_input<3> 0 PULSE(0 150m 721.81m 16.666u 16.666u 720m 3.6)

v5 data_input<4> 0 PULSE(0 150m 721.81m 16.666u 16.666u 720m 3.6)

v6 data_input<5> 0 PULSE(0 150m 721.81m 16.666u 16.666u 720m 3.6)

v7 data_input<6> 0 PULSE(0 150m 721.81m 16.666u 16.666u 720m 3.6)

v8 data_input<7> 0 PULSE(0 150m 1.81m 16.666u 16.666u 2.16 4.32)

vreset reset 0 PWL(0 150m 666.666u 150m 666.67u 0)61

* Library Name: ricardo_deltasigma1

* View Name: schematic

*.PININFO

```

CC2 data_outputrc Gnd 50f
XI5 net073 data_input<0> net094 data_input<1> net092 data_input<2> net090
+ data_input<3> net068 data_input<4> net047 data_input<5> net081 data_input<6>
+ net062 data_input<7> net050 clk net086 reset VddMod Gnd buffers8b
XI0 clk data_input<7> data_input<6> data_input<5> data_input<4> data_input<3>
+ data_input<2> data_input<1> data_input<0> data_outputrc reset VddMod Gnd
+ deltasigma8b_good
*****

*OPTIONS dsdac_V150
*****

.option post=1
.op all
.TRAN 12.6m tm uic
.param vddpam=150m
.param vddsup=2.5
.param tm=3.024
.nodeset v(n_4)=0
.nodeset v(n_8)=0
.nodeset v(n_12)=0
.nodeset v(n_15)=062
.nodeset v(n_19)=0
.nodeset v(n_23)=0
.nodeset v(n_26)=0
.nodeset v(n_29)=0
.nodeset v(n_32)=vddpam
.nodeset v(n_33)=0
.nodeset v(n_2)=0

```

```

*.nodeset v(L_out)=0

*.nodeset v(out)=0

*.IC v(l_out)=0

.IC v(data_outputrc)=0

.print TRAN v(data_input<7>) v(data_input<0>) v(data_outputrc) v(reset) v(clk)
i(VddMod)

.plot TRAN v(data_input<7>) v(data_input<0>) v(data_outputrc) v(reset) v(clk)
i(VddMod)

.print P(VddMod)

.measure TRAN iiddM integral i(vddM) FROM=0 TO=tm
.measure TRAN iiddLS1 integral i(vddls1) FROM=0 TO=tm
.measure TRAN iiddLS2 integral i(vddls2) FROM=0 TO=tm
.measure TRAN iiddbufls1 integral i(vddbuls1) FROM=0 TO=tm
.measure TRAN iiddbufls2 integral i(vddbuls2) FROM=0 TO=tm
.measure TRAN iiddbufls1low integral i(vdd4) FROM=0 TO=tm
.measure TRAN iiddbufls2low integral i(vdd5) FROM=0 TO=tm
.measure TRAN energyM param='iiddM*vddpam'
.measure TRAN energyLS1 param='iiddLS1*vddsup'
.measure TRAN energyLS2 param='iiddLS2*vddsup'63
.measure TRAN energybufls1 param='iiddbufls1*vddsup'
.measure TRAN energybufls2 param='iiddbufls2*vddsup'
.measure TRAN energybufls1low param='iiddbufls1low*vddsup'
.measure TRAN energybufls2low param='iiddbufls2low*vddsup'
.measure TRAN PWRM param='energyM/tm'
.measure TRAN PWRLS1 param='energyLS1/tm'
.measure TRAN PWRLS2 param='energyLS2/tm'
.measure TRAN PWRBUFLS1 param='energybufls1/tm'

```

```

.measure TRAN PWRBUFLS2 param='energybufls2/tm'
.measure TRAN PWRBUFLS1low param='energybufls1low/tm'
.measure TRAN PWRBUFLS2low param='energybufls2low/tm'

*****

.Include tsmc25.mod

*****

* Library Name: ricardo_deltasigma1
* Cell Name: inv_1
* View Name: schematic

*****

.SUBCKT inv_1 ip op VddMod Gnd

*.PININFO ip:I op:O

MP0 op ip VddMod VddMod PM W=3.36u L=240.00n m=1
MN0 op ip Gnd Gnd NM W=1.68u L=240.00n m=1

.ENDS64

*****

* Library Name: ricardo_deltasigma1
* Cell Name: buffers8b
* View Name: schematic

*****

.SUBCKT buffers8b b0 b0o b1 b1o b2 b2o b3 b3o b4 b4o b5 b5o b6 b6o b7 b7o clk
+ clko reset reseto VddMod Gnd

*.PININFO b0:I b1:I b2:I b3:I b4:I b5:I b6:I b7:I clk:I reset:I b0o:O b1o:O

*.PININFO b2o:O b3o:O b4o:O b5o:O b6o:O b7o:O clko:O reseto:O

XI19 net25 clko VddMod Gnd inv_1
XI18 net27 reseto VddMod Gnd inv_1
XI17 clk net25 VddMod Gnd inv_1

```

```

XI16 reset net27 VddMod Gnd inv_1
XI15 net37 b4o VddMod Gnd inv_1
XI14 net39 b5o VddMod Gnd inv_1
XI13 net41 b6o VddMod Gnd inv_1
XI12 net43 b7o VddMod Gnd inv_1
XI11 b4 net37 VddMod Gnd inv_1
XI10 b5 net39 VddMod Gnd inv_1
XI9 b6 net41 VddMod Gnd inv_1
XI8 b7 net43 VddMod Gnd inv_1
XI7 net47 b3o VddMod Gnd inv_1
XI6 b3 net47 VddMod Gnd inv_1
XI5 b2 net49 VddMod Gnd inv_1
XI4 net49 b2o VddMod Gnd inv_1
XI3 net55 b1o VddMod Gnd inv_1
XI2 b1 net55 VddMod Gnd inv_165
XI26 net59 b0o VddMod Gnd inv_1
XI25 b0 net59 VddMod Gnd inv_1
.ENDS

```

```

*****

```

```

* Library Name: ricardo_deltasigma1
* Cell Name: inv_4
* View Name: schematic

```

```

*****

```

```

.SUBCKT inv_4 ip op VddMod Gnd

```

```

*.PININFO ip:I op:O

```

```

MP0 op ip VddMod VddMod PM W=3.36u L=240.00n m=1

```

```

MP1 VddMod ip op VddMod PM W=3.36u L=240.00n m=1

```

MN1 Gnd ip op Gnd NM W=1.68u L=240.00n m=1

MN0 op ip Gnd Gnd NM W=1.68u L=240.00n m=1

.ENDS

* Library Name: ricardo_deltasigma1

* Cell Name: dp_1

* View Name: schematic

.SUBCKT dp_1 ck ip q VddMod Gnd

*.PININFO ck:I ip:I q:O

MN0 net44 ip Gnd Gnd NM W=840.0n L=240.0n m=1

MN1 net38 ck Gnd Gnd NM W=840.0n L=240.0n m=1

MN2 net35 net38 net44 Gnd NM W=840.0n L=240.0n m=1

MN3 net32 ck net35 Gnd NM W=840.0n L=240.0n m=1

MN4 net32 net78 Gnd Gnd NM W=840.0n L=240.0n m=166

MN5 net78 net35 Gnd Gnd NM W=840.0n L=240.0n m=1

MN6 net20 net78 Gnd Gnd NM W=840.0n L=240.0n m=1

MN7 net63 ck net20 Gnd NM W=840.0n L=240.0n m=1

MN8 net12 net38 net63 Gnd NM W=840.0n L=240.0n m=1

MN9 Gnd q net12 Gnd NM W=840.0n L=240.0n m=1

MN10 q net63 Gnd Gnd NM W=840.0n L=240.0n m=1

MP0 net88 ip VddMod VddMod PM W=1.68u L=240.0n m=1

MP1 net38 ck VddMod VddMod PM W=1.68u L=240.0n m=1

MP2 net35 ck net88 VddMod PM W=1.68u L=240.0n m=1

MP3 net80 net38 net35 VddMod PM W=1.68u L=240.0n m=1

MP4 VddMod net78 net80 VddMod PM W=1.68u L=240.0n m=1

MP5 net78 net35 VddMod VddMod PM W=1.68u L=240.0n m=1

MP6 net68 net78 VddMod VddMod PM W=1.68u L=240.0n m=1

MP7 net63 net38 net68 VddMod PM W=1.68u L=240.0n m=1

MP8 net60 ck net63 VddMod PM W=1.68u L=240.0n m=1

MP9 VddMod q net60 VddMod PM W=1.68u L=240.0n m=1

MP10 q net63 VddMod VddMod PM W=1.68u L=240.0n m=1

.ENDS

* Library Name: ricardo_deltasigma1

* Cell Name: and2_2

* View Name: schematic

.SUBCKT and2_2 ip1 ip2 op VddMod Gnd

*.PININFO ip1:I ip2:I op:O

MN2 op net32 Gnd Gnd NM W=1.68u L=240.0n m=1

MN1 net32 ip1 net27 Gnd NM W=1.68u L=240.0n m=167

MN0 net27 ip2 Gnd Gnd NM W=1.68u L=240.0n m=1

MP1 net32 ip1 VddMod VddMod PM W=3.36u L=240.0n m=1

MP2 op net32 VddMod VddMod PM W=3.36u L=240.0n m=1

MP0 net32 ip2 VddMod VddMod PM W=3.36u L=240.0n m=1

.ENDS

* Library Name: ricardo_deltasigma1

* Cell Name: nor2_2

* View Name: schematic

.SUBCKT nor2_2 ip1 ip2 op VddMod Gnd

*.PININFO ip1:I ip2:I op:O

MP0 net35 ip1 VddMod VddMod PM W=3.36u L=240.0n m=1

MP1 op ip2 net35 VddMod PM W=3.36u L=240.0n m=1

MN0 op ip2 Gnd Gnd NM W=1.68u L=240.0n m=1

MN1 op ip1 Gnd Gnd NM W=1.68u L=240.0n m=1

.ENDS

* Library Name: ricardo_deltasigma1

* Cell Name: xnor2_2

* View Name: schematic

.SUBCKT xnor2_2 ip1 ip2 op VddMod Gnd

*.PININFO ip1:I ip2:I op:O

MP0 VddMod ip1 net096 VddMod PM W=1.68u L=240.0n m=1

MP18 VddMod ip1 net069 VddMod PM W=1.68u L=240.0n m=1

MP14 op net072 VddMod VddMod PM W=3.36u L=240.0n m=168

MP17 net071 ip2 VddMod VddMod PM W=1.68u L=240.0n m=1

MP16 net072 ip2 net084 VddMod PM W=1.68u L=240.0n m=1

MP19 net069 net071 net072 VddMod PM W=1.68u L=240.0n m=1

MP15 net084 net096 VddMod VddMod PM W=1.68u L=240.0n m=1

MN19 Gnd net096 net0108 Gnd NM W=840.0n L=240.0n m=1

MN13 op net072 Gnd Gnd NM W=1.68u L=240.0n m=1

MN18 net0108 net071 net072 Gnd NM W=840.0n L=240.0n m=1

MN20 net0116 ip1 Gnd Gnd NM W=840.0n L=240.0n m=1

MN17 net072 ip2 net0116 Gnd NM W=840.0n L=240.0n m=1

MN16 net071 ip2 Gnd Gnd NM W=840.0n L=240.0n m=1

MN21 Gnd ip1 net096 Gnd NM W=840.0n L=240.0n m=1

.ENDS

* Library Name: ricardo_deltasigma1

* Cell Name: and2_1

* View Name: schemati

.SUBCKT and2_1 ip1 ip2 op VddMod Gnd

*.PININFO ip1:I ip2:I op:O

MP0 net12 ip2 VddMod VddMod PM W=1.68u L=240.0n m=1

MP2 op net12 VddMod VddMod PM W=1.68u L=240.0n m=1

MP1 net12 ip1 VddMod VddMod PM W=1.68u L=240.0n m=1

MN0 net063 ip2 Gnd Gnd NM W=840.0n L=240.0n m=1

MN1 net12 ip1 net063 Gnd NM W=840.0n L=240.0n m=1

MN2 op net12 Gnd Gnd NM W=840.0n L=240.0n m=1

.ENDS

* Library Name: ricardo_deltasigma1

* Cell Name: fulladder

* View Name: schematic

.SUBCKT fulladder a b ci co s VddMod Gnd

*.PININFO a:I b:I ci:I co:O s:O

MP5 co net76 VddMod VddMod PM W=1.68u L=240.0n m=1

MP2 net76 b net6 VddMod PM W=1.68u L=240.0n m=1

MP3 net14 ci net76 VddMod PM W=1.68u L=240.0n m=1

MP4 s net90 VddMod VddMod PM W=1.68u L=240.0n m=1

MP6 net50 net76 net90 VddMod PM W=1.68u L=240.0n m=1

MP7 net90 ci net42 VddMod PM W=1.68u L=240.0n m=1

MP8 net50 a VddMod VddMod PM W=1.68u L=240.0n m=1
 MP9 VddMod b net50 VddMod PM W=1.68u L=240.0n m=1
 MP10 net50 ci VddMod VddMod PM W=1.68u L=240.0n m=1
 MP11 net46 a net50 VddMod PM W=1.68u L=240.0n m=1
 MP12 net42 b net46 VddMod PM W=1.68u L=240.0n m=1
 MP15 net14 a VddMod VddMod PM W=1.68u L=240.0n m=1
 MP16 VddMod b net14 VddMod PM W=1.68u L=240.0n m=1
 MP17 net6 a net14 VddMod PM W=1.68u L=240.0n m=1
 MN0 s net90 Gnd Gnd NM W=840.0n L=240.0n m=1
 MN5 net90 ci net98 Gnd NM W=840.0n L=240.0n m=1
 MN4 co net76 Gnd Gnd NM W=840.0n L=240.0n m=1
 MN2 net73 ci net76 Gnd NM W=840.0n L=240.0n m=1
 MN3 net76 b net66 Gnd NM W=840.0n L=240.0n m=1
 MN6 net106 net76 net90 Gnd NM W=840.0n L=240.0n m=1
 MN7 net101 a Gnd Gnd NM W=840.0n L=240.0n m=170
 MN9 Gnd a net106 Gnd NM W=840.0n L=240.0n m=1
 MN10 net106 b Gnd Gnd NM W=840.0n L=240.0n m=1
 MN11 Gnd b net73 Gnd NM W=840.0n L=240.0n m=
 MN12 net66 a Gnd Gnd NM W=840.0n L=240.0n m=1
 MN13 net73 a Gnd Gnd NM W=840.0n L=240.0n m=1
 MN14 Gnd ci net106 Gnd NM W=840.0n L=240.0n m=1
 MN15 net98 b net101 Gnd NM W=840.0n L=240.0n m=1

.ENDS

* Library Name: ricardo_deltasigma1

* Cell Name: or2_1

* View Name: schematic

.SUBCKT or2_1 ip1 ip2 op VddMod Gnd

*.PININFO ip1:I ip2:I op:O

MP2 op net46 VddMod VddMod PM W=1.68u L=240.0n m=1

MP1 net29 ip1 VddMod VddMod PM W=1.68u L=240.0n m=1

MP0 net46 ip2 net29 VddMod PM W=1.68u L=240.0n m=1

MN2 op net46 Gnd Gnd NM W=840.0n L=240.0n m=1

MN0 net46 ip1 Gnd Gnd NM W=840.0n L=240.0n m=1

MN1 net46 ip2 Gnd Gnd NM W=840.0n L=240.0n m=1

.ENDS71

* Library Name: ricardo_deltasigma1

* Cell Name: deltasigma8b_good

* View Name: schematic

.SUBCKT deltasigma8b_good clk data_input<7> data_input<6> data_input<5>

+ data_input<4> data_input<3> data_input<2> data_input<1> data_input<0>

+ data_output reset VddMod Gnd

*.PININFO clk:I data_input<7>:I data_input<6>:I data_input<5>:I

*.PININFO data_input<4>:I data_input<3>:I data_input<2>:I data_input<1>:I

*.PININFO data_input<0>:I reset:I data_output:O

Xg1355 reset n_11 VddMod Gnd inv_4

Xsigma_reg_reg[1] clk n_8 sigma_reg[1] VddMod Gnd dp_1

Xsigma_reg_reg[2] clk n_12 sigma_reg[2] VddMod Gnd dp_1

Xsigma_reg_reg[8] clk n_32 sigma_reg[8] VddMod Gnd dp_1

Xsigma_reg_reg[9] clk n_33 sigma_reg[9] VddMod Gnd dp_1

Xsigma_reg_reg[3] clk n_15 sigma_reg[3] VddMod Gnd dp_1

Xsigma_reg_reg[4] clk n_19 sigma_reg[4] VddMod Gnd dp_1
Xsigma_reg_reg[5] clk n_23 sigma_reg[5] VddMod Gnd dp_1
Xsigma_reg_reg[6] clk n_26 sigma_reg[6] VddMod Gnd dp_1
Xsigma_reg_reg[7] clk n_29 sigma_reg[7] VddMod Gnd dp_1
Xsigma_reg_reg[0] clk n_4 sigma_reg[0] VddMod Gnd dp_1
Xdata_output_reg clk n_2 data_output VddMod Gnd dp_1
Xg1352 data_input<0> sigma_reg[0] n_1 VddMod Gnd and2_2
Xg1351 n_11 sigma_reg[9] n_2 VddMod Gnd and2_2
Xg1348 reset n_3 n_4 VddMod Gnd nor2_2
Xg1350 data_input<0> sigma_reg[0] n_3 VddMod Gnd xnor2_272
Xg1345 n_11 n_6 n_8 VddMod Gnd and2_1
Xg1323 n_11 n_30 n_33 VddMod Gnd and2_1
Xg1342 n_11 n_10 n_12 VddMod Gnd and2_1
Xg1339 n_11 n_14 n_15 VddMod Gnd and2_1
Xg1336 n_11 n_17 n_19 VddMod Gnd and2_1
Xg1333 n_11 n_21 n_23 VddMod Gnd and2_1
Xg1330 n_11 n_25 n_26 VddMod Gnd and2_1
Xg1327 n_11 n_28 n_29 VddMod Gnd and2_1
Xg1343 sigma_reg[2] n_5 data_input<2> n_9 n_10 VddMod Gnd fulladder
Xg1346 sigma_reg[1] n_1 data_input<1> n_5 n_6 VddMod Gnd fulladder
Xg1325 sigma_reg[9] n_27 sigma_reg[8] n_30 n_31 VddMod Gnd fulladder
Xg1337 sigma_reg[4] n_13 data_input<4> n_16 n_17 VddMod Gnd fulladder
Xg1340 sigma_reg[3] n_9 data_input<3> n_13 n_14 VddMod Gnd fulladder
Xg1331 sigma_reg[6] n_20 data_input<6> n_24 n_25 VddMod Gnd fulladder
Xg1334 sigma_reg[5] n_16 data_input<5> n_20 n_21 VddMod Gnd fulladder
Xg1328 sigma_reg[7] n_24 data_input<7> n_27 n_28 VddMod Gnd fulladder
Xg1324 n_31 reset n_32 VddMod Gnd or2_1

.ENDS

*LEVEL SHIFTER NOVEL

*****subth inverter*****

MN3 sub1_b_n data_outputrc 0 0 NM w=0.5u L=240N m=1

MP3 sub1_b_n data_outputrc VddLS2L VddLS2L PM w=1.0u L=240N m=1

*****pull down nfets*****

MN4 A2 data_outputrc 0 0 NM w=5u L=240N m=1

MN5 LS2_out sub1_b_n 0 0 NM w=5u L=240N m=1

*****pmos current mirror*****

MP4 A A VddLS2H VddLS2H PM w=360N L=240N m=1

MP5 Z A VddLS2H VddLS2H PM w=360N L=240N m=1

MP6 A1 A1 A VddLS2H PM w=360N L=240N m=1

MP7 Z1 A1 Z VddLS2H PM w=360N L=240N m=1

MP8 A2 A2 A1 VddLS2H PM w=360N L=240N m=1

MP9 LS2_out A2 Z1 VddLS2H PM w=360N L=240N m=1

*BUFFER SHIFTER NOVEL

*****Inverter1*****

MN310 x1 LS2_out 0 0 NM w=0.5u L=240N m=1

MP310 x1 LS2_out Vddbufls2 Vddbufls2 PM w=1.0u L=240N m=1

MN311 x2 x1 0 0 NM w=0.5u L=240N m=1

MP311 x2 x1 Vddbufls2 Vddbufls2 PM w=1.0u L=240N m=1

*****Inverter2*****

MN312 x3 x2 0 0 NM w=2.0u L=240N m=1

MP312 x3 x2 Vddbufls2 Vddbufls2 PM w=4.0u L=240N m=1

MN313 x4 x3 0 0 NM w=2.0u L=240N m=1

```

MP313 x4 x3 Vddbufls2 Vddbufls2 PM w=4.0u L=240N m=1
*****Inverter3*****
MN314 x5 x4 0 0 NM w=2.0u L=240N m=4
MP314 x5 x4 Vddbufls2 Vddbufls2 PM w=4.0u L=240N m=4
MN315 x6 x5 0 0 NM w=2.0u L=240N m=4
MP315 x6 x5 Vddbufls2 Vddbufls2 PM w=4.0u L=240N m=4
*****Inverter4*****
MN316 x7 x6 0 0 NM w=2.0u L=240N m=1674
MP316 x7 x6 Vddbufls2 Vddbufls2 PM w=4.0u L=240N m=16
MN317 x8 x7 0 0 NM w=2.0u L=240N m=16
MP317 x8 x7 Vddbufls2 Vddbufls2 PM w=4.0u L=240N m=16
*****Inverter5*****
MN318 x9 x8 0 0 NM w=2.0u L=240N m=64
MP318 x9 x8 Vddbufls2 Vddbufls2 PM w=4.0u L=240N m=64
MN319 outb1s2 x9 0 0 NM w=2.0u L=240N m=64
MP319 outb1s2 x9 Vddbufls2 Vddbufls2 PM w=4.0u L=240N m=64
*****
*LEVEL SHIFTER TRADITIONAL
*****subth inverter*****
MN31 sub2_b_n data_outputrc 0 0 NM w=0.5u L=240N m=1
MP31 sub2_b_n data_outputrc VddLS1L VddLS1L PM w=1.0u L=240N m=1
*****pull down nfets*****
MN41 Ab data_outputrc 0 0 NM w=5u L=240N m=1
MN51 LS1_out sub2_b_n 0 0 NM w=5u L=240N m=1
*****pmos current mirror*****
MP41 Ab Ab VddLS1H VddLS1H PM w=360N L=240N m=1
MP51 LS1_out Ab VddLS1H VddLS1H PM w=360N L=240N m=1

```

*BUFFER SHIFTER traditional

*****Inverter1*****

MN320 xy1 LS1_out 0 0 NM w=0.5u L=240N m=1

MP320 xy1 LS1_out Vddbufls1 Vddbufls1 PM w=1.0u L=240N m=1

MN321 xy2 xy1 0 0 NM w=0.5u L=240N m=1

MP321 xy2 xy1 Vddbufls1 Vddbufls1 PM w=1.0u L=240N m=1

*****Inverter2*****

MN322 xy3 xy2 0 0 NM w=2.0u L=240N m=1

MP322 xy3 xy2 Vddbufls1 Vddbufls1 PM w=4.0u L=240N m=1

MN323 xy4 xy3 0 0 NM w=2.0u L=240N m=1

MP323 xy4 xy3 Vddbufls1 Vddbufls1 PM w=4.0u L=240N m=1

*****Inverter3*****

MN324 xy5 xy4 0 0 NM w=2.0u L=240N m=4

MP324 xy5 xy4 Vddbufls1 Vddbufls1 PM w=4.0u L=240N m=4

MN325 xy6 xy5 0 0 NM w=2.0u L=240N m=4

MP325 xy6 xy5 Vddbufls1 Vddbufls1 PM w=4.0u L=240N m=4

*****Inverter4*****

MN326 xy7 xy6 0 0 NM w=2.0u L=240N m=16

MP326 xy7 xy6 Vddbufls1 Vddbufls1 PM w=4.0u L=240N m=16

MN327 xy8 xy7 0 0 NM w=2.0u L=240N m=16

MP327 xy8 xy7 Vddbufls1 Vddbufls1 PM w=4.0u L=240N m=16

*****Inverter5*****

MN328 xy9 xy8 0 0 NM w=2.0u L=240N m=64

MP328 xy9 xy8 Vddbufls1 Vddbufls1 PM w=4.0u L=240N m=64

MN329 outbls1 xy9 0 0 NM w=2.0u L=240N m=64

MP329 outbls1 xy9 Vddbufls1 Vddbufls1 PM w=4.0u L=240N m=64

```

*****

.END

*****

*Voltage levels, input stimulus for analysis at 250mv

*SOURCES 250mv

*****

v0 Gnd 0 dc 0

vclk clk 0 PULSE(0 250m 31.25u 3.125u 3.125u 31.25u 62.5u)

v1 data_input<0> 0 PULSE(0 250m 134.271m 3.125u 3.125u 134m 670m)
v2 data_input<1> 0 PULSE(0 250m 134.271m 3.125u 3.125u 134m 670m)
v3 data_input<2> 0 PULSE(0 250m 134.271m 3.125u 3.125u 134m 670m)
v4 data_input<3> 0 PULSE(0 250m 134.271m 3.125u 3.125u 134m 670m)
v5 data_input<4> 0 PULSE(0 250m 134.271m 3.125u 3.125u 134m 670m)
v6 data_input<5> 0 PULSE(0 250m 134.271m 3.125u 3.125u 134m 670m)
v7 data_input<6> 0 PULSE(0 250m 134.271m 3.125u 3.125u 134m 670m)
v8 data_input<7> 0 PULSE(0 250m 271u 3.125u 3.125u 402m 804m)

vreset reset 0 PWL(0 250m 124.9u 250m 150u 0)

*****

*time parameters for analysis at 250mv

*OPTIONS 250mv

*****

.option post=1

.op all

.TRAN 2.35m tm uic

.param vddpam=250m

.param vddsup=2.5

.param tm=562.8m

```

*Voltage levels, input stimulus for analysis at 350mv

*SOURCES 350mv

v0 Gnd 0 dc 0

vclk clk 0 PULSE(0 350m 5u .5u .5u 5u 10u)

v1 data_input<0> 0 PULSE(0 350m 22.044m .5u .5u 22m 110m)

v2 data_input<1> 0 PULSE(0 350m 22.044m .5u .5u 22m 110m)

v3 data_input<2> 0 PULSE(0 350m 22.044m .5u .5u 22m 110m)

v4 data_input<3> 0 PULSE(0 350m 22.044m .5u .5u 22m 110m)

v5 data_input<4> 0 PULSE(0 350m 22.044m .5u .5u 22m 110m)

v6 data_input<5> 0 PULSE(0 350m 22.044m .5u .5u 22m 110m)

v7 data_input<6> 0 PULSE(0 350m 22.044m .5u .5u 22m 110m)

v8 data_input<7> 0 PULSE(0 350m 44u .5u .5u 66m 132m)

vreset reset 0 PWL(0 350m 19.9u 150m 20u 0)

*time parameters for analysis at 350mv

*OPTIONS 350mv

.option post=1

.op all

.TRAN 385u tm uic

.param vddpam=350m

.param vddsup=2.5

.param tm=92.4m

*Voltage levels, input stimulus for analysis at 350mv

*SOURCES 500mv

v0 Gnd 0 dc 0

vc1k clk 0 PULSE(0 500m 500n 50n 50n 500n 1u)

v1 data_input<0> 0 PULSE(0 500m 2.2044m 50n 50n 2.2m 11m)

v2 data_input<1> 0 PULSE(0 500m 2.2044m 50n 50n 2.2m 11m)

v3 data_input<2> 0 PULSE(0 500m 2.2044m 50n 50n 2.2m 11m)

v4 data_input<3> 0 PULSE(0 500m 2.2044m 50n 50n 2.2m 11m)

v5 data_input<4> 0 PULSE(0 500m 2.2044m 50n 50n 2.2m 11m)

v6 data_input<5> 0 PULSE(0 500m 2.2044m 50n 50n 2.2m 11m)

v7 data_input<6> 0 PULSE(0 500m 2.2044m 50n 50n 2.2m 11m)

v8 data_input<7> 0 PULSE(0 500m 4.4u 50n 50n 6.6m 13.2m)

vreset reset 0 PWL(0 500m 2.099u 500m 2.1u 0)

*time parameters for analysis at 500mv

*OPTIONS 500mv

.option post=1

.op all

.TRAN 1n tm uic

.param vddpam=500m

.param vddsup=2.5

.param tm=9.24m

*Voltage levels, input stimulus for analysis at 350mv

*SOURCES 700mv

```

v0 Gnd 0 dc 0

vclk clk 0 PULSE(0 700m 31.25n 3.125n 3.125n 31.25n 62.5n)

v1 data_input<0> 0 PULSE(0 700m 140.274u 3.125n 3.125n 140u 700u)
v2 data_input<1> 0 PULSE(0 700m 140.274u 3.125n 3.125n 140u 700u)
v3 data_input<2> 0 PULSE(0 700m 140.274u 3.125n 3.125n 140u 700u)
v4 data_input<3> 0 PULSE(0 700m 140.274u 3.125n 3.125n 140u 700u)
v5 data_input<4> 0 PULSE(0 700m 140.274u 3.125n 3.125n 140u 700u)
v6 data_input<5> 0 PULSE(0 700m 140.274u 3.125n 3.125n 140u 700u)
v7 data_input<6> 0 PULSE(0 700m 140.274u 3.125n 3.125n 140u 700u)
v8 data_input<7> 0 PULSE(0 700m 274n 3.125n 3.125n 420u 840u)

vreset reset 0 PWL(0 700m 126.49n 700m 126.5n 0)

*****

*time parameters for analysis at 700mv

*OPTIONS 700mv

*****

.option post=1

.op all

.TRAN 50u tm uic

.param vddpam=700m

.param vddsup=2.5

.param tm=588u

*****

*Voltage levels, input stimulus for analysis at 350mv

*SOURCES 1200mv

*****

v0 Gnd 0 dc 0

vclk clk 0 PULSE(0 1.2 4.6296n 462.9p 462.9p 4.6296n 9.25925n)

```

```

v1 data_input<0> 0 PULSE(0 1.2 20.0041u 462.9p 462.9p 20u 100u)
v2 data_input<1> 0 PULSE(0 1.2 20.0041u 462.9p 462.9p 20u 100u)
v3 data_input<2> 0 PULSE(0 1.2 20.0041u 462.9p 462.9p 20u 100u)
v4 data_input<3> 0 PULSE(0 1.2 20.0041u 462.9p 462.9p 20u 100u)
v5 data_input<4> 0 PULSE(0 1.2 20.0041u 462.9p 462.9p 20u 100u)
v6 data_input<5> 0 PULSE(0 1.2 20.0041u 462.9p 462.9p 20u 100u)
v7 data_input<6> 0 PULSE(0 1.2 20.0041u 462.9p 462.9p 20u 100u)
v8 data_input<7> 0 PULSE(0 1.2 41n 462.9p 462.9p 60u 120u)
vreset reset 0 PWL(0 1.2 18.519n 1.2 18.52n 0)

*****

*time parameters for analysis at 1200mv

*OPTIONS 1200mv

*****

.option post=1

.op all

.TRAN .1u tm uic

.param vddpam=1.2

.param vddsup=2.5

.param tm=65u

*****

*Voltage levels, input stimulus for analysis at 350mv

*SOURCES 2500mv

*****

v0 Gnd 0 dc 0

vclk clk 0 PULSE(0 2.5 1.70648n 170.64p 170.64p 1.70648n 3.412969n)

v1 data_input<0> 0 PULSE(0 2.5 7.3152u 170.64p 170.64p 7.3u 36.5u)

v2 data_input<1> 0 PULSE(0 2.5 7.3152u 170.64p 170.64p 7.3u 36.5u)

```

```

v3 data_input<2> 0 PULSE(0 2.5 7.3152u 170.64p 170.64p 7.3u 36.5u)
v4 data_input<3> 0 PULSE(0 2.5 7.3152u 170.64p 170.64p 7.3u 36.5u)
v5 data_input<4> 0 PULSE(0 2.5 7.3152u 170.64p 170.64p 7.3u 36.5u)
v6 data_input<5> 0 PULSE(0 2.5 7.3152u 170.64p 170.64p 7.3u 36.5u)
v7 data_input<6> 0 PULSE(0 2.5 7.3152u 170.64p 170.64p 7.3u 36.5u)
v8 data_input<7> 0 PULSE(0 2.5 15.2n 170.64p 170.64p 21.9u 43.8u)
vreset reset 0 PWL(0 2.5 7.69n 2.5 7.70n 0)

*****

*time parameters for analysis at 2500mv

*OPTIONS 2500mv

*****

.option post=1

.op all

.TRAN .129u tm uic

.param vddpam=2.5

.param vddsup=2.5

.param tm=31u

```

Appendix D Ocean

Open Command Environment for Analysis (OCEAN) is a text based process that can be run from a UNIX shell or from Virtuoso's Command Interpreter Window (CIW). OCEAN uses Cadence SKILL language to configure the design environment in order to create scripts to automate circuit verification also be useful to run simulations from a non-graphic, remote terminal. SKILL is similar to any other programming language that supports data types, operators, loops, file operators, linked list etc.

```
////////////////////////////////OCEAN Script to Plot the Output Spectrum////////////////////////////////
simulator( 'spectre )
design("/users/eesunz/faculty/cdsemac/cadence/simulation/final_dm_sim/spectre/schematic/netlist/netlist")
resultsDir("/users/eesunz/faculty/cdsemac/cadence/simulation/final_dm_sim/spectre/schematic" )
modelFile("/export/cadence/linux/tools.lnx86/dfII/local/ncsu-cdk-1.6.0.beta/models/hspice/public/tsmc25dN.m" "")
'("/export/cadence/linux/tools.lnx86/dfII/local/ncsu-cdk-1.6.0.beta/models/hspice/public/tsmc25dP.m" ""))
analysis('tran ?stop "120m" ?errpreset "liberal" ?method "gear2"?relref "sigglobal"
?compression "yes" ?strobeperiod "5u" )
converge( 'ic "/ls1out" "0" )
converge( 'ic "/ls2out" "0" )
temp( 27 )
run()
selectResult( 'tran )
plot(getData("/outls2filter") getData("/outls1filter") getData("/ls2out") getData("/ls1out")
getData("/reset") getData("/clk") getData("/data_input<7>") getData("/data_input<6>"))
```

```
getData("/data_input<5>") getData("/data_input<4>") getData("/data_input<3>")  
getData("/data_input<2>") getData("/data_input<1>") getData("/data_input<0>") )
```

Vita

Praveen Palakurthi earned his Bachelor of Technology degree in Electronics and Communication Engineering from Jawaharlal Nehru Technological University, India in 2005. He received his Master of Science in Electrical and Computer Engineering in 2009 from The University of Texas at El Paso. In 2010, he joined the doctoral program in Electrical and Computer Engineering at The University of Texas at El Paso.

Dr. Palakurthi has been the recipient of Texas Instruments Foundation Endowed Scholarship (TIF) and Texas public Education Grant (TPEG). While, pursuing his degree, Dr. Palakurthi worked as research associate and teaching assistant for the department of Electrical and Computer Engineering. He interned at ARM from fall 2012 to fall 2013 and is currently working for INF Microsensors based in San Diego, CA.

Dr. Palakurthi has presented his research in IEEE Subthreshold Microelectronics Conference and Journal of Low Power Electronics and Applications. Dr. Palakurthi's dissertation, *Ultra-Low Power, Robust Digital to Analog Converter*, was supervised by Dr. Eric MacDonald.

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