

2014-01-01

Growth And Analysis Of Micro And Nano CdTe Arrays For Solar Cell Applications

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GROWTH AND ANALYSIS OF MICRO AND NANO CDTE ARRAYS FOR
SOLAR CELL APPLICATIONS

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Brandon Aguirre

2014

Dedication

To my family

GROWTH AND ANALYSIS OF MICRO AND NANO CDTE ARRAYS FOR
SOLAR CELL APPLICATIONS

by

BRANDON ADRIAN AGUIRRE, BSEE, MSEE

DISSERTATION

Presented to the Faculty of the Graduate School of

The University of Texas at El Paso

in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

Department of Electrical and Computer Engineering

THE UNIVERSITY OF TEXAS AT EL PASO

December 2014

Acknowledgements

I would like to thank God Jehovah for giving me the opportunity to live and finish my doctoral degree in electrical engineering. I would like to thank my family for all their support and encouragement during my doctoral studies. I would like to thank each member of my dissertation committee; Dr. David Zubia, Dr. Jose Luis Cruz-Campa, Dr. John McClure and Dr. Stella Quinones for their guidance, mentorship and time dedicated to me. Special thanks to my advisors Dr. David Zubia and Dr. Jose Luis Cruz-Campa for sharing their research experience, friendship and advice.

I would like to thank our collaborators in Sandia National Labs and the Center for Integrated Nanotechnologies (CINT). Also, I would like to thank Yasemin Kutes and Dr. Bryan Huey from University of Connecticut. I was privileged to collaborate and learn from all of them.

I would like to thank current members (Jose Chavez, Damian Marrufo, Aldo Vidana, Luis Garcia, Sergio Almeida, Rodolfo Aguirre, Arka Talukdar, Cesar Valle, Cheik Sana) and past members of the NanoMIL lab at UTEP. Their support, training, discussions and hard work contributed to the successful completion of my dissertation work.

Finally I would like to thank the following sources of funding that supported me through my doctoral studies: The NSF LSAMP Bridge to the Doctorate Fellowship, The NSF Solar Economy IGERT fellowship, the HENAAC Robert and Debbie Amezcua scholarship, the National Institute of Nano Engineering and the Department of Energy (DOE).

Abstract

CdTe is an excellent material for infrared detectors and photovoltaic applications. The efficiency of CdTe/CdS solar cells has increased very rapidly in the last 3 years to ~20% but is still below the maximum theoretical value of 30%. Although the short-circuit current density is close to its maximum of 30 mA/cm², the open circuit voltage has potential to be increased further to over 1 Volt. The main limitation that prevents further increase in the open-circuit voltage and therefore efficiency is the high defect density in the CdTe absorber layer. Reducing the defect density will increase the open-circuit voltage above 1 V through an increase in the carrier lifetime and concentration to $\tau > 10$ ns and $p > 10^{16}$ cm⁻³, respectively. However, the large lattice mismatch (10%) between CdTe and CdS and the polycrystalline nature of the CdTe film are the fundamental reasons for the high defect density and pose a difficult challenge to solve.

In this work, a method to physically and electrically isolate the different kinds of defects at the nanoscale and understand their effect on the electrical performance of CdTe is presented. A SiO₂ template with arrays of window openings was deposited between the CdTe and CdS to achieve selective-area growth of the CdTe via close-space sublimation. The diameter of the window openings was varied from the micro to the nanoscale to study the effect of size on nucleation, grain growth, and defect density. The resulting structures enabled the possibility to electrically isolate and individually probe micrometer and nanoscale sized CdTe/CdS cells. Electron back-scattered diffraction was used to observe grain orientation and defects in the miniature cells. Scanning and transmission electron microscopy was used to study the morphology, grain boundaries, grain orientation, defect structure, and strain in the layers. Finally, conducting atomic force microscopy was used to study the current-voltage characteristics of the solar cells. An important part of this work was the ability to directly correlate the one-to-one relationship between the electrical performance and defect structure of

individual nanoscale cells. This method is general and can be applied to other material systems to study the electrical-microstructure relationship on a one-to-one basis with nanoscale resolution.

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Chapter 1: Introduction

The world consumption of energy represents a big challenge for the most highly-used energy sources. World energy consumption has been increasing every year for the last 30 years. There are different energy sources that supply the demand of energy, but the ones more often used are oil, natural gas and coal. Figure 1 shows a graph of world energy consumption in million tonnes oil equivalent versus time [1]. Figure 1 also shows the different sources of energy and how much they are used. Importantly, the finite sources of energy are the most used, and the infinite sources of energy are the least used by humanity.

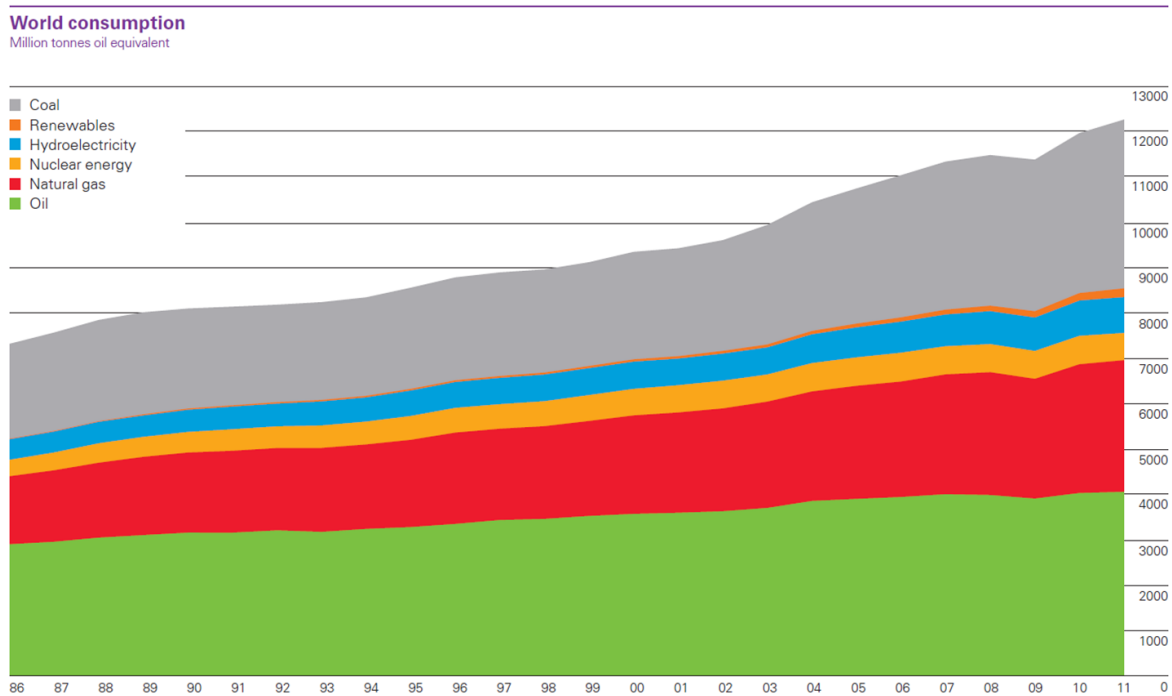


Figure 1 Shows the world energy consumption in million tonnes oil equivalent versus time [1].

A comparison between the total amount of energy provided by finite sources and the amount of energy per year provided by infinite energy sources is shown in Figure 2. Every year, the amount of energy from finite sources is reduced; this means that the circles on the right side of Figure 2 are reduced every year. World energy consumption exceeds most of the energy

available from renewable sources per year. However, the available energy from the sun every year is remarkably greater than any other source of energy.

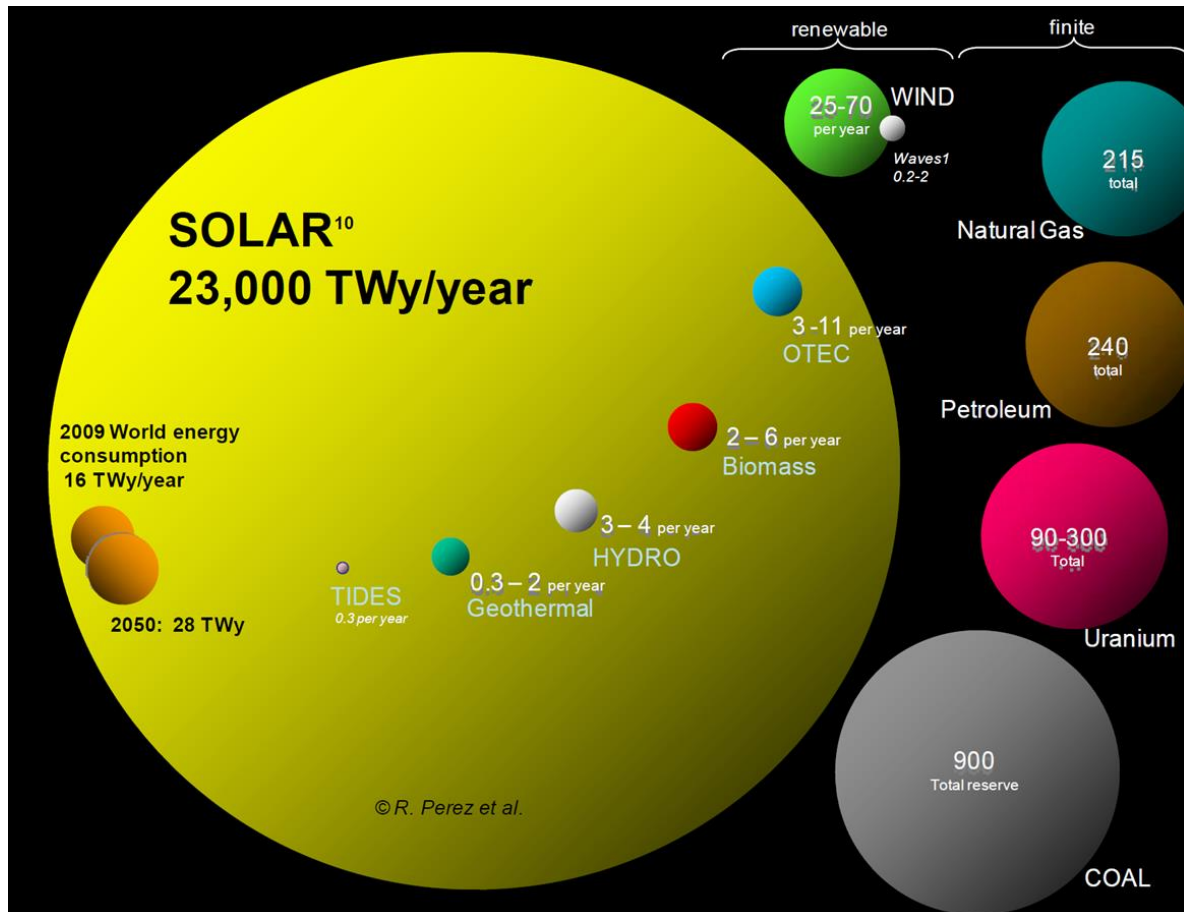


Figure 2 Shows a comparison between world energy consumption per year, renewable energy available per year and total amount of energy available from finite sources of energy. [2]

Photovoltaics (PVs) offer an excellent opportunity to transform solar energy into electrical energy. Photovoltaics use the photovoltaic effect to convert sunlight directly into electricity. PVs are clean, use a form of renewable energy, require relatively little maintenance and are noise-free.

There are different kinds of PV technologies, and CdTe-based PV is one of them. One of the main advantages of CdTe-based PVs is low cost; however, their efficiency is still low compared to the maximum theoretical efficiency they can attain. The low efficiency seen in

CdTe solar cells results from the low values of voltage caused by low quality material. If material properties could be studied and correlated to electrical performance, the CdTe quality could improve by eliminating defects that cause low voltages.

1.1 Contribution of this Thesis

This work creates a method to study the effect of defects on the electrical performance of any grown semiconductor material. In this case CdTe-based solar cells were studied. This method offers the unique capability of making a one-to-one correlation between material properties and electrical performance at the micro- and nano-scale levels. Besides providing a method to correlate material to electrical properties, this technique could be used to reduce the defect density in CdTe and contribute to efficiency increment in CdTe solar cells.

Chapter 2: Technical Background

2.1 Benefits of Solar Cells

Of all energy sources, solar energy is the most abundant [3] and it can be transformed to electric energy through photovoltaics (PV's). PV's consume energy and emit greenhouse gasses during the following stages of their life cycle: manufacturing process, module assembly, material transportation, installation, and system disposal or recycling [4]. However, when evaluating the life cycle of different PV systems, CdTe PV systems have the best performance in terms of energy payback time (EPBT) and greenhouse gasses (GHG) emission rate [4].

2.2 Properties of CdTe

CdTe is an ideal material for photovoltaics due to its excellent electrical and optical properties. Its 1.5 eV bandgap and high absorption coefficient make it ideal to absorb more than 90% of the light within a few micrometers of material. CdTe solar cells have a maximum theoretical efficiency of 30%, and several increases in record efficiency have been reported in the last three years after a 17-year plateau [5].

2.3 History of CdTe Solar Cells

The first studies of CdTe as a semiconductor date back to the 1950's when it was discovered that CdTe could act as a p-type material with a bandgap of 1.45 eV [6]. Since then, CdTe has been used to fabricate solar cells with efficiencies of 6% in 1963 [7], 10% in 1982 [8], 15.8% in 1993 [9] and an increase of 17%-21% in the last four years [10-13]. Figure 3 shows the record efficiency CdTe solar cells for the last 25 years and the name of the company, laboratory or university who fabricated them. It can also be seen in Figure 3 that there is still room to improve the efficiency of CdTe solar cells.

CdTe solar cells efficiencies over time

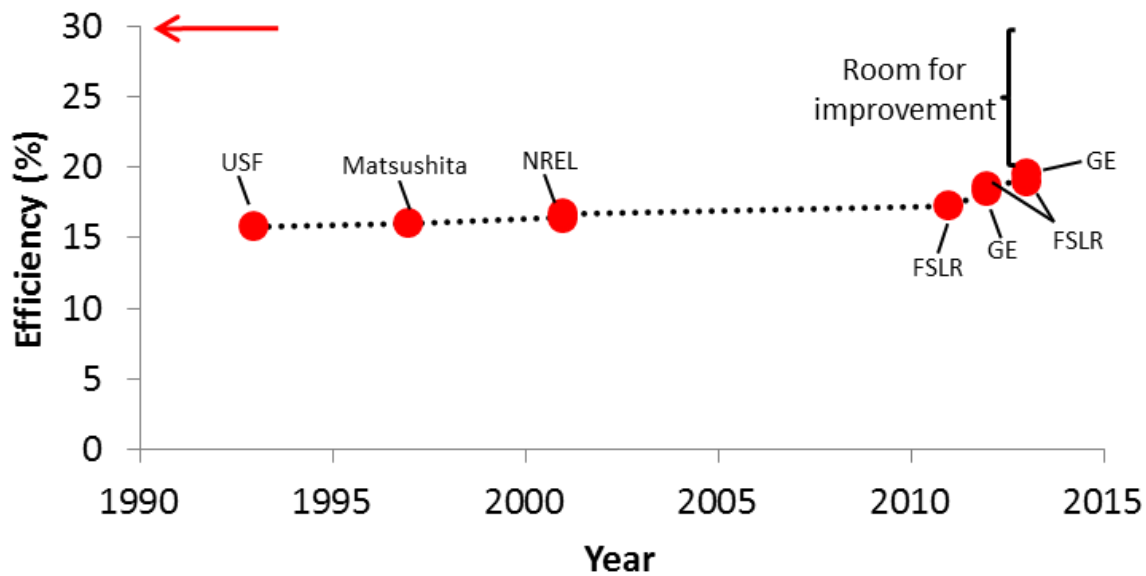


Figure 3 Shows the efficiency of CdTe solar cells over time for the last 25 years [10].

2.4 J_{sc} IN CdTe SOLAR CELLS

To achieve the conversion efficiencies in Figure 3, the majority of the optical losses have been reduced by preventing light absorption in the glass, window layer and front contact [10]. When optical losses are reduced, quantum efficiency and short circuit current (J_{sc}) increase and the overall conversion efficiency of solar cells increase. Improvements in quantum efficiency (QE) are shown in Figure 4. As the QE curve becomes higher and wider, less light is lost by absorption in glass, indium tin oxide (ITO) or CdS layers. The direct impact on conversion efficiency by an increase in QE is also mentioned in the legend of Figure 4. Conversion efficiencies increased from 16.7% to 18.7% by enhancing the absorption of high energy photons with wavelengths below 500 nm.

The history for short circuit current in CdTe record solar cells is shown in Figure 5. The increment in values of J_{sc} has resulted in values close to the maximum theoretical limit of about

30.5 mA/cm² [14]. Figure 5 also shows that the room for improvement in J_{sc} is small compared to the room for improvement in conversion efficiency of Figure 3.

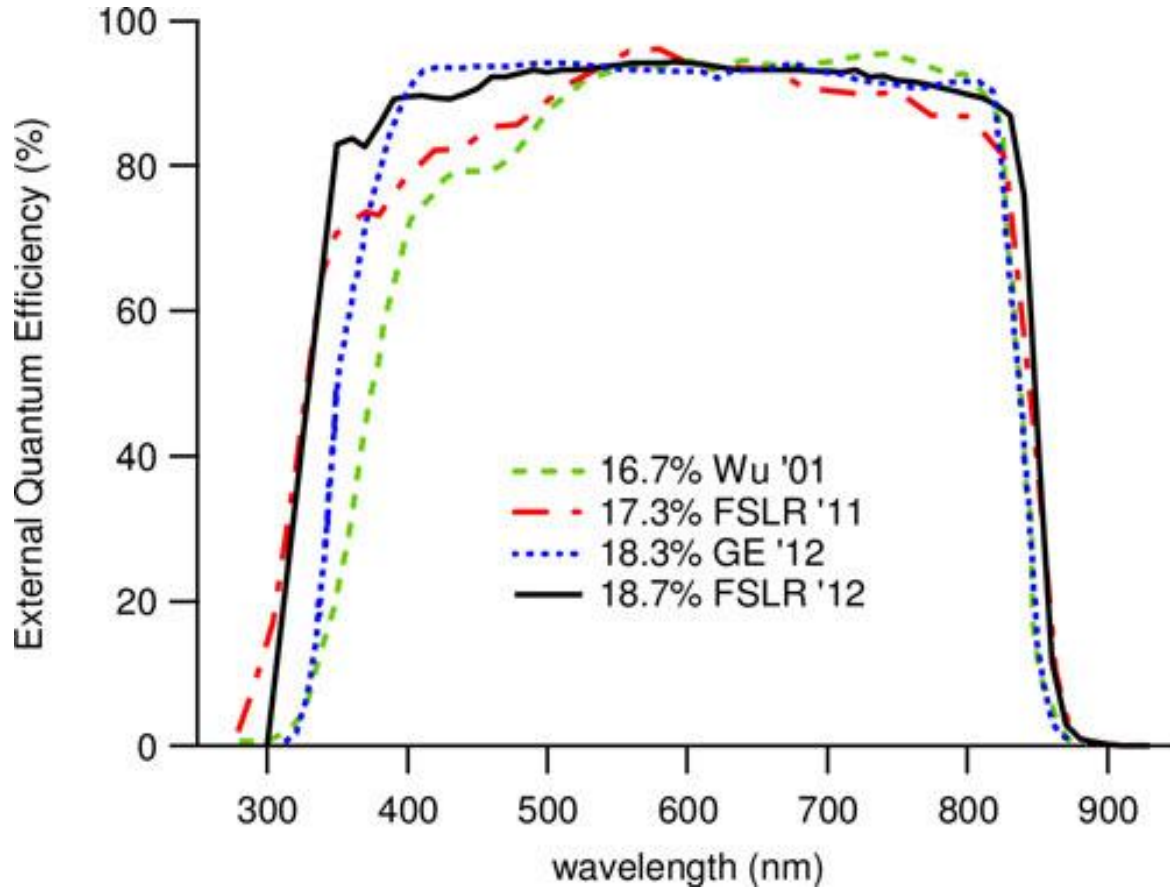


Figure 4 Shows the increment in quantum efficiency and its impact on conversion efficiency for CdTe solar cells [10].

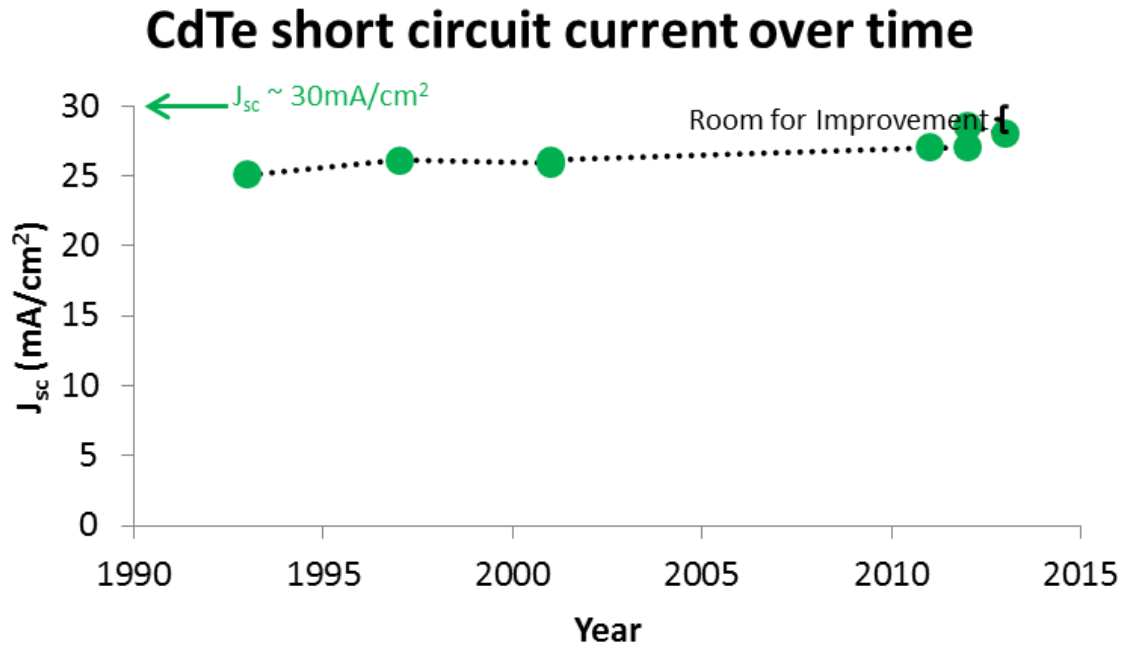


Figure 5 Shows the corresponding J_{sc} for each of the record efficiencies in Figure 3.[10]

2.5 V_{oc} IN CdTe SOLAR CELLS

For all the world record efficiencies shown in Figure 3 since 1993, the open circuit voltage (V_{oc}) did not have a substantial increment and fluctuated between 843 mV and 852 mV [10]. Figure 6 shows the values of V_{oc} obtained for record CdTe solar cells. It can be seen that V_{oc} values are still far from the theoretical limit of 1.1 V and there is more room for improvement compared to the J_{sc} . Losses in V_{oc} have been attributed to low doping levels, carrier recombination, and inhomogeneity of the CdTe grains [10, 15, 16]. If any of these loss mechanisms could be suppressed, the increment of V_{oc} would have an immense impact on the conversion efficiency of CdTe solar cell devices.

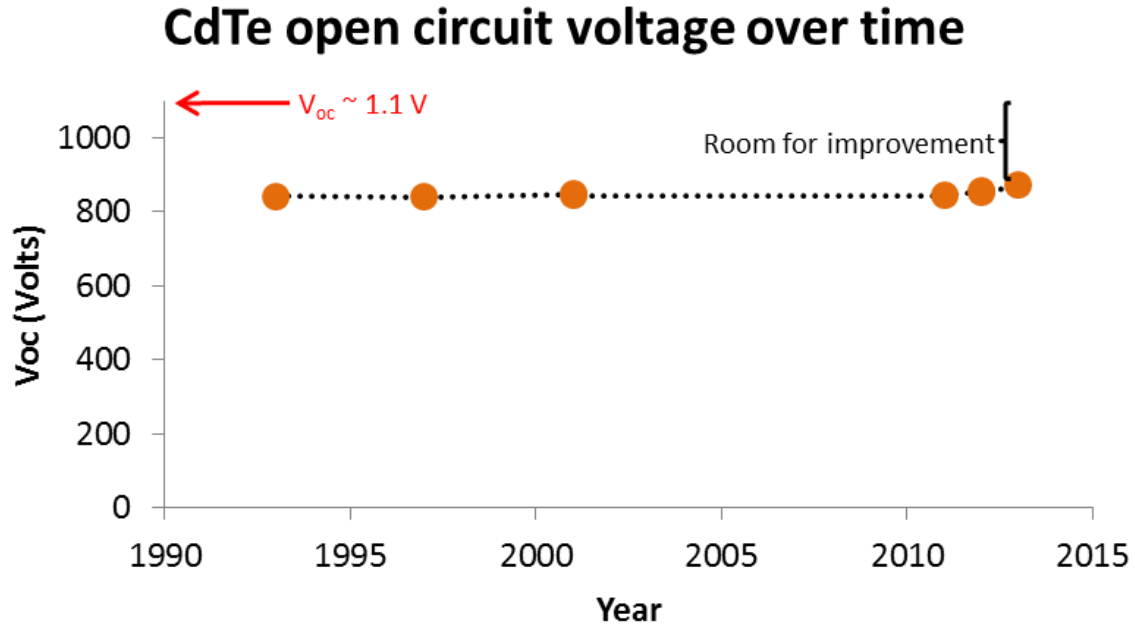


Figure 6 Shows the values of V_{oc} for the record efficiency solar cells in Figure 3 [10].

2.5.1 Effect of Material Quality on V_{oc}

The effect of material quality on V_{oc} is manifested through various mechanisms which include carrier recombination velocity in the space-charge and neutral regions, carrier concentration, and carrier lifetime. The effect of carrier recombination velocity and carrier concentration can be observed by studying the V_{oc} equation for a one-sided abrupt n^+ -p junction. In this device, the built-in voltage can be expressed as

Equation 1
$$V_{bi} = E_g - \frac{kT}{q} \ln \left(\frac{N_v}{p} \right)$$

where E_g is the bandgap, k is the Boltzmann's constant, T is the temperature, q is the charge of an electron, N_v is the effective density of states in the valence band, and p is the hole concentration. If it can be assumed that complete acceptor ionization is achieved then $p \approx N_A$ where N_A is the acceptor concentration. However, it is well known that in polycrystalline CdTe thin-films a significant degree of compensation occurs due to the high level of defects so usually

$p < N_A$ in thin film solar cells. Either way, the expression for V_{bi} shows that the built-in voltage increases as p increases. Assuming that the current in a CdTe solar cell is dominated by space-charge recombination, the current can be expressed as [14]:

$$\text{Equation 2} \quad J = J_{oo} e^{-qV_{bi}/AkT} e^{qV/AkT} - J_L$$

where A is the ideality factor, J_L is the photocurrent, and the saturation current J_{oo} is given by recombination in the space-charge region,

$$\text{Equation 3} \quad J_{oo} = qp v_r$$

where v_r is the recombination velocity in the space-charge region. Combining the last 3 equations and setting the current equal to zero, $J = 0$, one can solve for the open circuit voltage, V_{oc} as follows,

$$\text{Equation 4} \quad V_{oc} = E_g - \frac{AkT}{q} \ln \left(\frac{q\sqrt{N_v}}{J_L} v_r \sqrt{p} \right)$$

Typical material and device values for CdTe solar cells are $E_g = 1.45$ eV, $N_v = 1.8 \times 10^{19} \text{ cm}^{-3}$, $J_L = 29 \text{ mA/cm}^2$, and $A = 2$ for recombination dominated current. V_{oc} is plotted below in in Figure 7 as a function of the recombination velocity and parameterized by the hole concentration. It is observed that V_{oc} generally increases with slower recombination velocity and lower hole density. This indicates that material with low defect density in the space-charge region is highly desirable to obtain a high V_{oc} . Counterintuitively, Figure 7 also predicts that a lower hole density is desirable although a lower p will reduce V_{bi} as shown above. However if it is assumed that the hole density and recombination velocity are interrelated such that p decreases when v_r increases according to $p = C/v_r$, then the model predicts (black trace in Figure 7) that a slow v_r and high p are required to obtain high V_{oc} in agreement with intuition. The important point is that high quality material is required in the space-charge region to reduce recombination *and* in the neutral region to increase the hole concentration through a reduction in compensation. However due to

the large lattice mismatch between CdTe and CdS (~10%), achieving low-defect density at or near the interface is a challenging task.

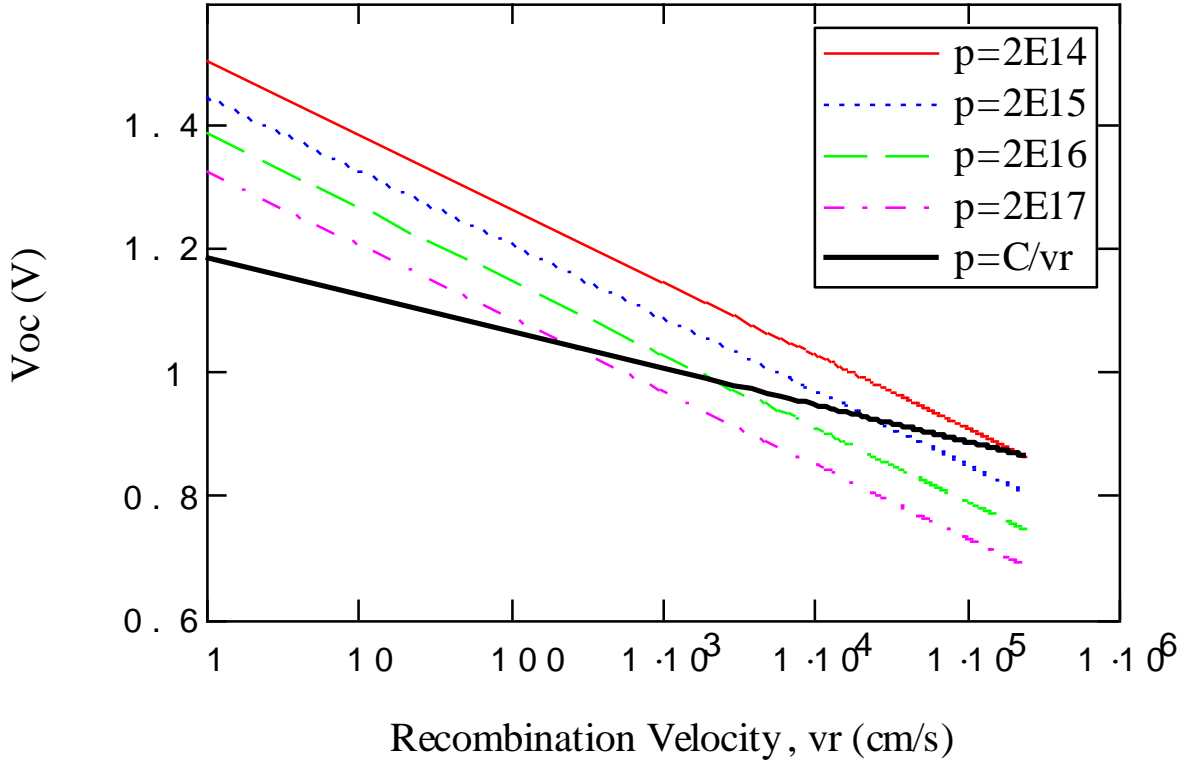


Figure 7 Open circuit voltage as a function of recombination velocity for different hole concentrations.

Sites and Pan performed simulations of V_{oc} as a function of carrier lifetime and carrier concentration. In one simulation, when the carrier concentration was set to a typical value of $2 \times 10^{14} \text{ cm}^{-3}$, the V_{oc} increased with carrier lifetime but was limited by the value of V_{bi} which is set by the hole concentration as indicated by Equation 1. In other words, V_{oc} “is limited by the separation of the quasi-Fermi levels”. [15] Therefore it is important to ensure that V_{bi} is made as close to E_g as possible without degrading carrier lifetime. This was confirmed by a second simulation where the carrier concentration was set to $2 \times 10^{17} \text{ cm}^{-3}$; in this case a higher V_{oc} was predicted due to the higher V_{bi} . The conclusion is that a high carrier concentration (p) and high

carrier lifetime (τ) are *both* needed to achieve a high V_{oc} . Physically this implies that the defect density in the CdTe should be low to minimize carrier compensation and density of traps.

2.6 EFFECT OF INHOMOGENEITY ON EFFICIENCY

Inhomogeneity in CdTe grains is another source of low efficiency in CdTe solar cells [16]. CdTe is usually grown as a polycrystalline thin film. Each grain in a polycrystalline CdTe film has different electrical properties, and each grain could be modeled as an independent pn junction diode. Therefore, the electrical performance of a CdTe solar cell would equal the composite behavior of all CdTe grains that form the solar cell. This means that good and bad CdTe grains or diodes are connected through a polycrystalline film, and the bad diodes act as loads to the good diodes. For example using Karpov's model of diodes in parallel [16], it is anticipated that the current-voltage (I-V) characteristic is affected by the variation in the diode parameters. Figure 8 plots the modeled I-V characteristic of 21 diodes. The red (bold) curve is the I-V of all the diodes connected in parallel. In this analysis the reverse saturation current was varied from 1 – 11 nA/cm². The other parameters (ideality factor, shunt and series resistance and photo current) were set to model the 16.5% record cell reported by Wu, *et al.* [17]. Indeed the model predicted 16.5% efficiency and is the dashed curve with the highest open-circuit voltage in Figure 8 (a,b,d). Notice however that if the reverse saturation current of the 21 diodes degrade linearly the combined effect is that the efficiency is reduced to 14.4% as shown by the red (bold) curve in Figure 8 (a). The dashed black curve to the left of the red curve is the diode with the worst reverse saturation current. Moreover, if one of the 21 diodes suffers a catastrophic short (2 W-cm²), the efficiency is reduced to 8.8% as shown in Figure 8 (b). This one diode represents 4.7% (1/21) of the diode area but has the effect of reducing the efficiency by approximately one-half. A confounding effect is that the efficiency can be increased by worsening (increasing) the series resistance! This is shown in Figure 8 (c) where the efficiency increases from 8.8% to 10.0% when the series resistance is increased from 1 to 3 W-cm². Finally, Figure 8 (d) shows the

effect of one diode having an extremely poor reverse saturation current. Here the efficiency is not only reduced but also the knee of the red (bold) curve is much broader. Notice also that this cell will be severely forward biased under max power-point operation causing heating and degradation. [18].

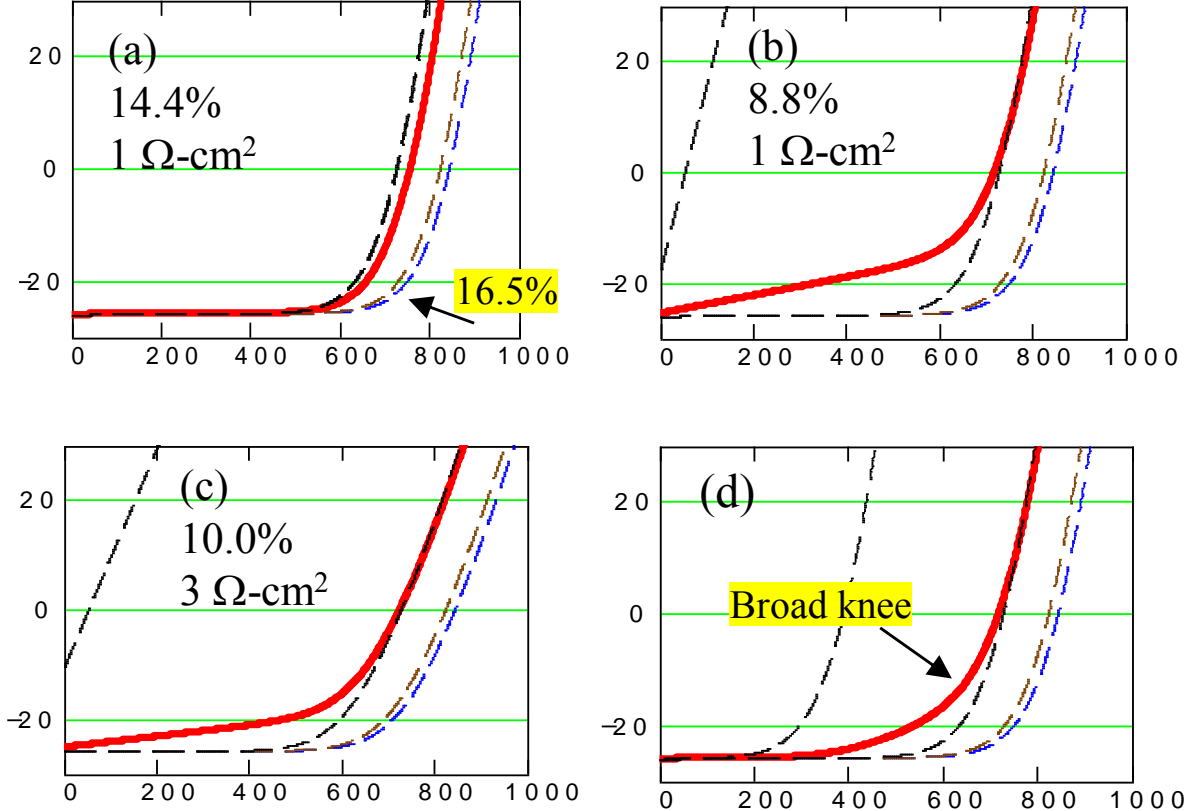


Figure 8 (a)-(d) These plots model the I-V characteristic of diodes. The vertical axis is I (mA/cm^2) and the horizontal axis is V (mV).

2.7 APPROACHES IN LITERATURE TO MITIGATE THE EFFECT OF DEFECTS IN CdTe

Examples of defects in CdTe formed due to the CdS/CdTe lattice mismatch are misfit dislocations. Misfit dislocations accommodate any misfit that is not removed by elastic strain [19]. Other defects found in CdTe films are stacking faults, twins, and grain boundaries [20]. Twin boundaries affect the electrical performance of CdTe [21], and grain boundaries act as recombination centers and as a medium for diffusion of impurities [22]. Post-deposition

treatments are usually employed to mitigate these defects in CdTe films. CdCl₂ treatments have been used very effectively to increase the efficiency of solar cells from less than 2% to more than 10% [23]. CdCl₂ is believed to electrically passivate grain boundaries, promote recrystallization and grain growth [24, 25]. CdCl₂ could also form n-type grain boundaries (GB's) by substituting Te with Cl atoms; thus forming p-n-p junctions that help to separate carriers between CdTe grains and GB's [26]. Alternatively, MgCl₂ has given very good results as a non-toxic alternative to CdCl₂ for the activation step [23].

2.8 TECHNIQUES USED IN LITERATURE TO STUDY DEFECTS IN CdTe

Many studies are underway to understand defects and their impact on device performance. The work by Li, et al., use scanning transmission electron microscopy (STEM), electron beam induced current (EBIC) and electron backscatter diffraction (EBSD) to correlate atomic structure to electrical activity [27]. Mountinho and coworkers have used conductive atomic force microscopy (C-AFM) to correlate the current-voltage (I-V) characteristics of polycrystalline regions to intra-grain and grain-boundary morphologies [28, 29]. In another study, Mountinho used focused ion beam (FIB) marks to correlate grain structure via EBSD with cathodoluminescence of the exact same areas [30]. However, all of these studies were performed on polycrystalline films with little effort to prevent the formation of defects from the onset. Moreover, it is difficult to de-convolute the effect of various defects (point, linear, areal) on device electrical performance.

2.9 PROPOSED TECHNIQUES TO ANALYZE AND REDUCE DEFECTS IN CdTe

Nanoheteroepitaxy is a technique that uses selective area growth (SAG) to reduce the defect density on mismatched materials by three-dimensional strain distribution and substrate compliance [31]. A reduction in defect density has been reported in silicon and GaAs systems

[31]. In CdTe, SAG has been studied only at the micro-scale level on polycrystalline substrates [32],[33].

In this work, we propose SAG of CdTe as a template to study the effect of defects on the electrical performance of CdTe. SAG produces physically and electrically isolated CdTe islands that can be indexed and individually probed for electrical performance and atomic structure analysis. The schematic in Figure 9 shows the fabrication process after a polycrystalline CdS film is deposited on glass/ITO substrates. The first step is to deposit a SiO_2 layer on top of the CdS (Figure 9 (b)), then pattern the SiO_2 film, and finally grow CdTe, selectively, inside each window.

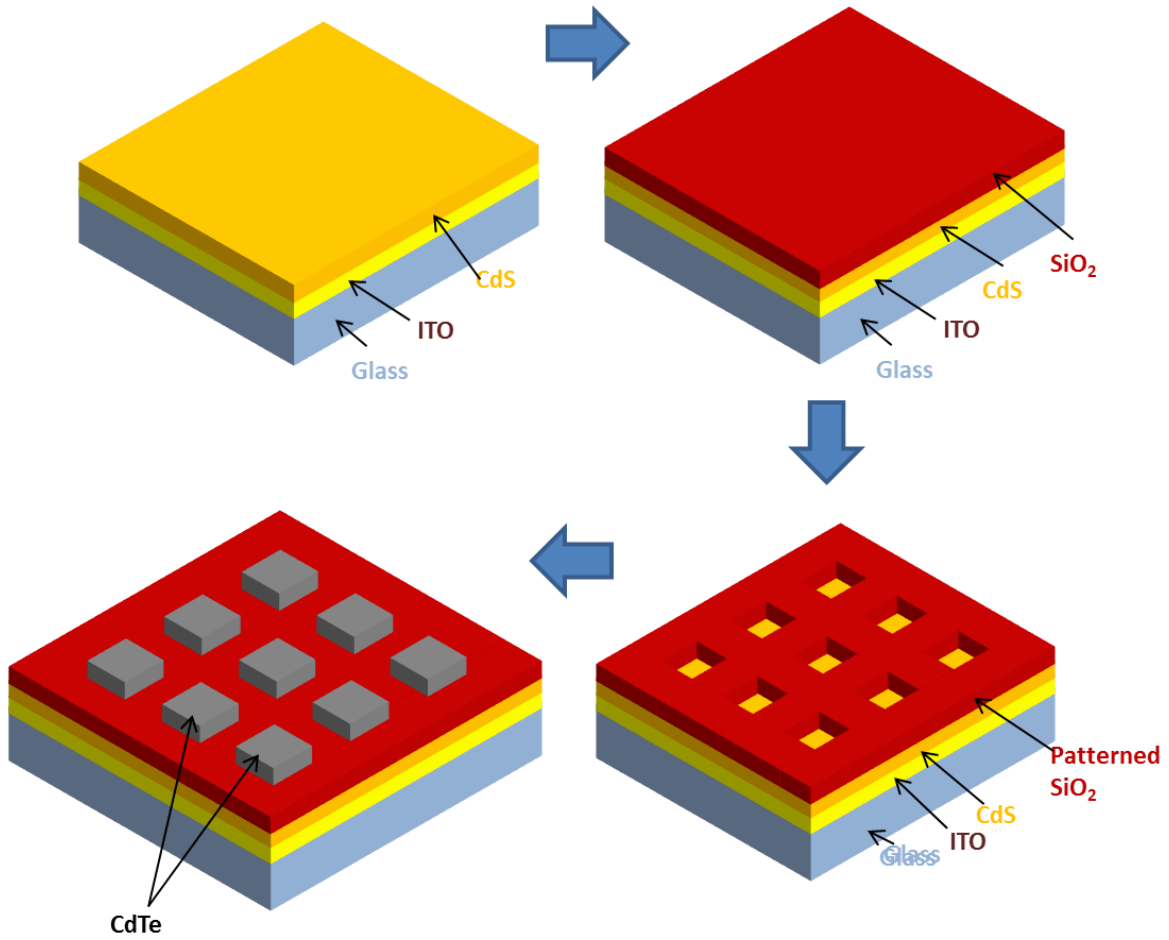


Figure 9 Schematic of the glass/ITO substrates after: (a) CdS deposition, (b) SiO_2 deposition, (c) patterning and (d) selective deposition of CdTe.

A focused ion beam (FIB) system was used to remove material from the sample and make micro and nano-marks as shown in Figure 10. The micro marks were used to identify an area of interest using low-magnification SEM and the optical microscope in the AFM. The nano-marks were used to locate specific islands with SEM, FIB and AFM for sample preparation and electrical characterization.

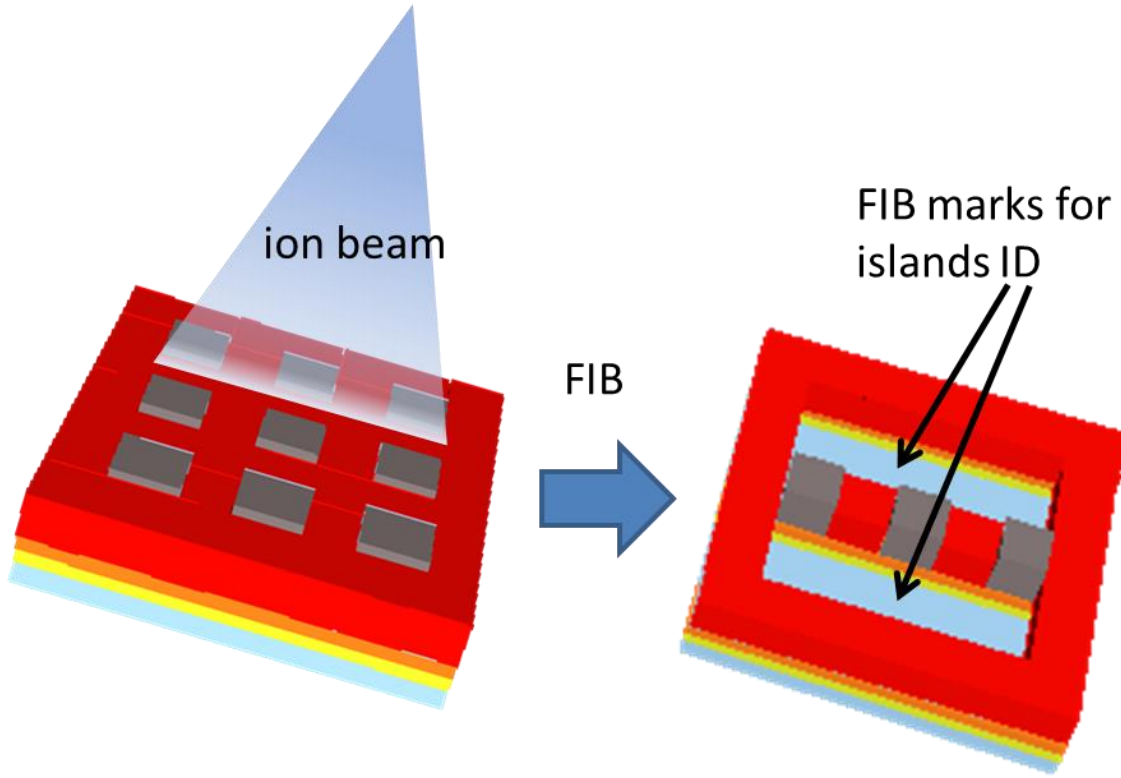


Figure 10 Schematic of SAG of CdTe and the FIB process used to make marks for island indexing and identification

SAG of CdTe provides a unique configuration that offers the possibility to probe electrically isolated CdTe grains to understand the relationship between processing, atomic structure and electrical performance. A conducting-AFM (C-AFM) was proposed to be used for electrical characterization as shown in Figure 11. C-AFM provides spatial resolution to test micro and nano-islands separately. J-V characteristics under dark or light conditions can be measured from single CdTe islands. Also, C-AFM provides electric current maps to electrically

test several islands in a relatively short amount of time. This is particularly helpful when initially screening and find islands with very different electrical behavior without the need to test each one individually.

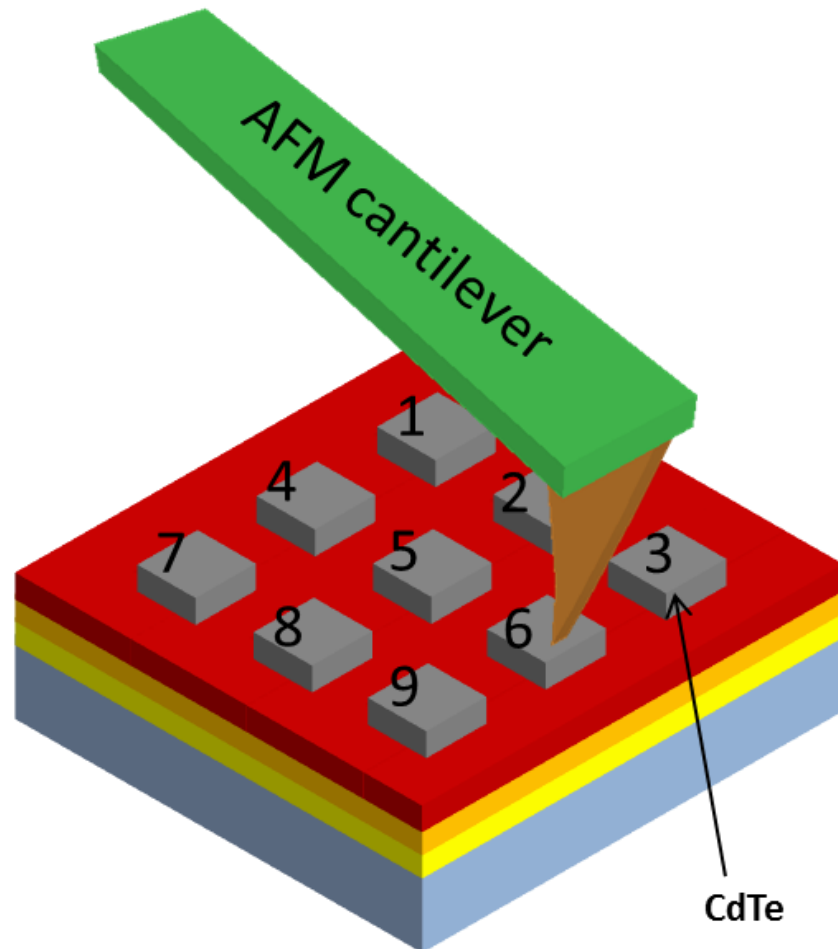


Figure 11 Schematic showing an AFM cantilever to probe single and isolated CdTe islands.

To study the microstructure properties of CdTe arrays, we propose to use EBSD and TEM. From EBSD, the grain orientation can be found as well as the number of grains and grain boundaries per CdTe island. TEM provides detailed information on the types of defects at the atomic scale, the nature of the interface and the bulk of the material. EBSD and TEM analysis

require prior sample preparation. In the case of EBSD, the surface of the sample needs to be planarized. “A well prepared sample is prerequisite to obtaining a good diffraction pattern. Surfaces must be sufficiently smooth to avoid forming shadows on the diffraction pattern from other parts of the sample” [34]. An FIB system was used to planarize the CdTe islands as shown in Figure 12 (a). In the case of TEM, a thin lamella needs to be prepared for atomic scale analysis. The standard lift-out process was proposed to prepare very thin foils that contain CdTe islands as shown in Figure 12 (b). Crystallographic and atomic scale data were obtained for CdTe islands analyzed with EBSD and TEM.

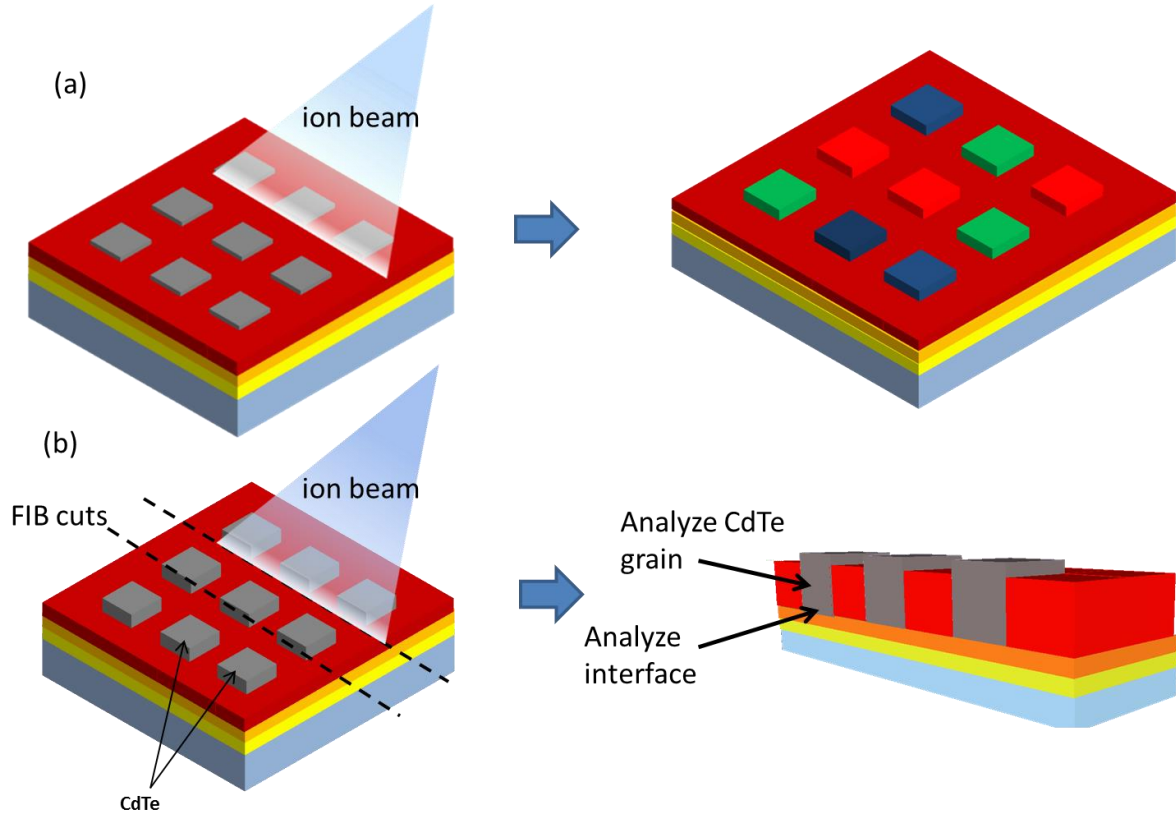


Figure 12 Schematics of the sample preparation for (a) EBSD and (b) TEM.

Chapter 3: Fabrication and Processing

3.1 THIN FILM CdS GROWTH

CdS was deposited via chemical bath deposition on commercially obtained indium tin oxide (ITO)-coated glass wafers (CG-411N-DF100/0.7; Delta Technologies, USA). The glass wafers were 100 mm in diameter and 0.7 mm in thickness with a 4–8 Ω /square ITO sheet resistance. Prior to CdS deposition, the wafers were cleaned in a high-pH ammonium hydroxide and hydrogen peroxide solution to produce a negative charge on the surface and to assist in the dense heterogeneous nucleation of CdS on the wafer surface. A novel CdS deposition process was used that allows the real-time, in situ monitoring and control of the free Cd^{2+} molarity above 10^{-7} M at 60 °C. Uniform 80- to 90-nm-thick CdS films were obtained using this process. [35] Figure 13 shows the nanocrystalline structure of a typical film with grain size on the order of ≤ 50 nm and a surface roughness of 3 nm. Following deposition, the glass/ITO/CdS substrates were then soaked in isopropyl alcohol for 5 minutes, rinsed in DI water, and dehydrated for 15 minutes at 150 °C.

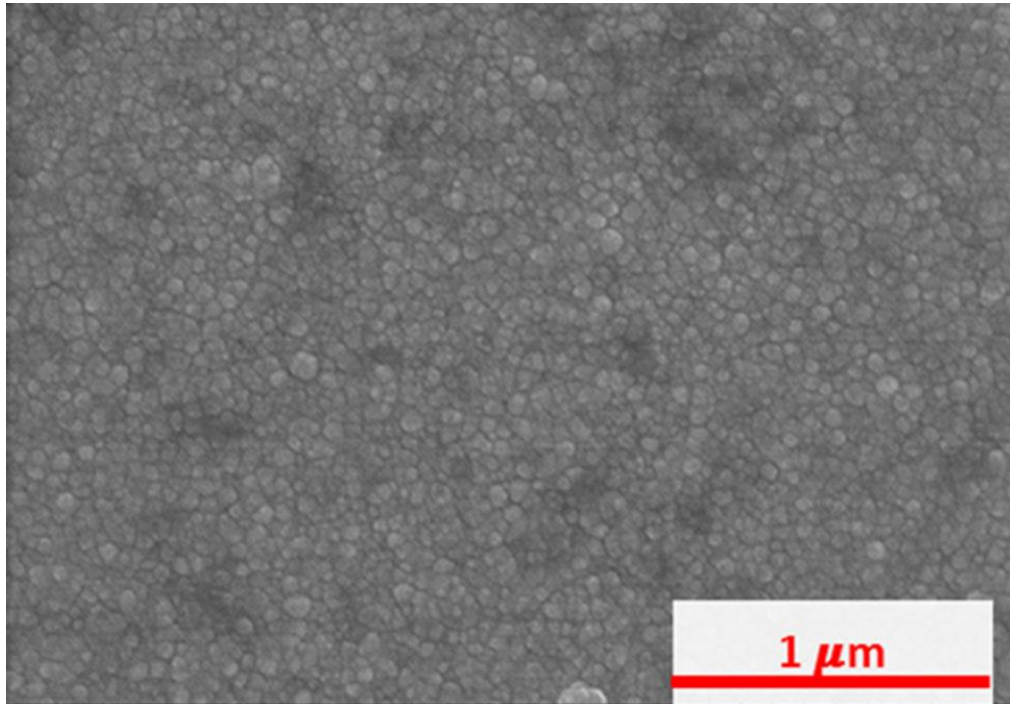


Figure 13 SEM plan view of a typical CdS film microstructure.

3.2 MICRO AND NANO-PATTERN FABRICATION

SiO_2 micro and nano-windows were fabricated on CdS substrates using four different patterning techniques as shown in Figure 14. Each patterning technique created windows of different sizes. The larger windows were fabricated using standard optical lithography. The smaller windows were made using more sophisticated techniques, such as nano-imprint lithography (NIL), interferometry, and electro-beam lithography.

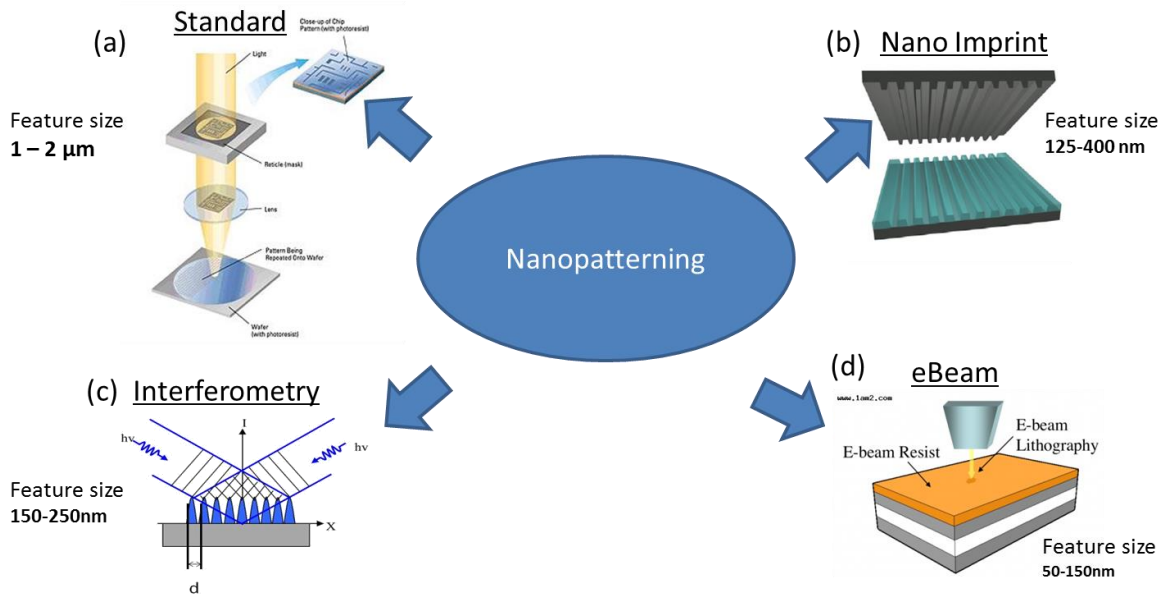


Figure 14 Schematics of four different patterning techniques a) standard, b) nano imprint, c) interferometry, and d) electron beam lithography used to create SiO_2 windows from 2- μm to 136-nm sizes [36-38].

3.2.1 Optical and Nano-imprint Lithography

Si_3N_4 and SiO_2 were used as masking materials for selective area deposition (SAG) of CdTe on Si (100) and CdS substrates, respectively. Plasma-enhanced chemical vapor deposition (PECVD) was used to deposit a 200-nm-thick Si_3N_4 film on Si substrates. Optical lithography then was used to pattern the film and create micrometer sized windows for subsequent SAG of CdTe. A layer of SiO_2 was deposited on the CdS and then patterned to expose the CdS layer underneath as shown in Figure 15. The SiO_2 layer served as a selective-growth mask to deposit isolated CdTe islands on the CdS. Samples with 2- μm and 300-nm-sized holes were created to

compare the effect of patterning scale on subsequent CdTe crystal growth. The samples with the 2- μm windows were created by depositing 200-nm-thick SiO_2 via PECVD and then patterned using optical lithography as shown in Figure 15 (a). In contrast, nano-imprint lithography was used to create the samples with the 300-nm windows. In this process, 460-nm-thick SiO_2 was first deposited by PECVD. A reverse-tone step and flash imprint lithography (S-FIL/R) process was then applied to nanopattern the SiO_2 using a lithography tool (Imprio-100; Molecular Imprints Inc., USA). A general description of the S-FIL/R nano-imprint lithographic (NIL) technique is given in reference. [39] An important step in NIL is the parallel alignment between the template (which contains the pattern) and substrate. Due to the relatively large surface roughness of the CdS (~ 3 nm), the transfer (110 nm) and resist (300 to 500 nm) layers were much thicker than usual to overcome the rough surface. 16 N of force, which is larger than usual, was used to press the template against the resist for 120 seconds. A mixture of 20 sccm of CHF_3 and 15 sccm of Ar was used to etch the SiO_2 and gave excellent etch selectivity with respect to the CdS. A final Ar plasma etch was used to clean the CdS surface of any oxide creating the 300-nm windows shown in Figure 15 (b).

3.2.3 E-beam Lithography

A 200-nm-thick SiO_2 layer was deposited on the polished side of single crystal substrates at 200 °C using PECVD. The sample was then spun-coated with PMMA and ZEP for patterning. Feature sizes of 1 μm , 400 nm, 250 nm, and 136 nm were created on the resist. After patterning the resist, the pattern was transferred to the SiO_2 film using CHF_3 in a reactive ion etching system. SEM images of the resulting pattern in SiO_2 film are shown in Figure 15 (d). Four different feature sizes are distinguished and grouped under the same area. This mask design has the advantage of studying the microstructure of CdTe as a function of feature/island size. All islands are grown on the same substrate and exposed to the same deposition conditions at the same time.

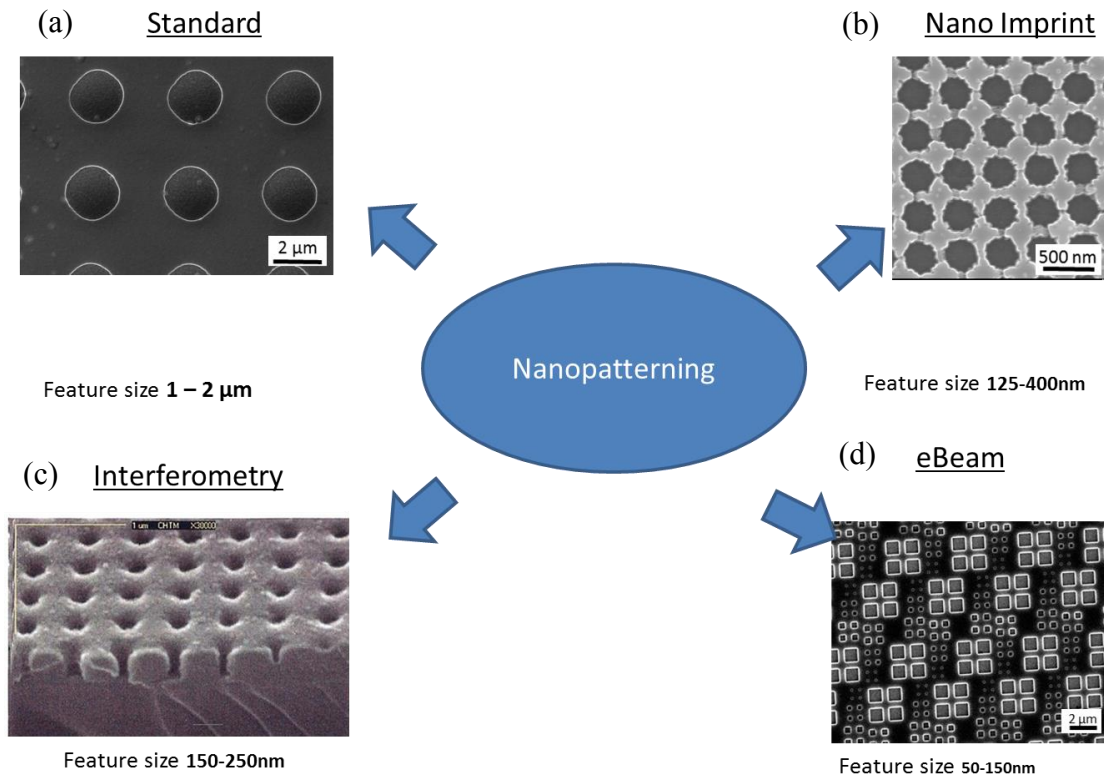


Figure 15 SEM picture of the SiO_2 patterned structures obtained with a) standard, b) nano imprint c) interferometry and electron beam lithography techniques

3.3 CdTe SELECTIVE AREA GROWTH

3.3.1 Intro to Deposition Technique

CdTe was deposited on patterned single-crystal CdS substrates using close space sublimation (CSS). CSS is a physical vapor deposition technique in which the source of the material and substrate are heated and separated 1.1 mm apart. The source-substrate difference in temperature drives the deposition and selectivity of the grown CdTe films [32, 33, 40]. Depositions are made under 1-10 Torr of helium pressure. A schematic of the CSS system used in this study is shown in Figure 16.

Growth selectivity is primarily governed by the relative difference in the sticking coefficients and surface adatom migration lengths of the reactant species on the masked and unmasked areas of a substrate. Moreover, the patterning scale relative to the migration lengths is

also an important parameter. In turn, these parameters depend on the source evaporation rate, adatom re-evaporation, substrate roughness, material properties of the masked and unmasked areas, and the concentration of the reactant species near the substrate surface. In CSS, the source evaporation rate is controlled predominantly by the source temperature, T_{so} . In contrast, the substrate temperature, T_{sub} , controls the adatom re-evaporation and surface migration length. CSS is used widely for the deposition of CdTe in photovoltaic applications and is characterized by the short distance between the source and the substrate (1–4 mm). Due to the short distance, the chamber pressure is also an important parameter that determines the growth mode [41].

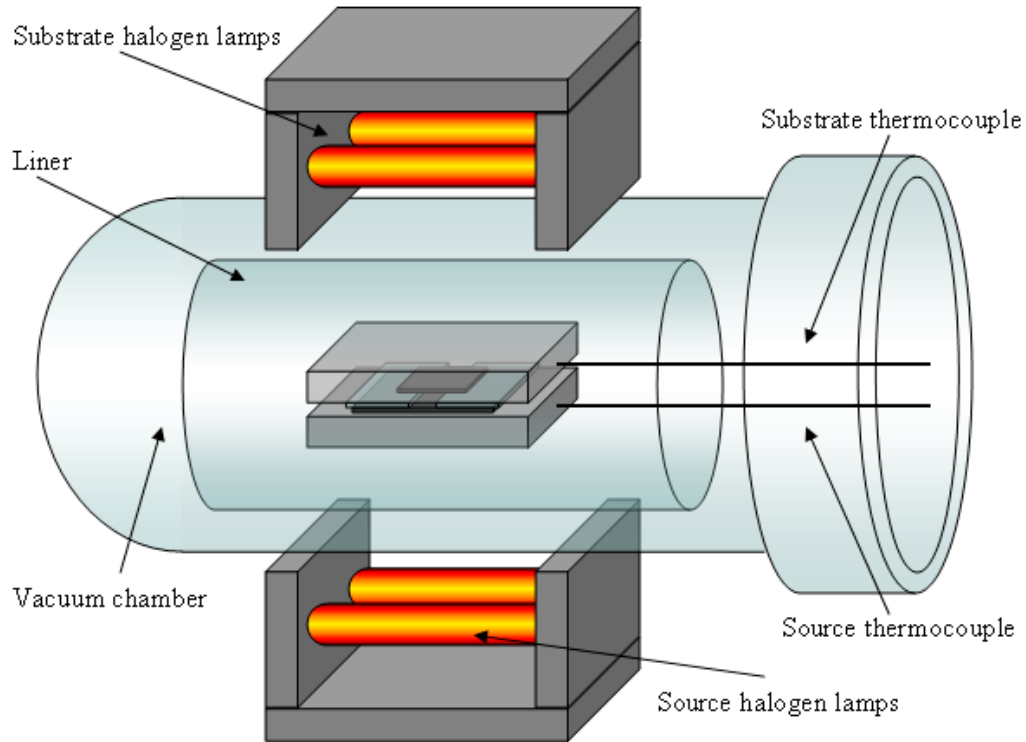


Figure 16 Schematic of the CSS apparatus used to deposit CdTe in this study. [42] The system consists of halogen lamps that increase the temperature of the source and substrate. Two graphite blocks are used to transfer the heat from the lamps to the source and the substrate. The source and the substrate are located inside a vacuum chamber.

3.3.1 Selective Area Growth Results

Growth selectivity can be either positive, zero, or negative. Consistent with previous works, positive selectivity is defined when the reactant species nucleates only on the unmasked material and not on the mask. Conversely, negative selectivity occurs when the species deposits only on the mask material. Finally, zero selectivity occurs when the reactant species nucleates on all areas of the substrate. In CSS, zero selectivity is readily achieved by setting T_{so} relatively high (and T_{sub} relatively low) to establish a high source evaporation rate.

The parameters that determine positive or negative selectivity are more intricate and generally enhance relative differences in the sticking coefficients and surface adatom migration lengths on the substrate. In this work, CdTe was selectively grown using a helium flow of 0.13 standard liters per minute (SLPM), a pressure of 5 Torr, and a source-substrate separation distance of 1.1 mm. The CSS depositor is similar to the one used recently to selectively grow InP on flexible substrates.[43] The CdTe source consisted of a 1" x 1" CdTe single crystal wafer without twins (1.5" x 1.5" x 1 mm, (111) oriented, twin free, double sided polished; Keystone Crystal Corp., USA). Twinning in CdTe sources produce poor spatial uniformity due to higher sublimation rates from regions with high-defect density. However, even without twins, the sublimation rate from each CdTe source was calibrated to account for variability from source to source. All sources started to sublime within the range of $T_{so} = 540$ to 570 °C. The substrate temperatures (T_{sub}) and deposition time are then adjusted to achieve selectivity in the micro- and nano-patterned substrates. In this work, the first step was to obtain selective area growth of CdTe on micropatterned substrates. The source temperature and deposition time then were reduced to control the CdTe grain size in the nano-patterned substrates by reducing the amount of material sublimated to the substrate. Table 1 summarizes the depositor and substrate conditions used in this study as well as the modulation in source temperature and deposition time for the nano-patterned substrates.

Table 1 Summary of deposition conditions to obtain positive and negative selectivity on Si and glass/ITO/CdS-patterned substrates.

Sample	Substrate type	Mask material	T_{so} (°C)	T_{sub} (°C)	$\Delta T = T_{so} - T_{sub}$	Deposition time (Sec)	Pattern scale	Selectivity
1	(100) Si	Si_3N_4	550	370	180	240	1 μm	Negative
2	pc-CdS	SiO_2	550	500	40	600	2 μm	Positive
3	pc-CdS	SiO_2	540	500	40	50	300 nm	Positive

Negative selectivity was observed when CdTe was deposited on a (100) silicon substrate patterned with a Si_3N_4 growth mask as shown in Figure 17. In this sample, the CdTe nucleated on the Si_3N_4 and not on the silicon, forming a connected square network of CdTe. No superfluous CdTe nucleation can be observed on the (100) silicon.

A comparison of the microstructure for CdTe grown on micro-patterned versus nano-patterned substrates is presented in Figure 6. For both cases, positive selectivity was achieved in large areas as shown in Figure 18 (a)-(d) without nucleation on the SiO_2 mask when using CdS-coated substrates.

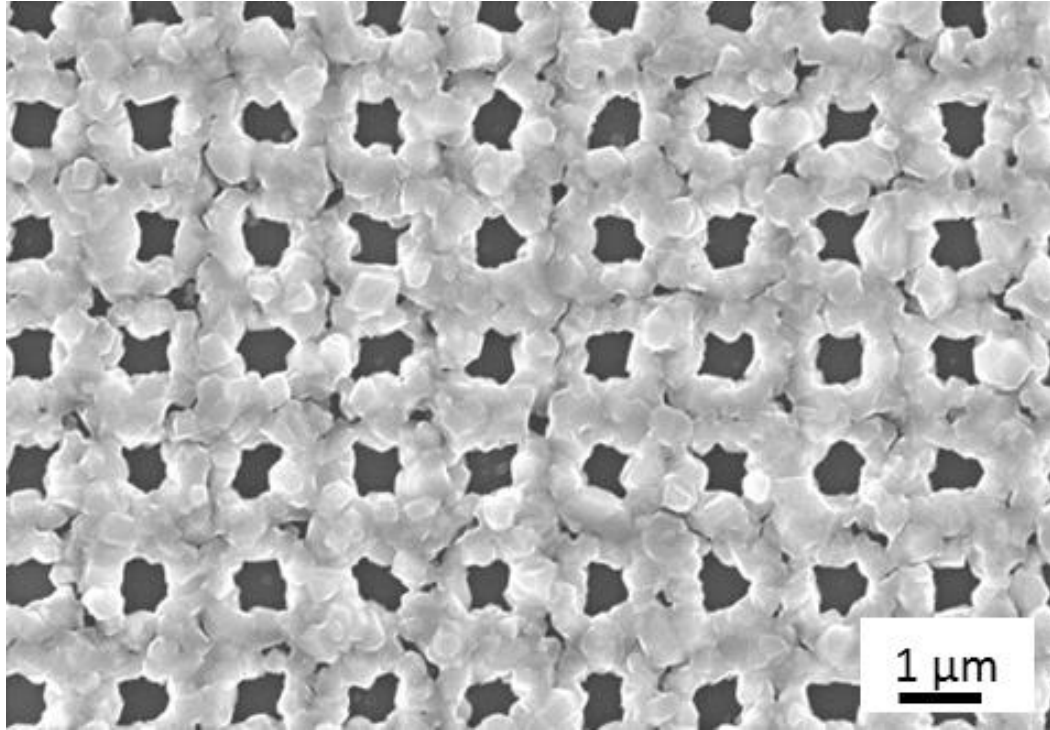


Figure 17 Negative SAG of CdTe on (100) silicon patterned with a Si_3N_4 growth mask.

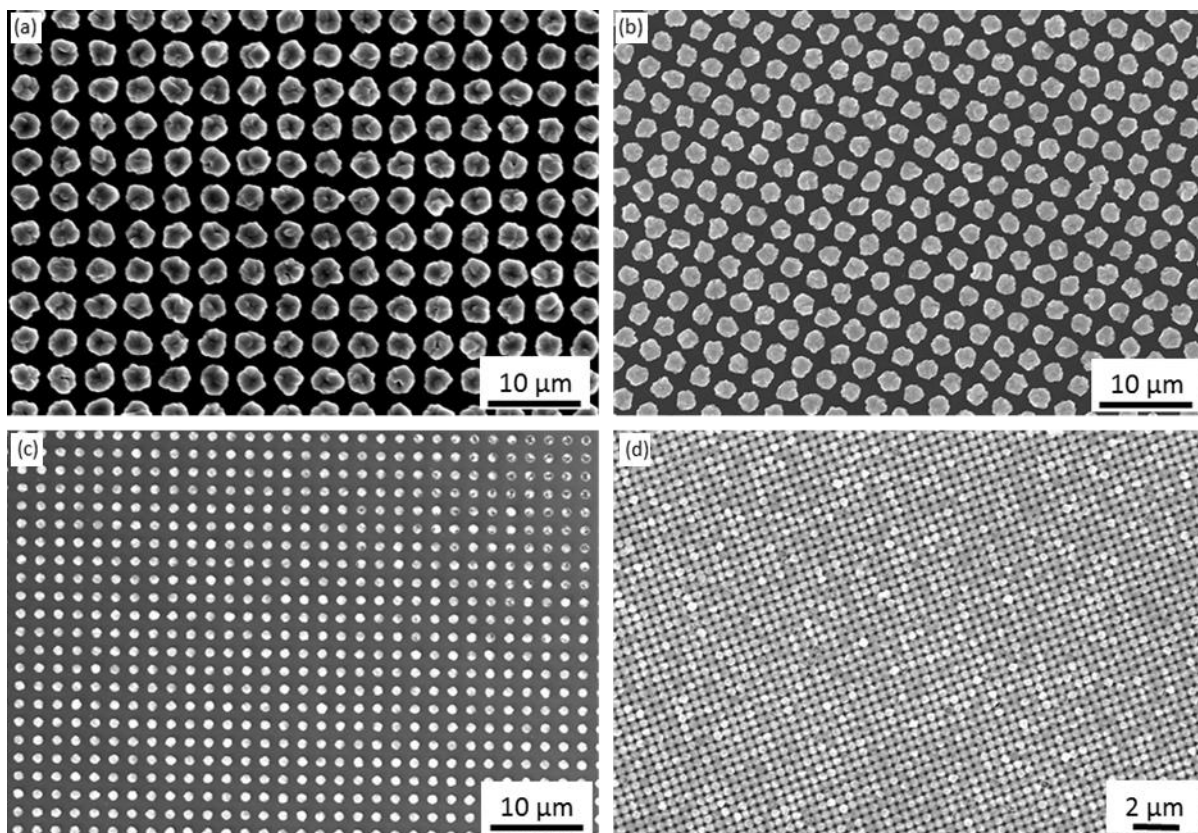


Figure 18 SAG of CdTe on glass/ITO/CdS patterned substrates with feature sizes of (a) 2 μm, (b) 1 μm, (c) 1.5 μm, and (d) 300 nm.

Chapter 4: Specimen Preparation via Focused Ion Beam

Focused ion beam (FIB) milling was used to prepare samples as required for SEM, EBSD, Conducting AFM and TEM characterization. Moreover, FIB marks were used to identify regions on the sample and locate cells to facilitate one-to-one comparison of the various characterization data of individual cells. In some cases, FIB was also used to electrically isolate solar cells. Finally, FIB was used to etch-back and deposit electrical contacts to individual solar cells.

4.1 MICRO AND NANO-MARKS FOR ISLAND INDEXING AND IDENTIFICATION

A strategy was developed to identify areas of interest and to index individual islands within a sample. Basically large (course) marks were created using the FIB to identify regions of interest. Smaller (fine) marks were created to help locate individual sets of islands in the nanoscale samples. Figure 19 for (a) and (b) show a sample with micrometer sized CdTe islands and the corresponding FIB marks. Similarly, Figure 19 (c) and (d) show a sample with nanometer sized CdTe islands and the corresponding FIB marks. Square and triangular marks were made on the micropatterned samples. The triangular marks served as direction pointers to help locate region more easily.

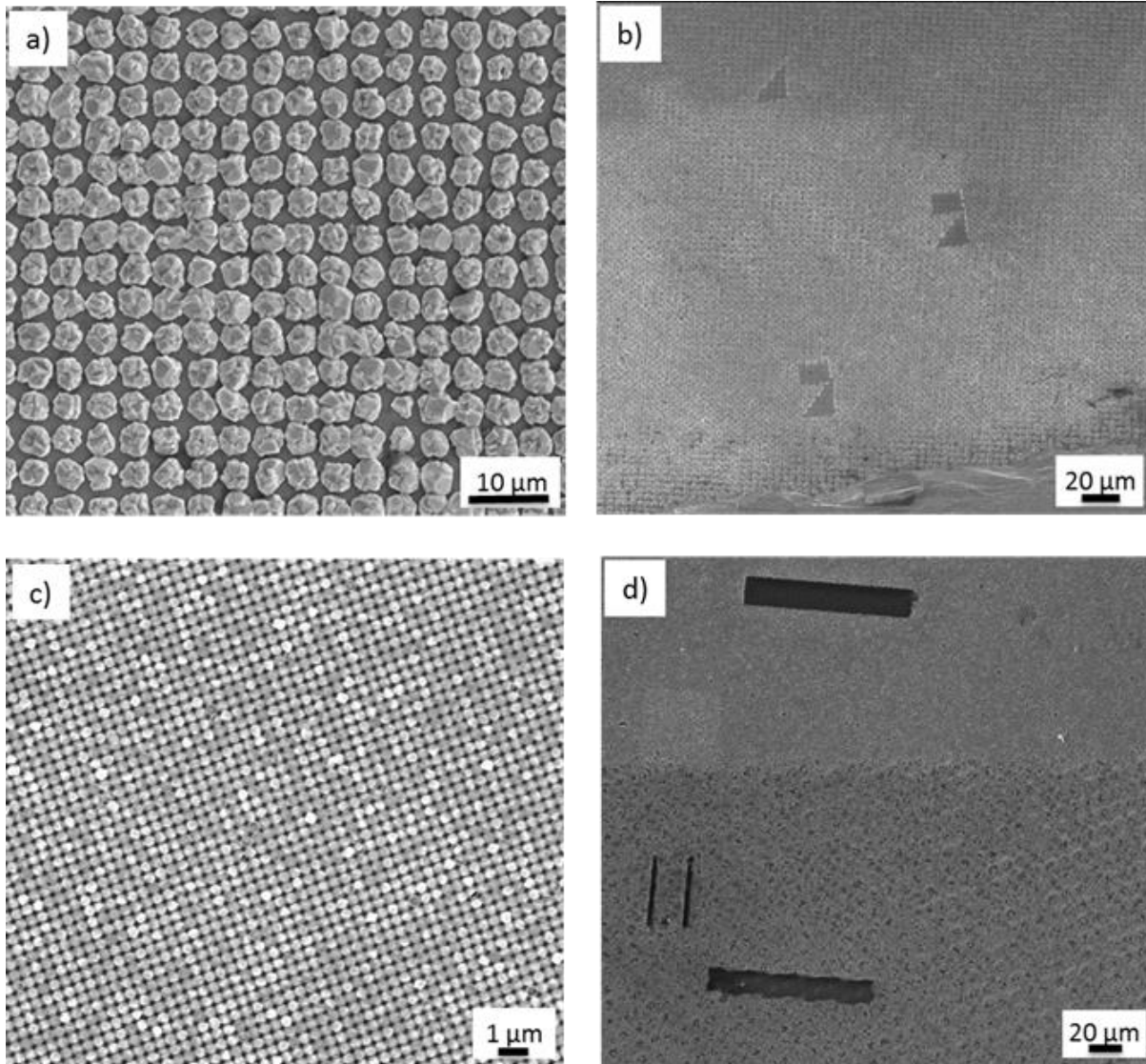


Figure 19 SEM plan view images of (a) an area with CdTe microislands, (b) an area with CdTe nano-islands, (c) micromarks used to identify and index CdTe microislands and (d) an area with micro and nano-marks to identify and index CdTe nano-islands.

4.2 ISLAND PREPARATION FOR EBSD STUDIES

Since EBSD requires a smooth surface, the surfaces of CdTe islands needed to be smoothed before data could be collected. CdTe micro and nano islands usually grow with non-flat surfaces. A flat surface is required in order to detect scattered electrons that provide information on the grain orientations of the material. The surfaces of CdTe micro and nano-islands were shaved (planarized) using a focus ion beam parallel to the surface. Figure 20 shows

the CdTe islands (a) before and (b) after the planarization process. . Figure 20 (c) shows a low-magnification SEM image of a planarized region between the FIB marks.

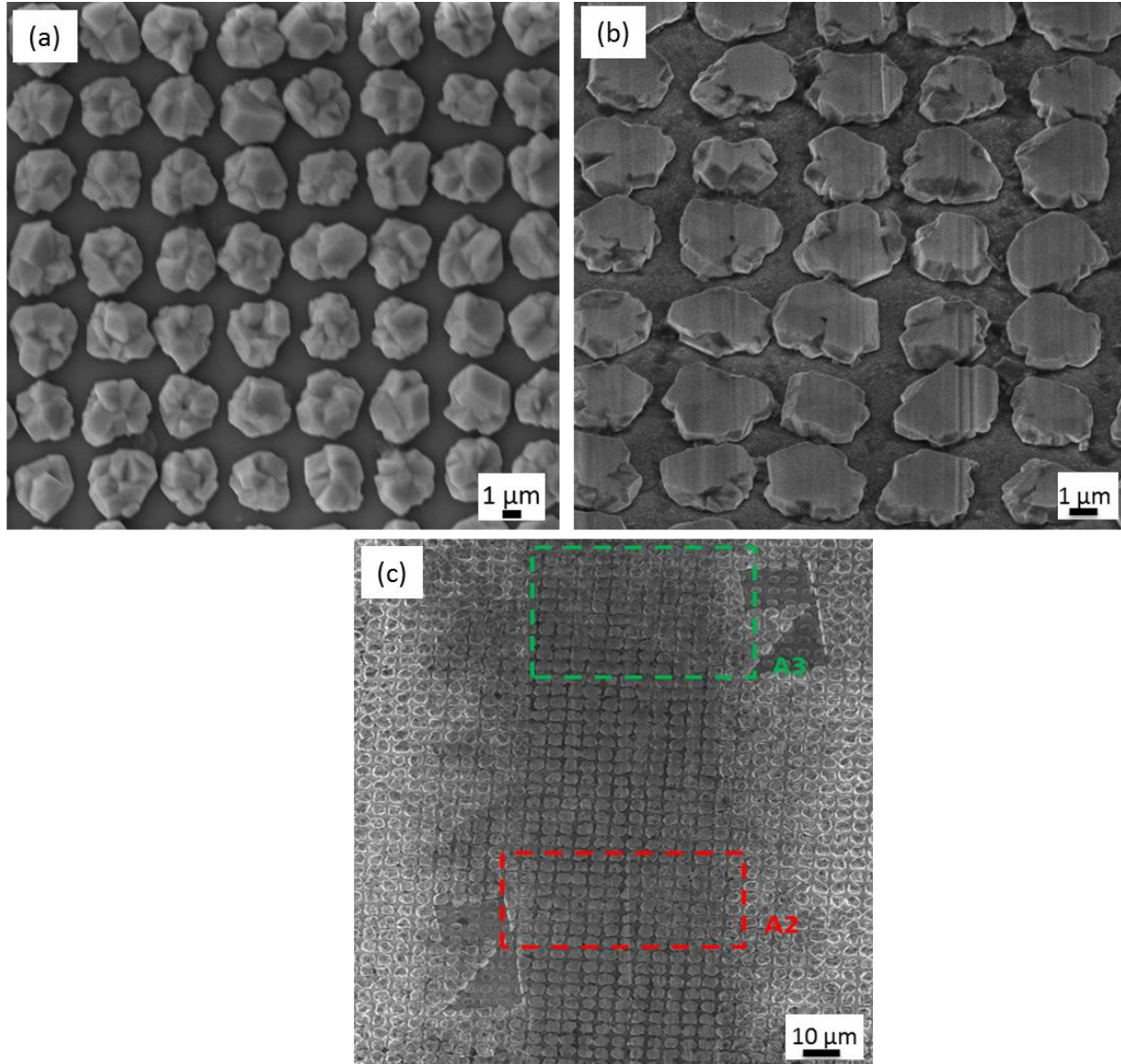


Figure 20 shows SEM (a) plan view of CdTe microislands before planarization and (b) perspective view of CdTe microislands after planarization. (c) Shows two areas of interest where EBSD data was taken from.

4.3 FOIL PREPARATION FOR TEM

The in-situ lift-out process was used to prepare specimens for cross-sectional TEM [44]. Samples were mounted on a sample holder and inserted into a dual-beam SEM/FIB system. The surface of the samples was placed perpendicular to the gallium ion beam and at 52° from the

electron beam. First, a small amount of platinum was deposited on top of a region of interest to protect the CdTe islands as it is shown in Figure 21. Platinum was deposited by decomposing Methylcyclopentadienyl (Trimethyl) platinum with the gallium ion beam. Then, two staircase-shaped trenches were milled on the sides of the platinum deposition as shown in Figure 22 (a). Fine milling was then made close to the region of interest to thin the specimen. A “U-cut” was made on the specimen to detach it from the bottom and the sides of the substrate as shown in Figure 25 (b). Specimens were removed from the substrate using an omniprobe (Figure 25 (d)) and thinned to 120 nm using the gallium ion beam for electron transparency (Figure 25 (e)-(f)). Samples were finally mounted on a carbon/copper and pure copper grids for TEM analysis.

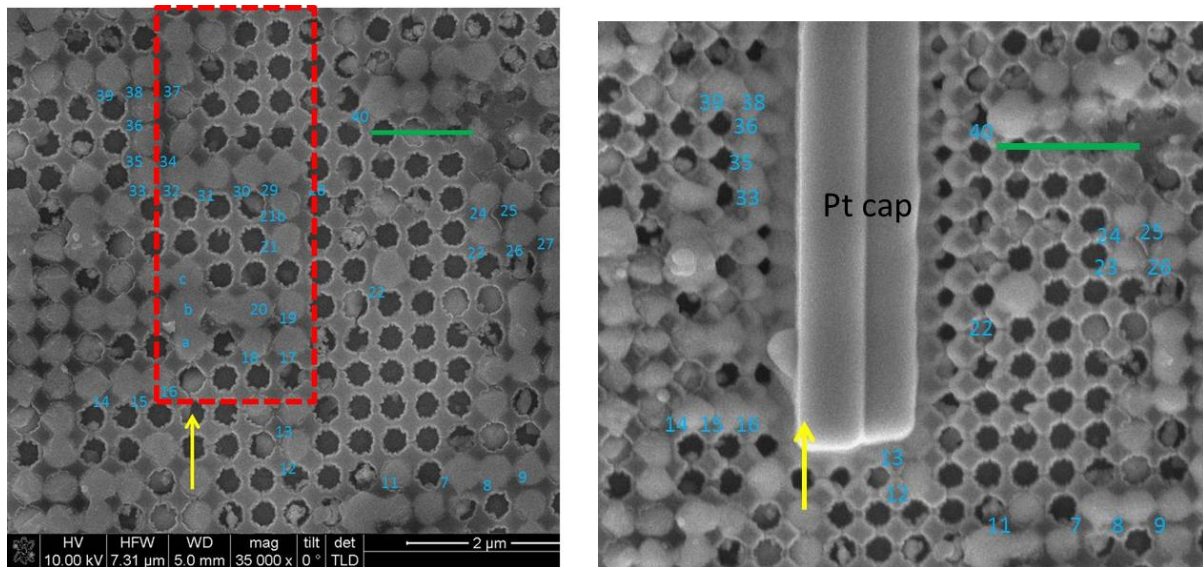


Figure 21 Shows SEM plan view of (a) an area of interest delineated by a red dashed rectangle and (b) the same area of interest covered with a platinum protective cap

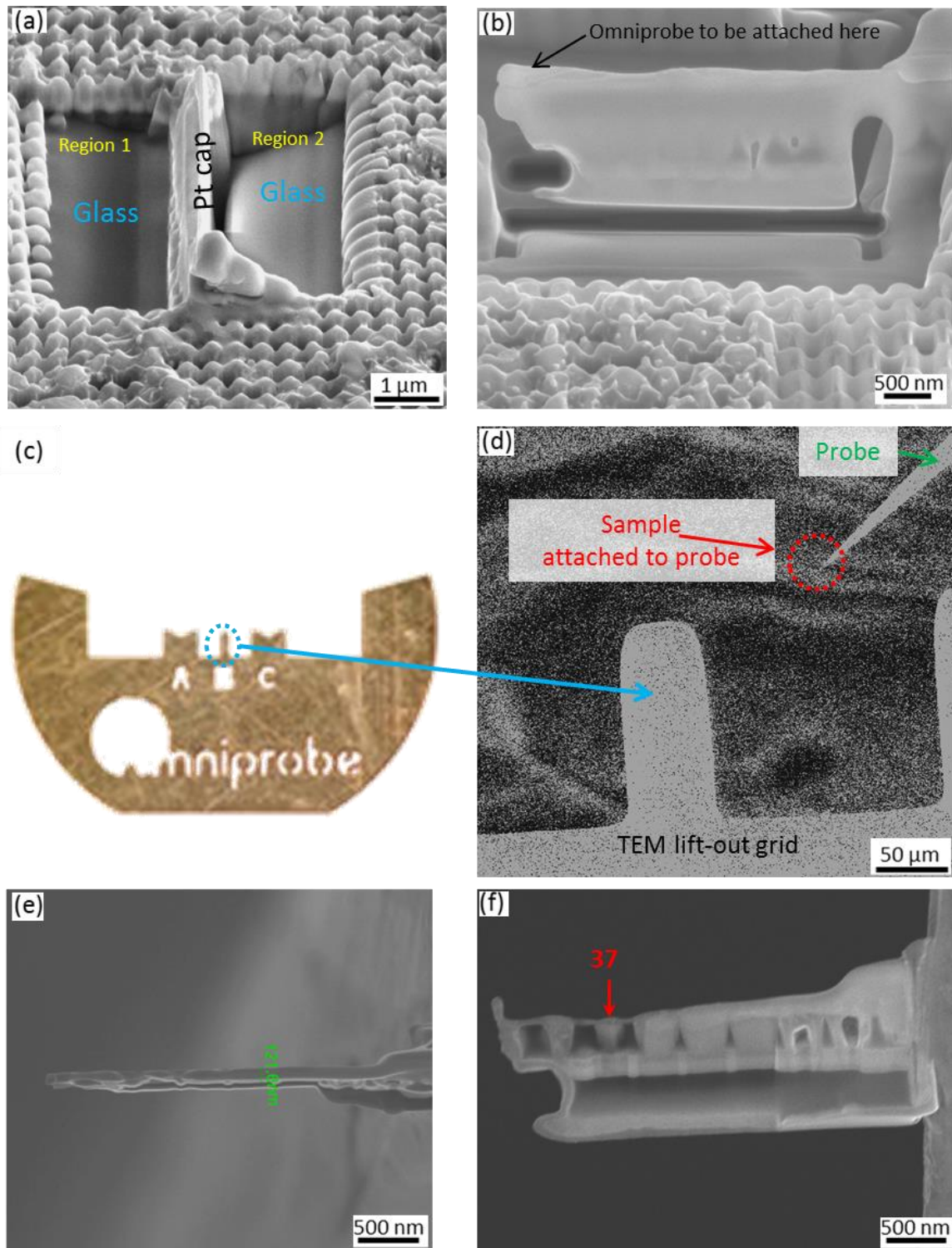


Figure 22 Shows the TEM lamella preparation process. (a) Shows two stair-shaped trenches made on the sides of the area of interest, (b) shows the “u” cut made on the bottom of the lamella. (c) Shows the TEM cooper grid used to mount the sample inside the TEM. (d) Shows the lamella attached to an omniprobe used to transfer the sample to the center pillar of the TEM grid. (e) Shows the plan view of the TEM lamella with a thickness of about 120 nm. (f) Shows the cross-sectional view of the TEM lamella mounted on the cooper grid after the final thinning.

Chapter 5: Microstructure Characterization-SEM and EBSD

5.1 SURFACE ANALYSIS

A comparison of the microstructure for CdTe grown on micro-patterned versus nano-patterned substrates is presented in Figure 23. For both cases, positive selectivity was achieved in large areas as shown in Figure 23 (a) and (b) without nucleation on the SiO₂ mask when using CdS-coated substrates. Figure 23 (c) and (e) of CdTe grown on the 2- μ m patterned substrate show that the CdTe islands are composed of several grains as indicated by the dark contrast along grain boundaries. Moreover, the size of each CdTe crystal grain is $\sim 1\ \mu\text{m}$, in agreement with previous reports [33]. In comparison, Figure 23 (d) and (f) show that in several cases the CdTe deposited on the 300-nm patterned substrate appear to be single-crystal as indicated by lack of contrast. (The cross-sectional samples were created using a gallium focused ion beam (FIB) to reduce contrast due to morphology.) It should be noted, however, that some islands do appear to have multiple crystal grains as indicated by the arrows in Figure 23 (d).[45]

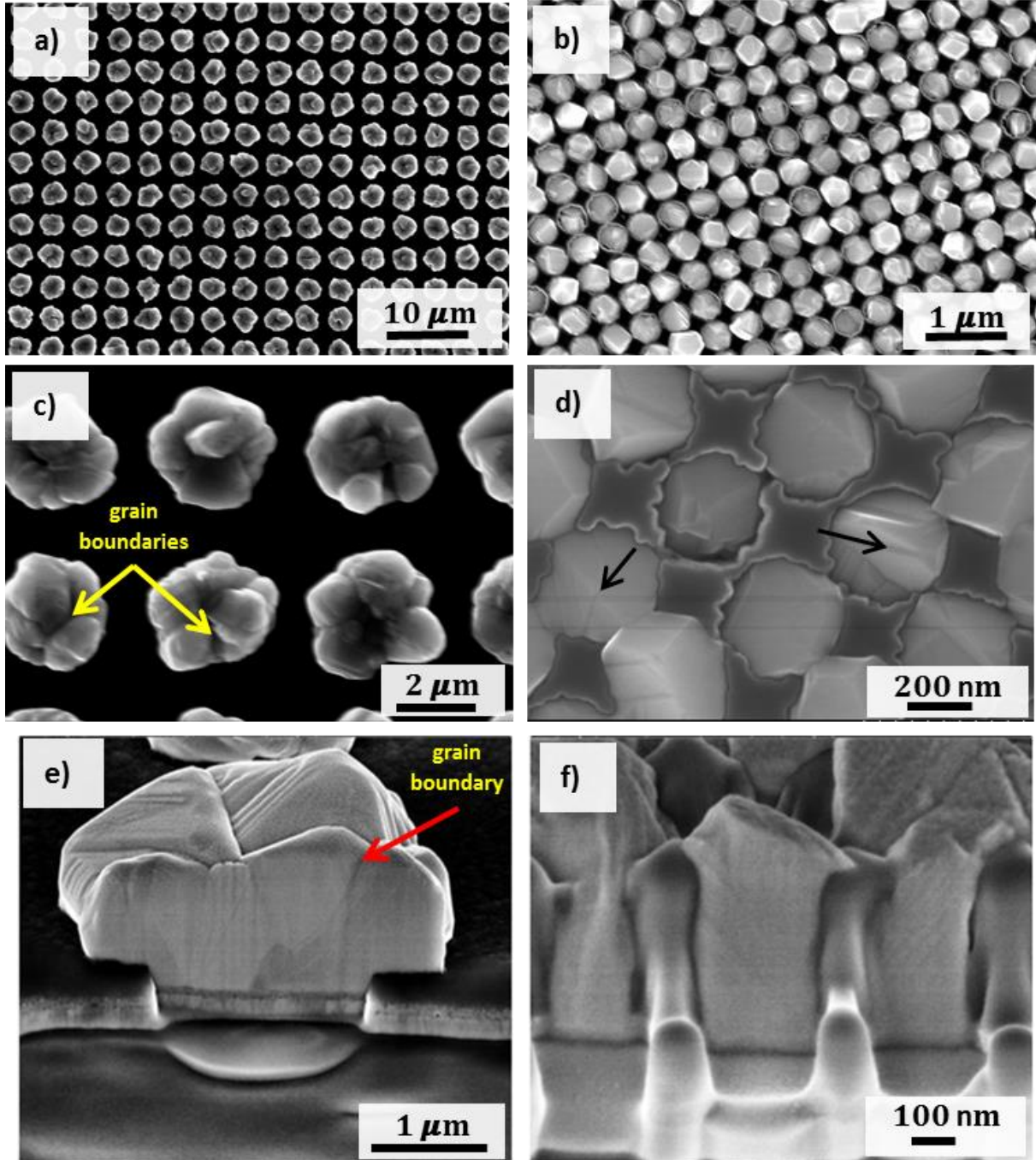


Figure 23 Micro-structures of CdTe deposited in window sizes of 2 μm and 300 nm at temperatures $T_{\text{so}} = 550^\circ\text{C}$ and $T_{\text{sub}} = 500^\circ\text{C}$. Low (a, b) and high (c, d) [45] magnification planar SEM images of selectively grown CdTe islands on micro- and nano-patterned substrates. Cross-sectional SEM images of selectively grown CdTe islands on micro- (e) and nano-patterned (f) substrates.

Electron backscatter diffraction (EBSD) was performed to further study the effect of patterning size on crystal nucleation and orientation. EBSD uses color contrast to indicate the

orientation of crystals. To prepare the samples, FIB was used to planarize the surface as explained in the last chapter. Figure 24 shows band-contrast and EBSD images of non-patterned, micropatterned, and nanopatterned samples. The band-contrast and EBSD images are from the same region of each sample type to facilitate direct comparison. The inset in Figure 24 (b) shows the color orientation map. The color in the map represents the CdTe orientation. EBSD of CdTe deposited on the non-patterned substrate shows typical polycrystalline growth with random grain morphology and crystal orientation as shown in Figure 24 (b). The number of grains per window was determined by counting the number of colors per window in the EBSD map. Table 2 shows a summary of the number of grains per island and the grain-orientation distribution in the micro and nano-patterned substrates. EBSD of CdTe deposited on the micro-patterned substrate shows that each island contains ~3–10 grains with an average of 5.4 grains per island (Figure 24 (d)). No islands are observed containing a single grain, consistent with Band contrast. Conversely, CdTe growth on the nano-patterned substrate showed that most of the islands were composed of a single crystal grain, as shown in Figure 24 (f), with an average of 1.8 grains per nano-window. There were only six nano-islands containing three to five grains. From the orientations analyzed with EBSD, the (101) orientation occurred most often for both the micro and nano-patterned samples compared to the (001) and (111) orientations. Although the CdS is nanocrystalline with average grain size of 50 nm, as shown in Figure 13, it is well known that CdTe grains can nucleate grains much larger than the grains of the underlying CdS during planar growth. Indeed, our initial experiments with microscopic patterning attempted to exploit this phenomenon. However, due to the relative smaller latitude in processing (usually lower temperature) needed to achieve the desired positive selectivity, the grain size of the selectively- grown grains is smaller compared to planar growth. Nevertheless, it is reasonable to expect that nucleation of single-crystal grains of CdTe with diameter of 300 nm can occur in the nanopatterned substrate, although the CdS has a grain size of 50 nm.

Table 2 Grains per island and percentage of grains grown in the (101), (001), and (111) orientations for the micro- and nano-patterned samples.

	Grains per island			CdTe crystal orientation			
Window size	Minimum	Maximum	Average	-101	-1	-111	Other
Micro (2um)	3	10	5.4	11.85%	3.73%	4.22%	80.20%
Nano (300nm)	1	5	1.8	18.18%	7.07%	5.05%	69.70%

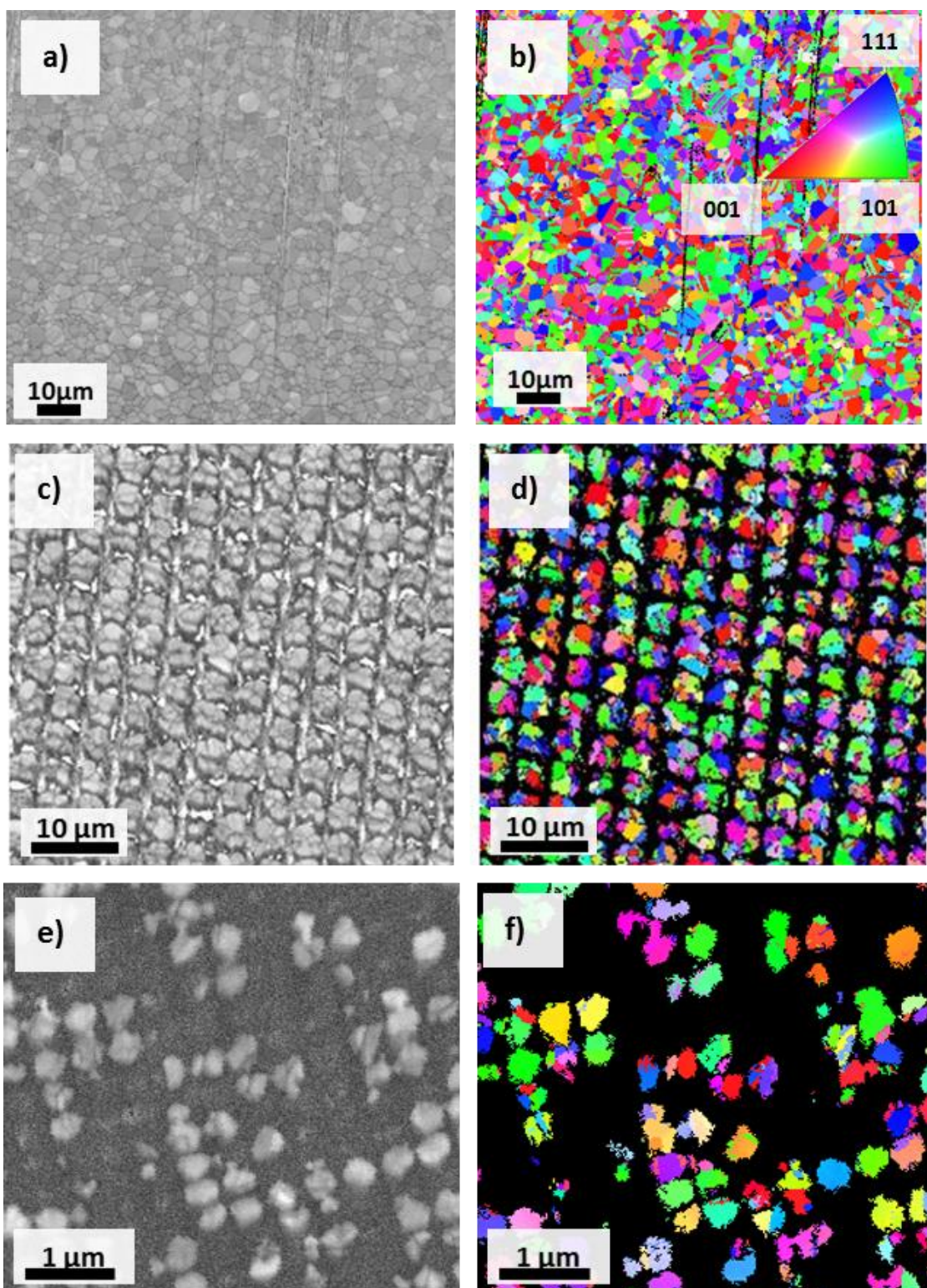


Figure 24 SEM and EBSD plan view images of CdTe deposited on (a, b) planar, (c, d) micro-patterned, and (e, f) nano-patterned CdS substrates.

5.2 CROSS-SECTION ANALYSIS

Selective growth of CdTe was also studied on single crystal CdS. A SiO₂ mask with different window sizes as the one shown in section 3 was used. CdTe was grown selectively at the beginning, and the deposition continued to overgrow CdTe. A FIB system was used to make a trench in the sample and to look at the cross-sectional view of the CdS/CdTe interface. SEM revealed that several CdTe grains nucleated in the micro-sized windows, whereas single grains nucleated in the 136-nm windows, as shown in Figure 25. Figure 25 compares the CdTe grown inside a 1- μ m SiO₂ window with CdTe grown inside a 136-nm window. Variation in contrast inside the 1- μ m window indicates multiple CdTe and grain boundaries were found in this case. In Figure 25 (b), there is no contrast variation observed inside the 136-nm island. Another observation is that CdTe continued growing with a multigrain structure over the 1- μ m island. In the nanowindow case, the single CdTe grain that nucleated inside the 136-nm island acts as a high-quality seed that continues to grow into high-quality material. The streak that extends from the top to bottom in Figure 25 (b) is a byproduct of the sample FIB milling process. A more detailed study was performed to examine the effect of the SiO₂ window size on the atomic defects and CdS/CdTe interface. The results are presented in the next section.

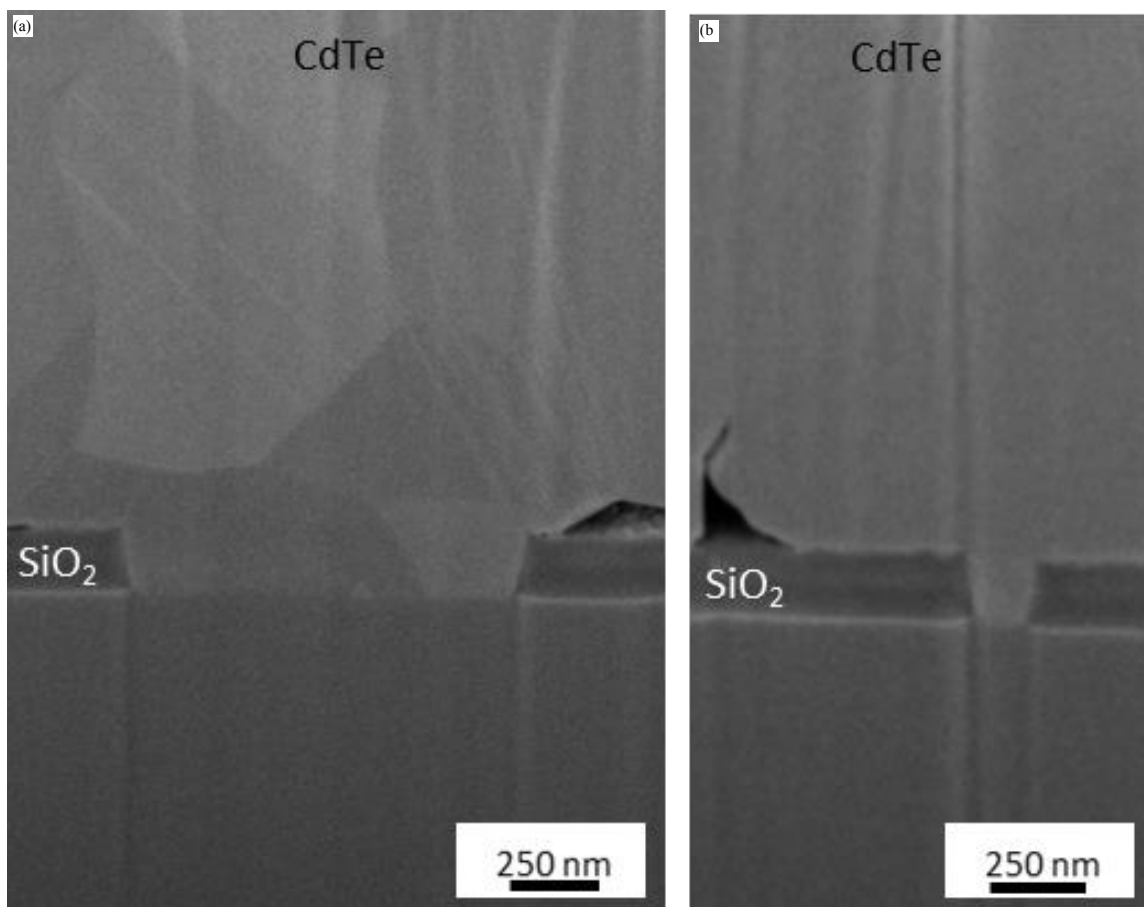


Figure 25 SEM cross-sectional view of the CdS/CdTe interface for two SiO₂ window sizes (a) 1 μm and (b) 136 nm.

Chapter 6: Microstructure Characterization-TEM

6.1 CROSS-SECTION ANALYSIS

Cross-sectional TEM characterization was performed to study the crystal growth habit and defect microstructure in CdTe islands selectively-grown on a single crystal (0001) CdS substrate. In order to understand the effect of patterning size on the defect density, low and high magnification images were taken of a set of islands with diameter of 1 μm , 250 nm, and 136 nm. Figure 26 shows low-magnification TEM images of the (a) 1- μm , (b) 250-nm and (c) 136-nm CdTe islands. TEM images of the 1- μm island were taken with a FEI Tecnai G (2) F30 S-Twin 300 kV TEM equipped with a field emission gun and a resolution of 0.2 nm. The TEM images of the 250-nm and 136-nm islands were taken with a FEI Titan G2 80-200 that has ChemiSTEM technology on an aberration-corrected scanning/transmission electron microscope (AC-STEM) [46].

Image contrast is an indicator of defects in a material due to electron beam scattering by the defects. In the selectively grown CdTe samples it was observed that image contrast varied according to island size as shown in Figure 26. The 1- μm island has the highest degree of contrast whereas the 136-nm island has the least amount. This suggests that the defect density was reduced concomitant with a reduction in island diameter in qualitative agreement with the theory of nanoheteroepitaxy.

Another interesting observation is that the 1- μm and 250-nm islands have surfaces that are inclined with respect to the CdTe/CdS interface indicating that growth on these islands occurred at an angle. On the other hand, the 136-nm island displayed a surface parallel to the interface indicating growth occurring normal to the interface. These three islands were further analyzed using high-resolution TEM and their corresponding fast-Fourier transforms (FFT) as described below.

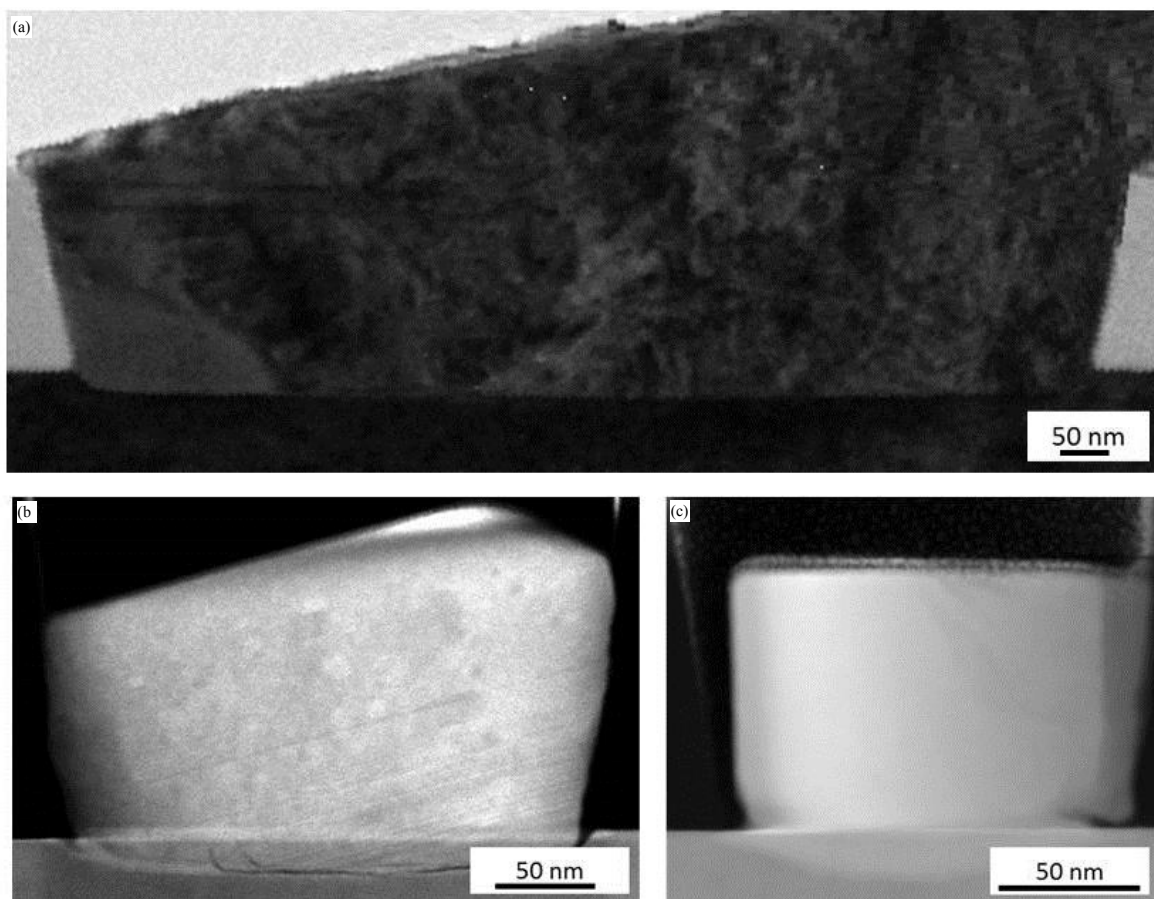


Figure 26 TEM low-magnification images of CdTe islands grown in three window sizes: a) 1 μm , b) 250 nm and c) 136 nm.

6.2 HIGH-RESOLUTION INTERFACE ANALYSIS

High-magnification TEM imaging at the interfaces of the 1- μm , 250 nm, and 136-nm CdS/CdTe islands was performed to study the crystal habit and defect structure. In general the findings were consistent with the low-magnification images in that a reduction in defect density was observed as the island size decreased. Figure 27 shows the lattice images of the three islands and corresponding FFTs.

The two-dimensional FFTs were created using Gatan's DigitalMicrographTM (Version 2.31.734.0). Since the three CdTe islands were grown on the same single crystal (0001)CdS substrate, it is reasonable to expect that the diffraction spots associated with the CdS layer will be similar if not identical for each island. Indeed the sets of spots labeled by yellow arrows in Figure 27 indicate an identically (0001) orientated wurtzite CdS for each island. The sets of spots

labeled by the red arrows correspond to the selectively grown CdTe. Unlike the CdS, each CdTe island is oriented differently as observed in the TEM lattice images and corresponding FFTs. Moreover, the crystal structure of the 136-nm CdTe island is wurtzite whereas the 250-nm and 1- μm islands are zincblende. Finally, since the lattice constant of CdTe is bigger than CdS, the CdTe spots are located closer to the center than the corresponding spots from CdS.

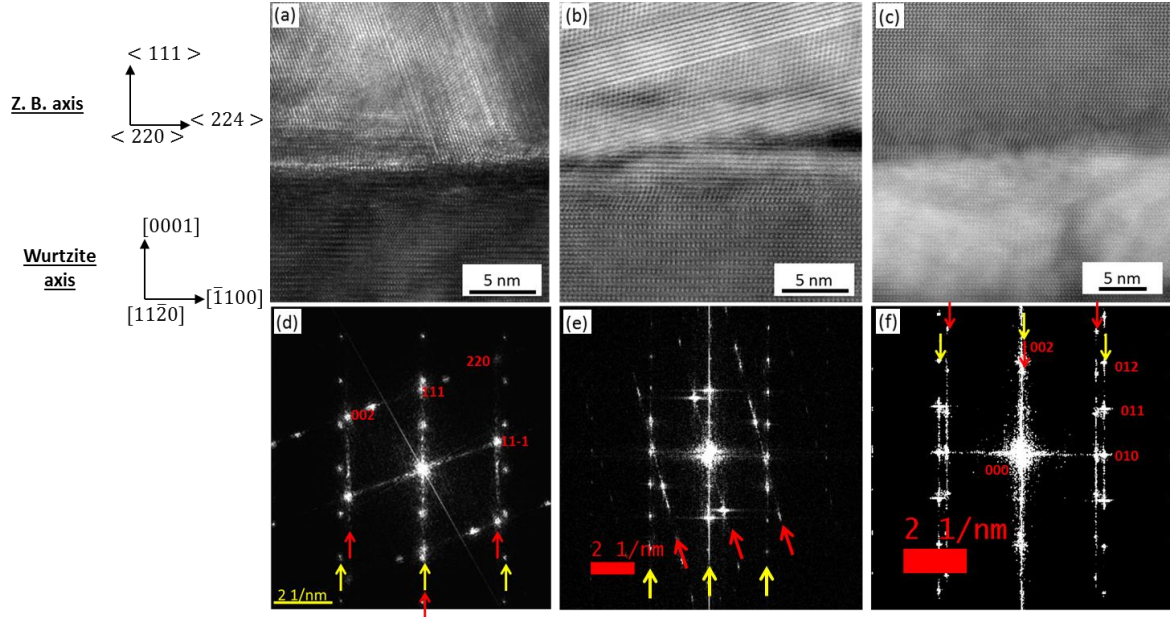


Figure 27 High-magnification TEM images of the CdS/CdTe cross-sectional view of three island sizes (a) 1 μm , (b) 250 nm and (c) 136 nm, and their corresponding FFTs, (d) 1 μm , (e) 250 nm and (f) 136 nm.

Defect-free images of zincblende and wurtzite CdTe crystals were simulated using molecular dynamics [47]. These structures provided a detailed view of the atom stacking in each crystal configuration. Since the simulated crystals can be rotated in any direction, they were used to analyze the TEM images of the experimental growth. Figure 28 (a) shows a cross-sectional view of a simulated perfect zincblende crystal. The crystal was made intentionally perfect to visualize the stacking of atomic planes. From Figure 28, it is observed that Cd atoms (in blue) and Te atoms (in red) follow the AaBbCc stacking sequence of a zincblende crystal structure. Also, the close-packed planes (Aa, Bb or Cc) and the atomic “dumbbells” can be observed in this simulated structure.

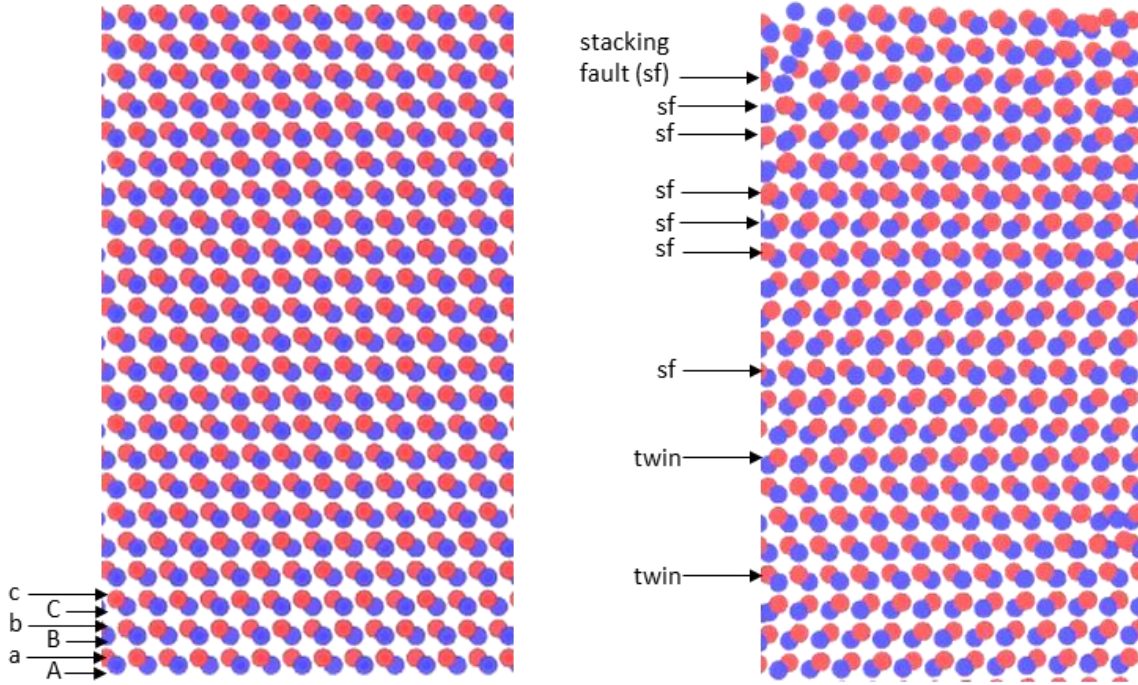


Figure 28 Shows (a) a perfect simulated CdTe ZB structure and (b) a simulated growth of CdTe on a planar CdS fixed substrate

A simulation of a CdTe deposited on planar CdS using periodic boundary conditions was also used to understand the experimental growth. Figure 28 (b) shows the cross-sectional view of a simulated growth of CdTe on a planar substrate. From Figure 28 (b), there are two types of defects that are identified with black arrows: twin boundaries and stacking faults. These simulations helped identify defects in the experimental growth.

From the perfect zincblende and wurtzite crystals that were simulated, a structure guide was made to follow the stacking sequence and detect stacking faults in the experimental growth. The structure guides are shown in Figure 29. The structure guides were superimposed in each TEM image and the findings for each island are discussed in the sub-sections below.

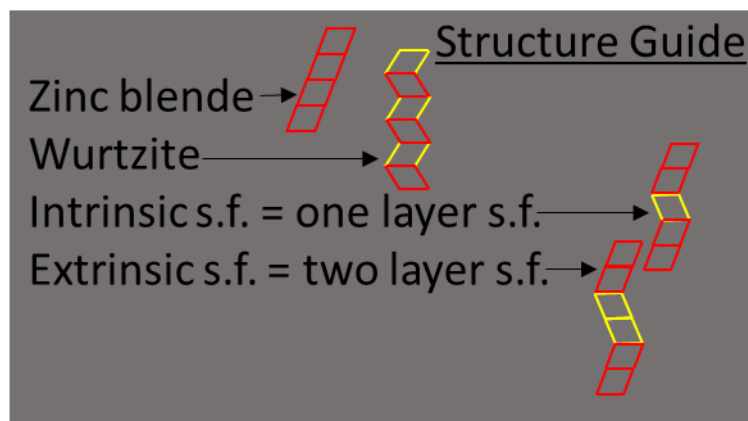


Figure 29 Structure guide used to analyze the stacking sequence and defects in the experimental growth.

Detailed analysis of the lattice images and FFTs was performed to understand the growth habit and calculate the residual strain in each of the islands. In order to calculate the lattice mismatch and therefore residual strain in the CdTe/CdS structures it is important to analyze the detailed atomic alignment at the hetero-interface. For the case of the 136-nm island (Figure 27 (f)), the analysis and calculation is straight forward since the CdS and CdTe are both wurtzite and oriented with the basal plan parallel to the hetero-interface. However the 250-nm (Figure 27 (e)) and 1- μm (Figure 27 (d)) required more analysis since the CdTe is zincblende and the CdS is wurtzite. Moreover, the (111) plane of 250-nm CdTe island is rotated $\sim 15^\circ$ relative to the interface whereas the (111) plane of 1- μm island is aligned with the hetero-interface.

To facilitate analysis of the atomic alignment at the interface, a three-dimensional (3D) schematic of the zincblende structure is shown in Figure 30. The triangle formed by the blue lines in Figure 30 (a) corresponds to the (111) plane. The letter “a” in Figure 30 (b) refers to the lattice constant, and “h” to the hypotenuse of the triangle made by sides “a” on the base of the cube.

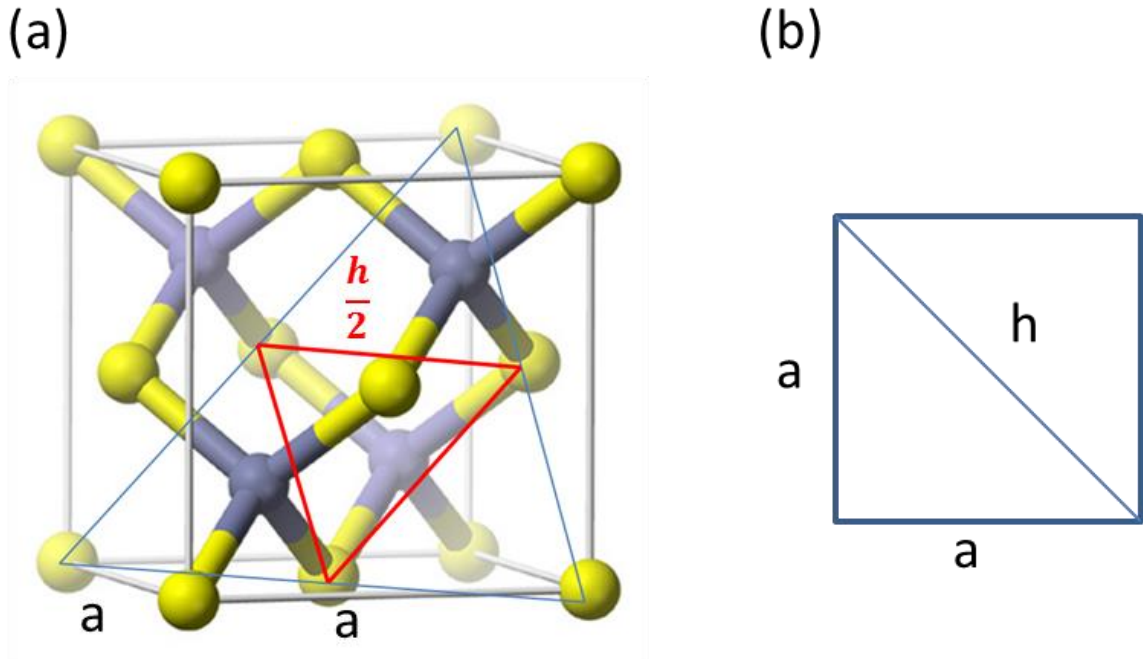


Figure 30 Shows the (a) 3D schematic of a zincblende structure and (b) the base of the cube in (a) [48]

CdS substrates used in this work have the wurtzite (WZ) configuration. A 3D schematic of a wurtzite structure is shown in Figure 31 (a), and its (0001) plane is shown in Figure 31 (b). Notice that the base of the wurtzite structure is a hexagon formed by three rhomboids. Figure 31 (b) shows one of the rhomboids in red and two of the rhomboids in dashed blue lines. When ZB CdTe grows on a WZ CdS substrate, the biggest triangle made with blue lines in Figure 30 (a) faces the (0001) surface shown in Figure 31 (b). Figure 32 shows the triangle in Figure 30 (a) superimposed by dashed lines in the (0001) plane. Notice that $h/2$ in Figure 30 (a) is equivalent to the lattice constant “a” in the hexagonal structure.

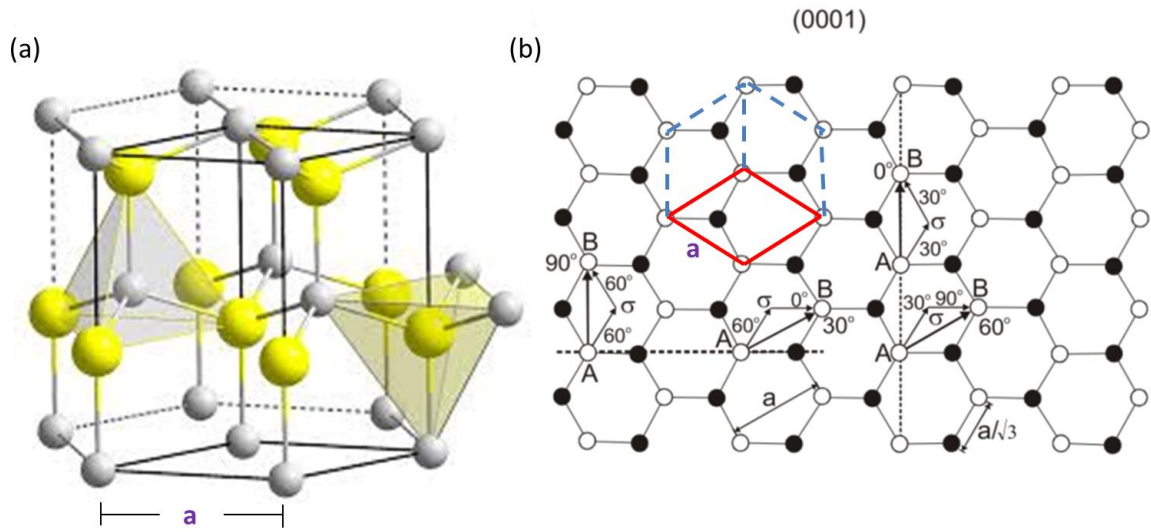


Figure 31 Shows (a) a 3D schematic of a hexagonal unit cell and (b) the view of the (0001) plane in a hexagonal structure [49, 50].

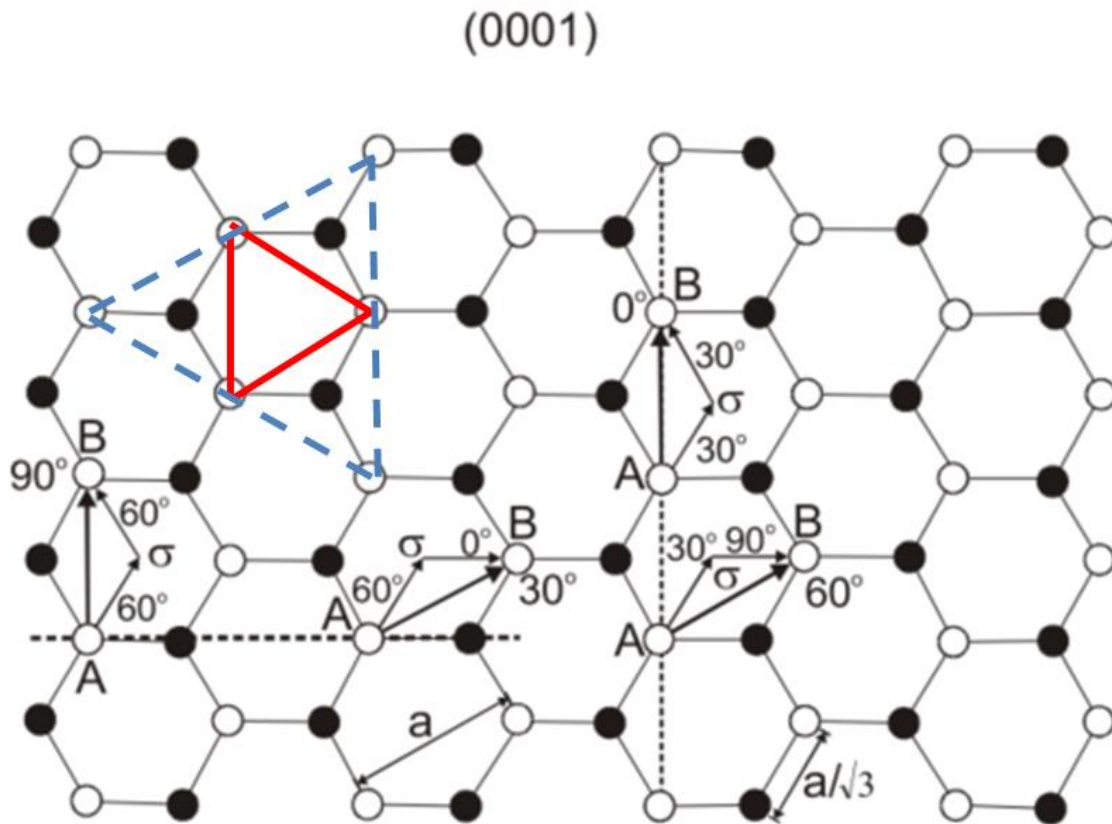


Figure 32 Shows the triangle (111) plane of a ZB structure superimposed on a (0001) plane of a WZ structure [50].

6.2.1 Detailed Analysis of the 1- μm Island

The high-resolution cross-sectional TEM image of the 1- μm island was studied with the structure guides shown in Figure 29. The atomic stacking of the CdS substrate matched the wurtzite atomic stacking when the structure guide was superimposed in Figure 33. The atomic stacking of the CdTe island matched the ZB configuration when the structure guides were superimposed in the high-resolution TEM image. Intrinsic stacking faults were observed close to the interface as indicated by the yellow rectangles of the structure guides on the CdTe side of Figure 33 [51].

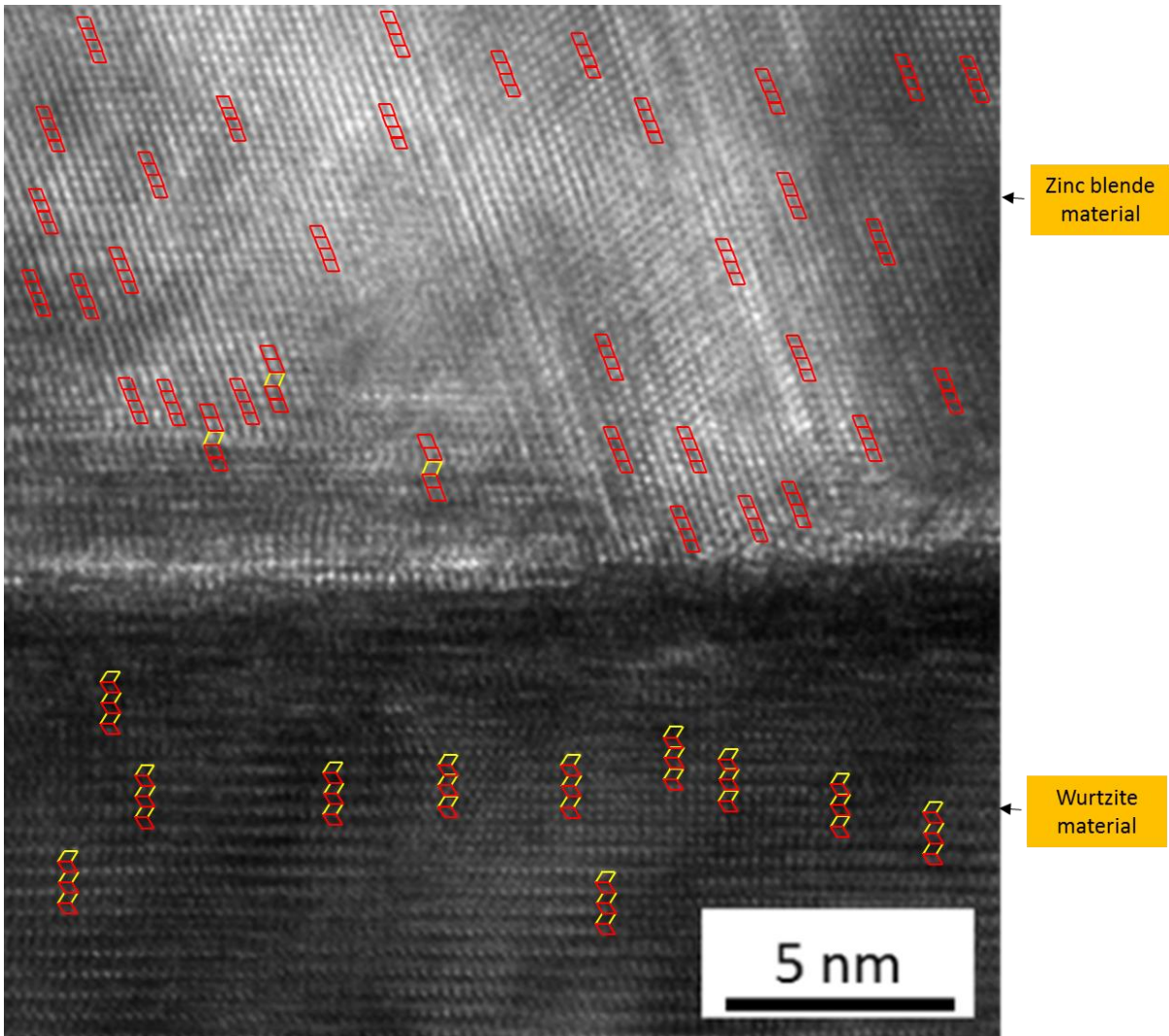


Figure 33 Structure guides superimposed in TEM images to determine the atomic stacking and stacking fault types in the 1- μm -sized CdTe island [51].

To calculate the CdS/CdTe lattice mismatch in the 1- μm island, isotropic stresses were assumed and the CdTe lattice constant “a” was extracted from the d-spacing formula given by

$$\text{Equation 5} \quad d_{hkl} = \frac{a}{\sqrt{h^2 + k^2 + l^2}}$$

where $d_{hkl} = d_{002} = 3.27 \text{ \AA}$. The value of d_{002} was obtained by measuring the d-spacing of the (002) reflection in Figure 27 (d). Since $h/2$ in Figure 30 (a) is equivalent to the lattice constant “a” in the hexagonal structure, “h” was calculated using

$$\text{Equation 6} \quad h^2 = \sqrt{a^2 + a^2}$$

where a = lattice constant in Equation 5. For CdTe in the 1- μm island, $h/2$ resulted in 4.62 \AA .

The lattice constant “a” for wurtzite CdS was calculated by solving for “ a_{CdS} ” in the following equation;

$$\text{Equation 7} \quad d_{\text{CdS}(\bar{1}100)} = \frac{a_{\text{CdS}}}{\sqrt{3}} + \left(\frac{a_{\text{CdS}}}{\sqrt{3}} \right) \cos 60^\circ$$

where $d_{\text{CdS}(\bar{1}100)} = 3.59 \text{ \AA}$ = the measured d-spacing of the $\bar{1}100$ reflection in Figure 27 (d). The $\bar{1}100$ reflection corresponds to planes perpendicular to the interface. The distance between $\bar{1}100$ planes is shown in Figure 34 with a green letter “d”. The value for the lattice constant “a” of the CdS resulted in 4.14 \AA for the 1- μm island.

Using $h/2 = 4.62 \text{ \AA}$ and $a_{\text{CdS}} = 4.14 \text{ \AA}$, the CdS/CdTe lattice mismatch was calculated to be 10.4 % using,

$$\text{Equation 8} \quad \text{lattice mismatch} = 100 \left(\frac{h/2 - a_{\text{CdS}}}{h/2} \right)$$

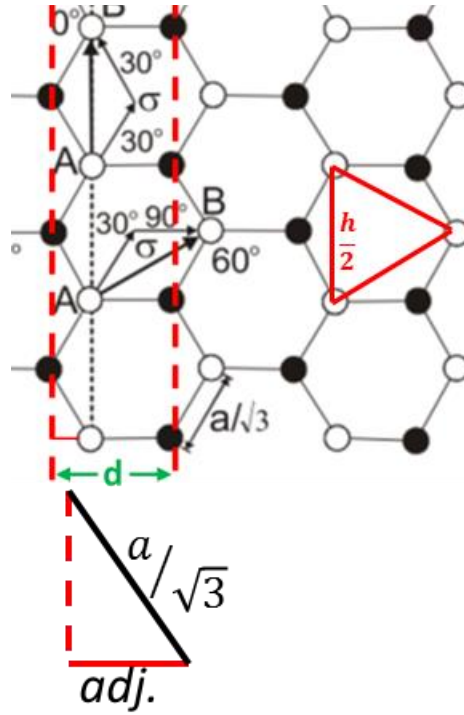


Figure 34 Shows the schematic used to calculate the lattice parameter “a” of CdS [50].

6.2.2 Detailed Analysis of the 136-nm Island

The high-resolution cross-sectional TEM image of the 136-nm island was studied with the structure guides shown in Figure 29. The atomic stacking of the CdS substrate matched the wurtzite atomic stacking when the structure guide was superimposed in Figure 35 as expected. The atomic stacking of the CdTe island matched the WZ configuration when the structure guides were superimposed in the high-resolution TEM image. Very close to the interface intrinsic and extrinsic faults formed. After a few nanometers the stacking faults disappear and the atomic stacking continued as WZ as shown in Figure 35 [51].

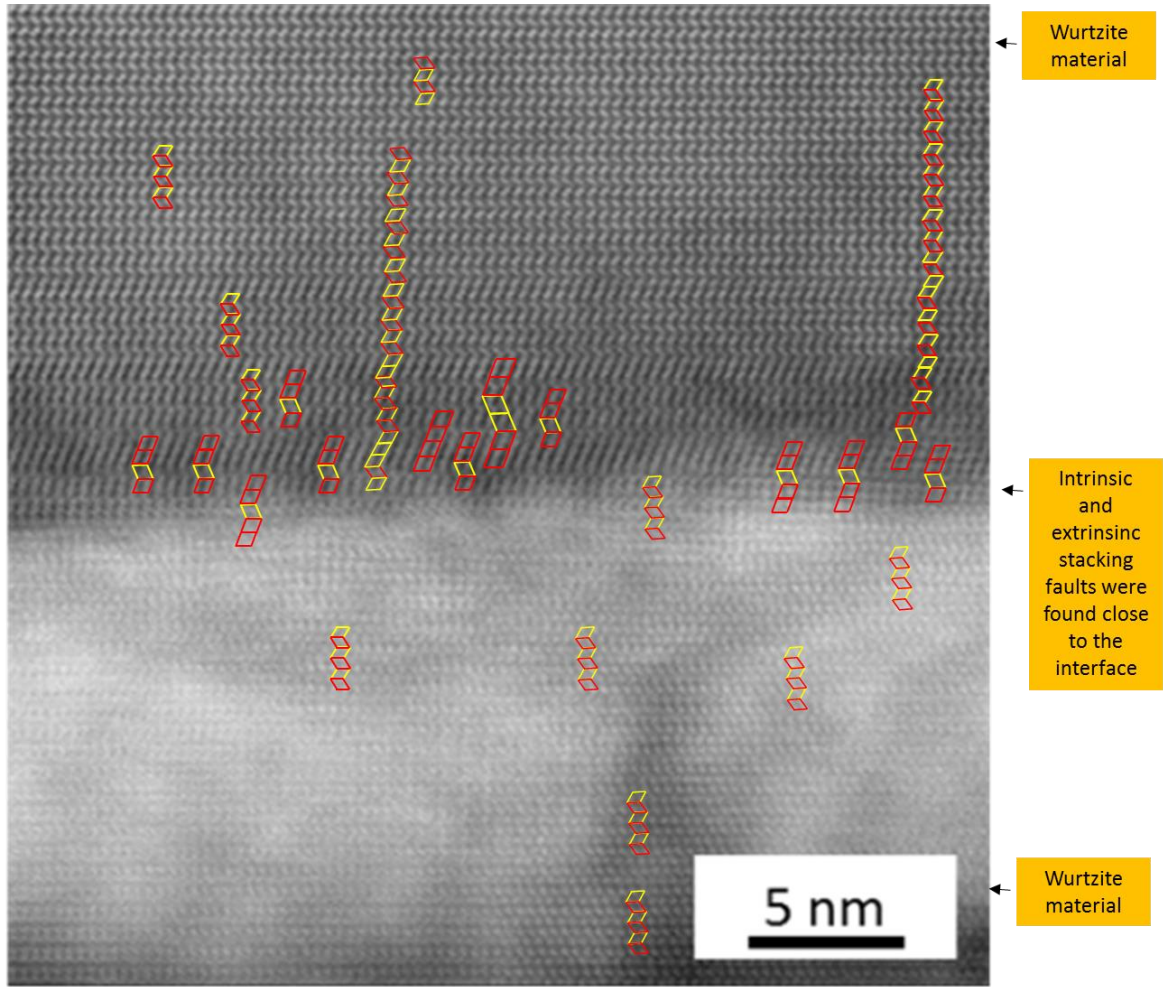


Figure 35 Structure guides superimposed in TEM images to determine the atomic stacking and stacking fault types in the 136-nm-sized CdTe island.

CdTe grew in the wurtzite configuration in the 136-nm island. To calculate the CdS/CdTe lattice mismatch, the lattice constants were calculated using the (010) reflections in Figure 27 (f) and Equation 7 to solve for “a”. Since both CdS and CdTe structures are hexagonal in this island, the lattice constants of the two hexagonal structures were used to calculate the lattice mismatch using

$$\text{Equation 9} \quad \text{lattice mismatch} = \frac{a_{\text{CdTe}} - a_{\text{CdS}}}{a_{\text{CdTe}}}.$$

The lattice mismatch resulted in 8.37 %. A reduction in the CdS/CdTe lattice mismatch suggests that CdTe is under compressive strain and CdS under tensile strain to reduce the formation of misfit dislocations at the interface. In this manner, material defects are reduced in CdTe and high quality material is grown. Figure 36 shows a schematic of a substrate under tension and an epilayer under compression. Similar to the CdS/CdTe system, the lattice constant of the substrate material is smaller than the lattice constant of the film.

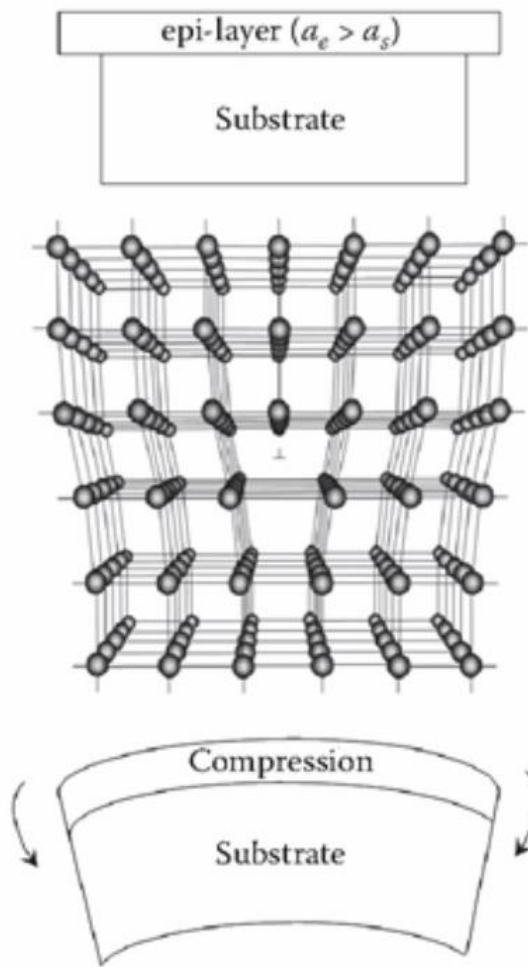


Figure 36 Shows a schematic of a lattice mismatch system where the substrate has a smaller lattice constant than the epi-layer. Substrate is under tension and epi-layer under compression [53].

The lattice mismatch was calculated for different orientations in the 136-nm island. Since all CdS and CdTe reflections in Figure 27 (f) align and both materials have a wurtzite

configuration, the lattice mismatch is equivalent to the d-spacing mismatch. The d-spacings were measured from the FFTs for each orientation in Figure 27 (f) and the mismatch was calculated using,

$$\text{Equation 10} \quad \text{Mismatch} = 100 \left(\frac{d_{\text{CdTe}} - d_{\text{CdS}}}{d_{\text{CdTe}}} \right)$$

Figure 37 shows the CdS/CdTe mismatch for each orientation shown in Figure 27 (f). Tetragonal distortion can be seen from Figure 37 because the mismatch is different in each orientation. Planes that are perpendicular to the interface are more strained compared to the planes that are parallel to the interface.

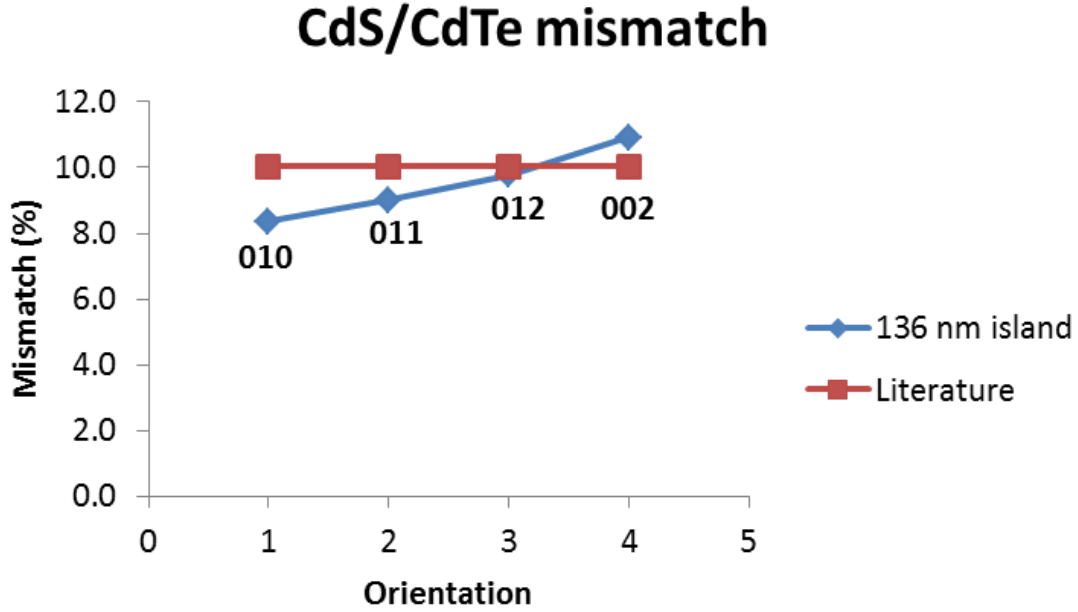


Figure 37 Shows the CdS/CdTe mismatch in the 136-nm island for the reflections indexed in Figure 27 (f).

The CdS/CdTe mismatch was also calculated using the bulk equilibrium values of lattice constant. For CdS ($a = 4.12 \text{ \AA}$, $c = 6.73 \text{ \AA}$) and CdTe ($a = 4.58 \text{ \AA}$, $c = 7.48 \text{ \AA}$) with wurtzite configurations, the d-spacing was calculated using,

$$\text{Equation 11} \quad \frac{1}{d^2} = \frac{4}{3} \left(\frac{h^2 + hk + k^2}{a^2} \right) + \frac{l^2}{c^2}$$

where hkl corresponds to the values of each reflection in Figure 27 (f). The mismatch was calculated using Equation 10. For all orientations the mismatch was $\sim 10\%$ as shown by the red line in Figure 37.

6.2.3 Detailed Analysis of the 250-nm Island

The high-resolution cross-sectional TEM image of the 250-nm island was studied with the structure guides shown in Figure 29. The atomic stacking of the CdS substrate matched the wurtzite atomic stacking away from the interface. Very close to the interface, there were some regions in the CdS substrate that had the ZB configuration. Also, intrinsic stacking faults were found as shown in Figure 38.

The atomic stacking of the 250-nm CdTe island matched the ZB configuration when the structure guides were superimposed in the high-resolution TEM image. As it is shown in Figure 38, stacking faults in CdTe resulted in the formation of twin boundaries close to the CdS/CdTe interface. Since CdTe grew in ZB configuration, the presence of ZB regions close to the surface of the CdS substrate suggests intermixing of CdTe or the formation of a strained CdTe epilayer of a few monolayers in thickness. After this region of mixed ZB and WZ atomic stacking, the interface becomes incoherent and then CdTe grows in a total ZB configuration.

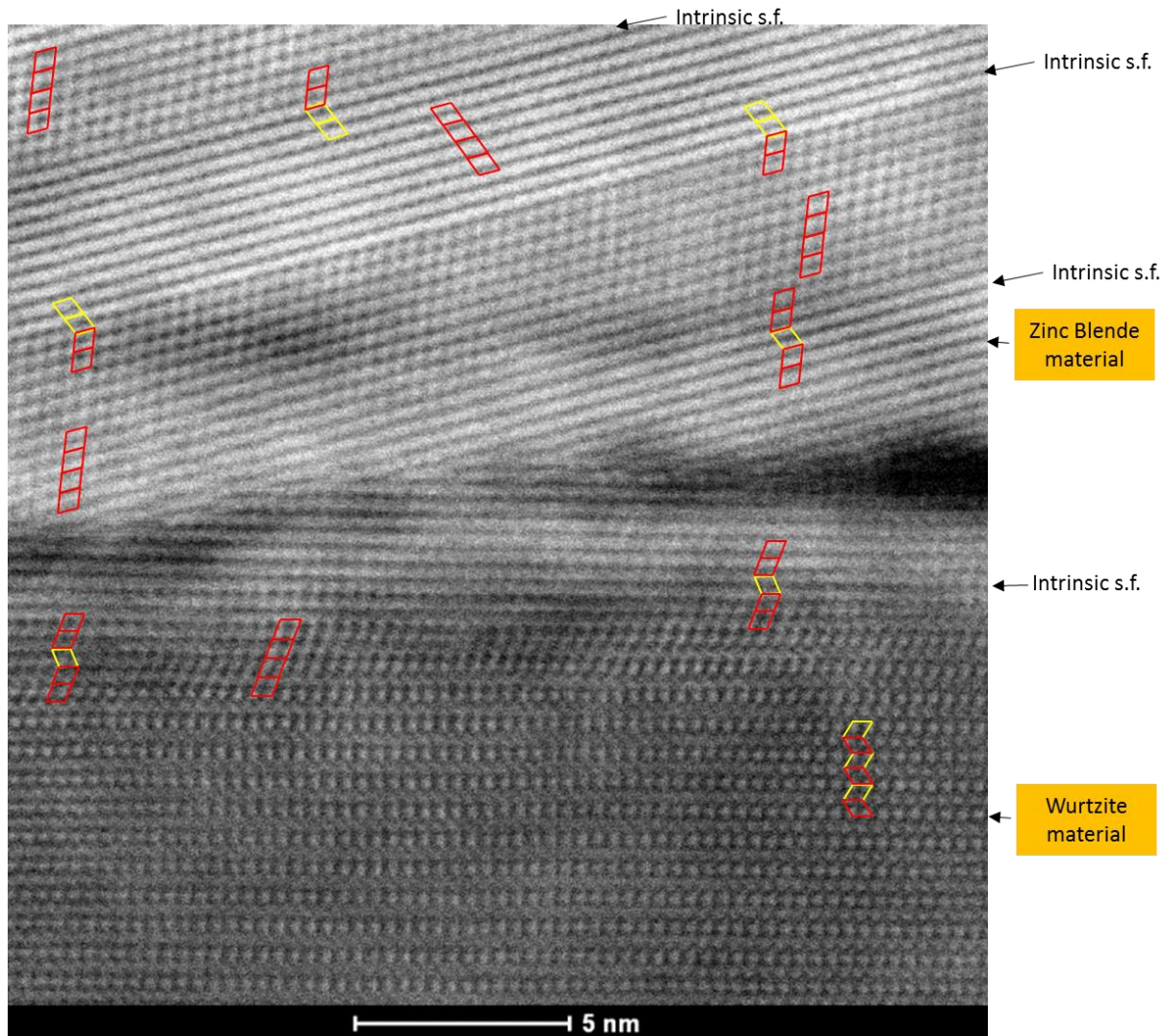


Figure 38 Structure guides superimposed in TEM images to determine the atomic stacking and stacking fault types in the 250-nm-sized CdTe island.

In the 250-nm island, the CdTe crystal rotated a few degrees to align to the CdS substrate. A set of CdTe planes perpendicular to the interface aligned very close to the ($\bar{1}100$) CdS planes. The inter-planar distance was measured and a mismatch of 0.51 % was calculated when comparing d-spacings close to the interface. The CdS/CdTe mismatch increased to 3.82 % when the CdTe d-spacing were compared to CdS d-spacings far from the interface. This indicates that CdS planes are under tensile strain close to the surface of the substrate but relax away from the

surface. The cross-sectional TEM image of the 250-nm island is shown in Figure 39 as well as a schematic that shows the strain in the CdS planes.

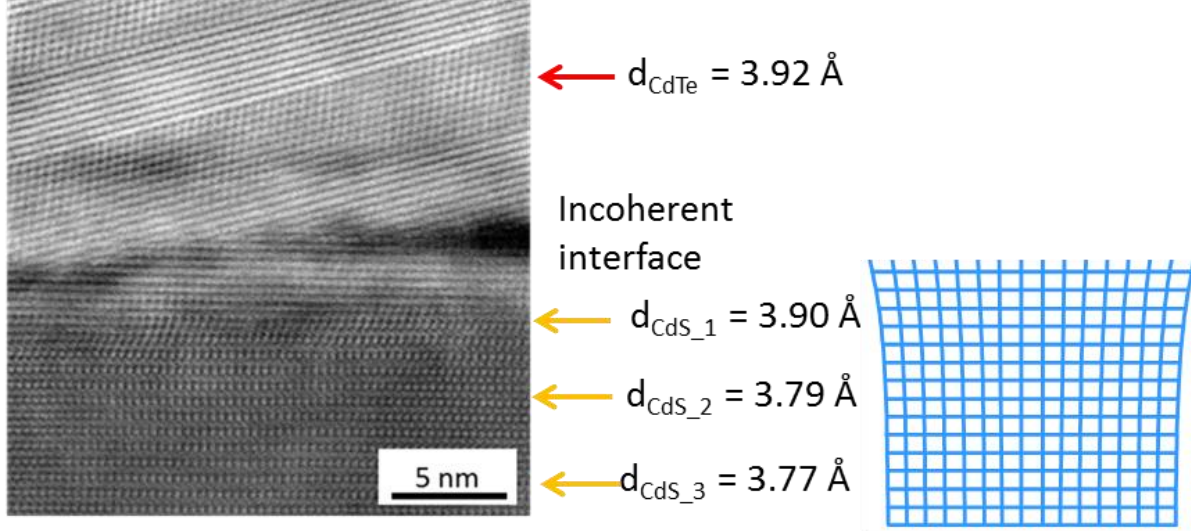


Figure 39 Shows a TEM image of a cross-sectional view of a 250-nm CdTe island grown on a single crystal CdS substrate. The d-spacing's for planes perpendicular to the CdS/CdTe interface are also shown. The schematic on the right illustrates CdS planes under tensile strain close to the interface as suggested by the d-spacing measurements.

A good alignment of some of the CdTe planes to the CdS planes is suggested by the low CdS/CdTe mismatch calculated for this island. However, the alignment of some of these planes caused a crystal rotation of the CdTe.

6.3 GROWTH MODEL

A model proposed to explain the CdTe growth directions inside different window sizes is shown in Figure 40. The number of nuclei inside the SiO_2 windows dictates the direction in which CdTe grows. 1- μm window size has multiple growth directions because multiple nuclei occur inside the SiO_2 window. When the window size is reduced, the growth is confined to a single nucleus, and CdTe grows only in one direction. Multiple nuclei are shown in the 1- μm island Figure 40 (a), as opposed to a single nucleus in Figure 40 (b). The red arrows in Figure 40 (c) and (d) represent the CdTe growth directions and the straight black lines represent twin boundaries. A similar observation was made on the SAG of CdTe in polycrystalline CdS

substrates, where EBSD showed that multiple CdTe grains with different orientations grew in micro-size SiO₂ windows and single grains grew in nano-scale windows [40].

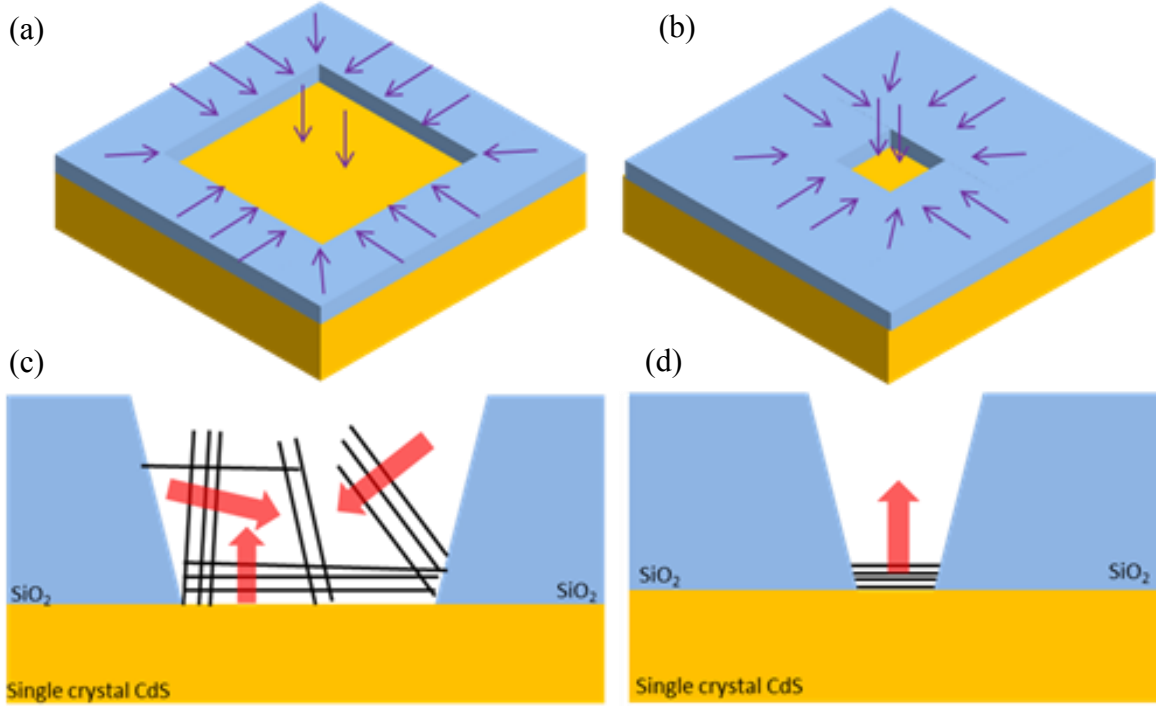


Figure 40 Shows a schematic representation of the growth mechanisms a) and b) and the initial nucleation c) and d) of CdTe inside micro and nano-size SiO₂ windows.

6.4 CdTe AWAY FROM INTERFACE

A reduction of defects away from the CdS/CdTe interface was also observed when the size of the CdTe island was reduced. High-resolution TEM images of CdTe away from the CdS/CdTe interface are shown in Figure 41 for three different island sizes. In the 1 μ m CdTe island, twin boundaries appear away from the CdS/CdTe as shown in Figure 41 (a). In the 250 nm island, twin boundaries appear away from the interface but they form parallel to the basal plane as shown in Figure 41 (b). For the 136 nm island size, no twin boundaries appear away from the CdS/CdTe interface as shown in Figure 41 (c).

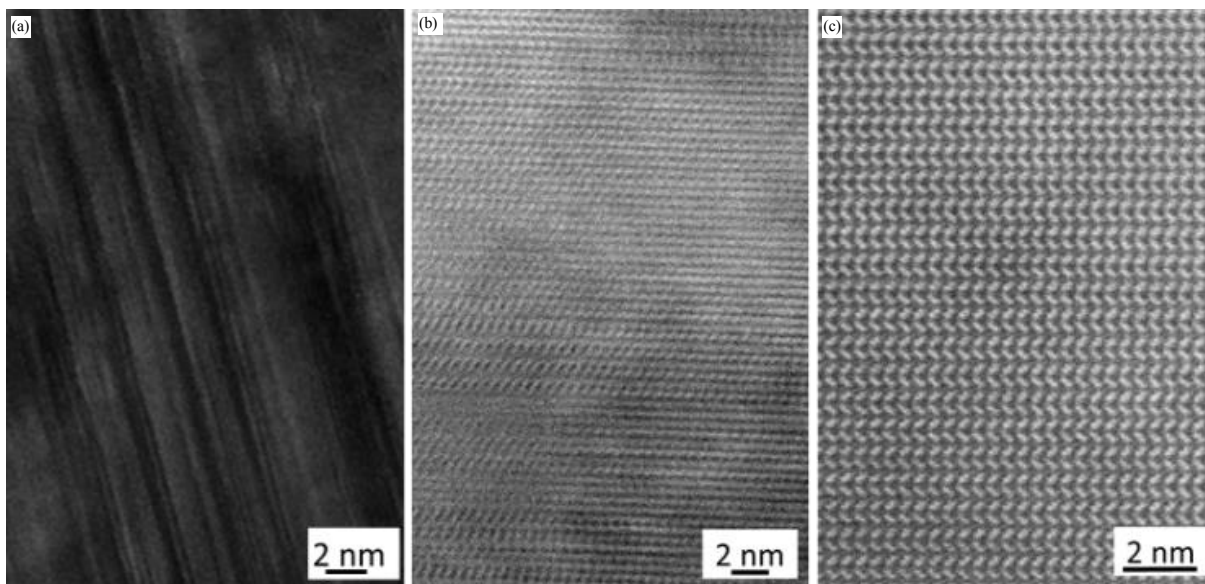


Figure 41 shows high magnification TEM images of CdTe far from the interface for 1 μm , 250 nm and 136 nm island sizes

Chapter 7: Electrical – Microstructural Characterization

The relationship between the electrical performance and microstructure was studied using conductive AFM (CAFM), SEM, and cross-sectional TEM (XTEM) characterization of groups of indexed CdTe/CdS cells. Non-destructive conductive AFM and SEM were performed first followed by destructive XTEM. In this way, a direct comparison was made between the J-V and microstructure of several indexed cells. In one set of experiments material morphology from SEM and AFM topology images were compared to electrical maps from CAFM. On another set of experiments J-V characteristics from CAFM were compared to cross-sectional images of the CdTe/CdS device from XTEM. In order to understand the effect of the device structure on the J-V characteristic, a simulation was performed using wxAMPS by using a structure similar to the miniature experimental cells.

7.1 CONDUCTIVE AFM CHARACTERIZATION

Conductive atomic force microscopy (CAFM) was performed to study the electrical properties of CdTe islands selectively- grown on glass/ITO/polycrystalline-CdS substrates. CAFM provides good spatial resolution to test several CdTe nano-islands as a group or individually. In order to study the electrical behavior of arrays of islands, electric current maps were taken from several islands. To study the electrical performance of individual islands, J-V measurements were taken of individual CdTe islands. Electric measurements under dark conditions were taken with a Veeco DI Dimension 3100 AFM system using a Pt/Ti coated cantilever. Electric measurements under light conditions were taken with an Asylum Research MFP-3D-BIO AFM system using a diamond cantilever.

7.2 MATERIAL TOPOLOGY TO ELECTRIC CURRENT MAP COMPARISON

Electric current maps were used to test several CdTe islands at the same time. Electric current maps are color coded AFM images that map the electrical activity of a sample under test. In this work, bright colors in an AFM electric current image represent electric current flow and

opaque colors represent no current flow. The first sample under test was a group of CdTe microislands grown on glass/ITO/CdS substrates. Figure 42 shows AFM images of the morphology (a) and electrical activity (c) of a group of CdTe microislands. From Figure 42 (a) it can be seen that CdTe islands grew selectively and physically isolated from each other. From Figure 42 (c) it is observed that current flows only through the CdTe islands and that the SiO₂ stays electrically inactive. This indicates that CdTe islands are electrically isolated from the CdTe side.

Electric current maps of a single CdTe microisland were taken to analyze the electric current flow within the island. Figure 42 (b) shows an AFM surface morphology image of a single CdTe island and its corresponding electric current map is shown in Figure 42 (d). From Figure 42 (d), it is observed that there are regions within the CdTe microisland with non-uniform electrical activity. This is indicated by the color contrast inside the island.

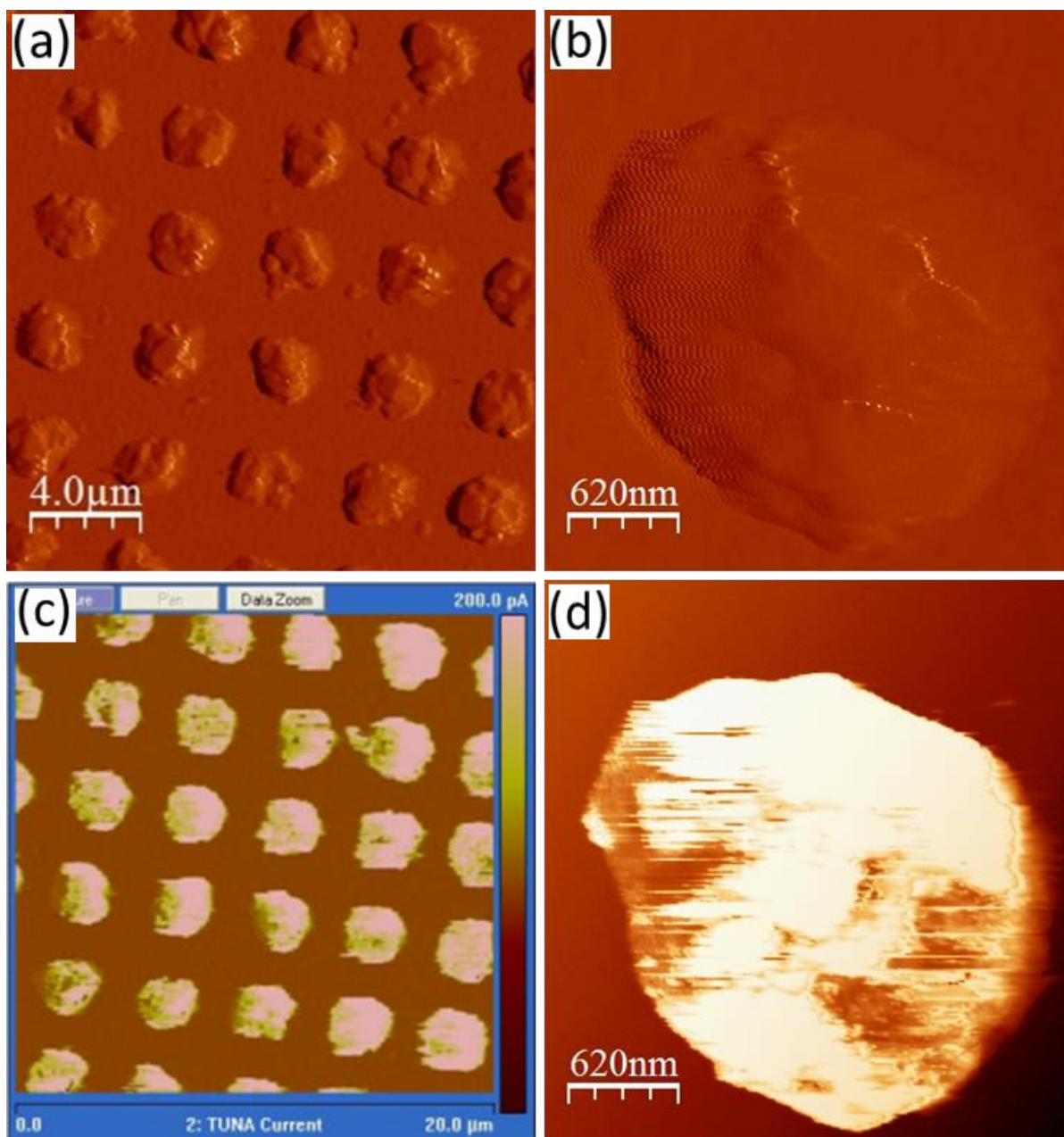


Figure 42 shows AFM images of the morphology of an array (a) of CdTe islands and of a single (b) CdTe island. Also, the electrical current map for an array (c) of CdTe islands and for a single (d) island are shown.

Electric current maps of nano-islands under dark conditions revealed differences in conductivity between nearby islands. Figure 43 (a) shows the SEM plan view of a group of CdTe nano-islands and its corresponding electric current map in Figure 43 (b). From Figure 43 (b), it is clearly seen that SiO₂ does not conduct and that electrical activity occurs only in the CdTe nano-

islands. One of the nano-islands (island 9) in Figure 43 shows no current flow. Since island 9 is not interconnected to other islands, its electrical behavior depends only on its material properties. This is an example of the use of this method to decouple the effect of defects on the electrical performance of CdTe.

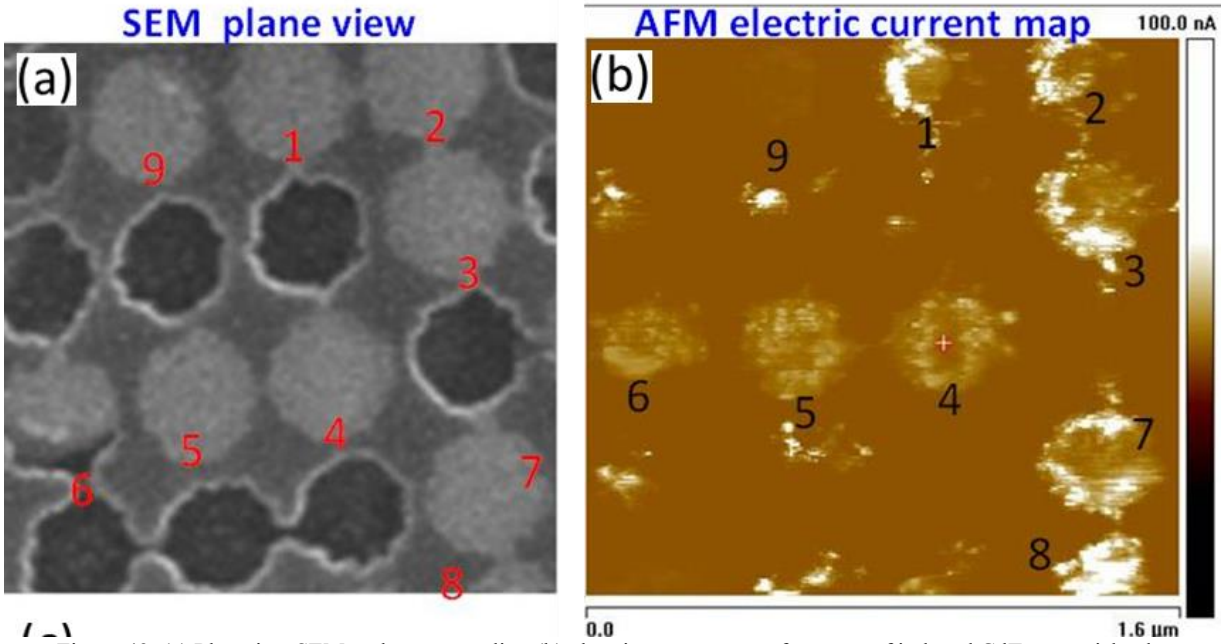


Figure 43. (a) Plan view SEM and corresponding (b) electric current map of a group of indexed CdTe nano-islands.

7.3 HIGH-RESOLUTION MICROSTRUCTURE TO CURRENT-VOLTAGE COMPARISON

In order to study the microstructure of the CdTe nano-islands, the island identification process described in chapter 3 was used to identify a group of nano-islands with SEM, AFM and TEM characterization tools. The nano-islands in Figure 44 (a) were first indexed using an SEM. Then, the same area shown in Figure 44 (a) was tested electrically with an AFM under dark conditions. Two of the IV curves for two separated nano-islands are shown in Figure 44 (c). It was observed that islands 32 and 37 had different IV characteristics and that both of them lie in the same row of islands enclosed by the red dashed rectangle. Island 37 has a very flat IV response and island 32 has an exponential response, as expected from a pn junction under dark

conditions. The next step was to remove a row of islands from the sample containing islands 32 and 37 and prepare the sample for TEM analysis. The standard lift-out process was used to prepare a thin lamella containing islands 32 and 37. The sample was finally mounted in a TEM holder as shown in Figure 44 (b).

Low-magnification TEM images were taken from each of the islands, and the results are shown in Figure 45. From the initial TEM results, it can be seen that both islands contain CdTe that connects with the CdS thin film and makes a pn junction. The TEM from island 37 shows a multitude of black spots throughout the island. This could be due to the platinum precursor getting inside a small gap between the grown CdTe and the SiO₂ mask for this specific island as observed from Figure 44 (a). On the other hand, in island 32 there seems to show no contamination from the platinum precursor because, as shown in Figure 10, there are no gaps between the grown CdTe island and the SiO₂. The CdS and CdTe materials and interface are observed in Figure 44. It is also seems that the CdS under island 32 was consumed for a few nano-meters and probably formed a CdTeS junction at the interface. The electrical performance of CdTe nano-islands was also tested under light conditions, and the results are shown in the next subsection.

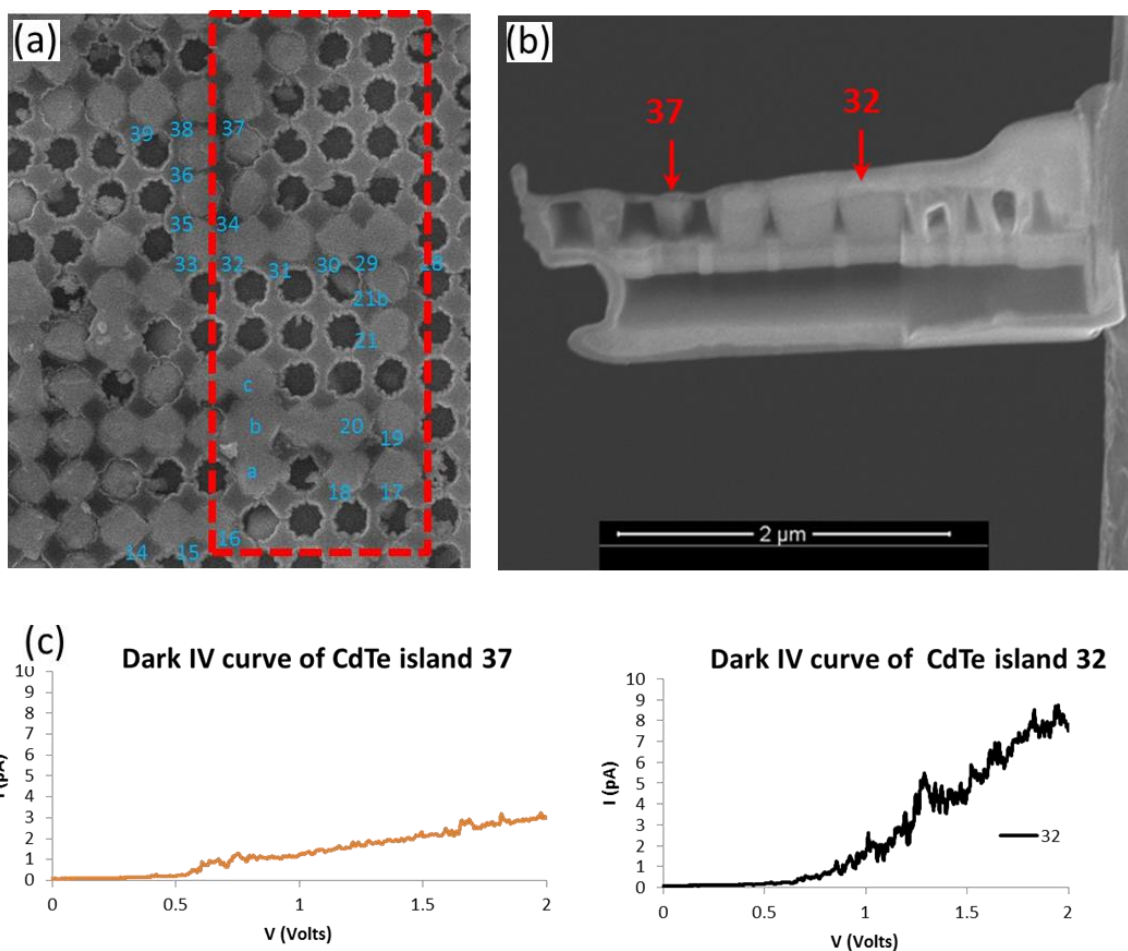


Figure 44 shows (a) the SEM plan view image showing an array of indexed CdTe nano-islands, (b) the IV characteristics of two nano-islands and (c) the SEM cross-section view of a thin lamella prepared for TEM that contains a row of islands tested electrically from the area shown in (a).

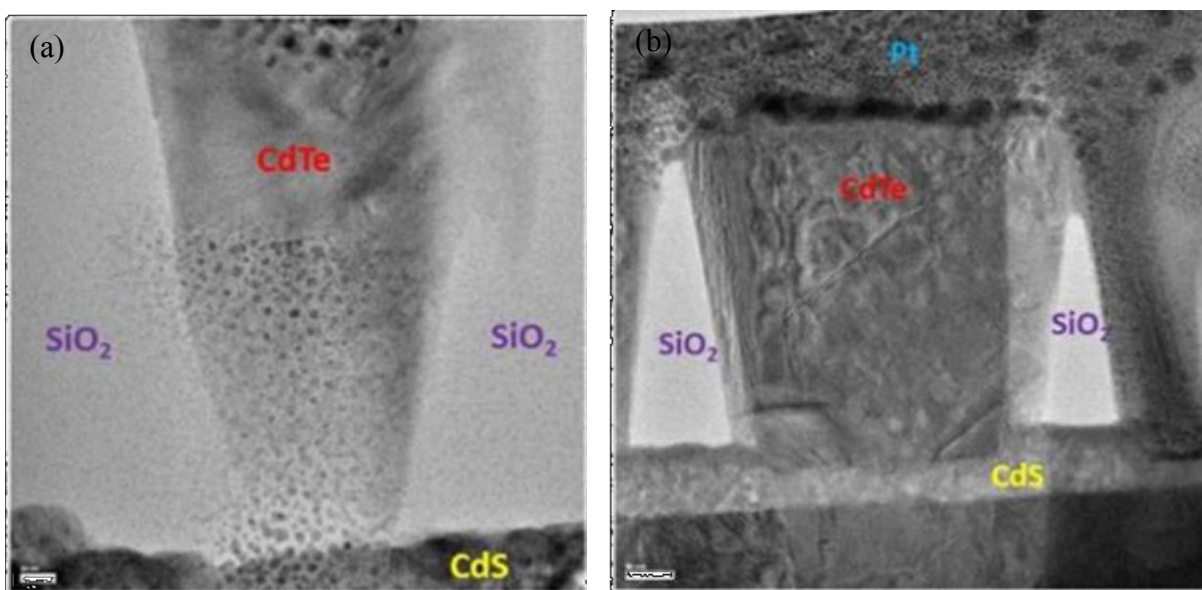


Figure 45 shows the low magnification TEM cross-section view of (a) island 37 and (b) island 32 shown in Figure 44

Nano CdTe islands were tested under illumination using an AFM and an external light source which is connected to the bottom of the AFM using a fiber optic light guide. The light source has a xenon arc lamp inside. The intensity of the light source was calculated when the light was focused on the sample as shown in the appendix in Figure 52. A polycrystalline silicon solar cell was used to calculate the light intensity when it was focused on the sample. More information on the light calibration is included in the Appendix B.

Several CdTe nano-islands were indexed, tested under illumination and prepared for TEM analysis. The SEM plan view of two nano-islands is shown in Figure 46 (a), and their corresponding J-V curves are shown in Figure 46 (b). Both CdTe nano-islands were tested under the illumination setup described in the appendix B, and their J-V characteristics showed power generation. It can be seen from Figure 46 (b) that both islands have an exponential J-V characteristic with short circuit current (J_{sc}) and open circuit voltage (V_{oc}) points typical of a solar cell. One of the islands (spot 1) shows less J_{sc} and V_{oc} compared to the second island (spot 2).

The initial micro-structure to electrical correlation is observed between surface SEM (Figure 46 (a)) and the J-V characteristics shown Figure 46 (b). To obtain a more detailed understanding on the effect of defects and electrical performance, the samples were prepared for TEM and placed in a TEM grid as shown in Figure 46 (c). Figure 46 (c) shows an SEM cross-section view of a thin foil extracted from the sample that contains spot 1 and spot 2. This is an excellent method to correlate the micro and atomic structure of materials to the electrical performance.

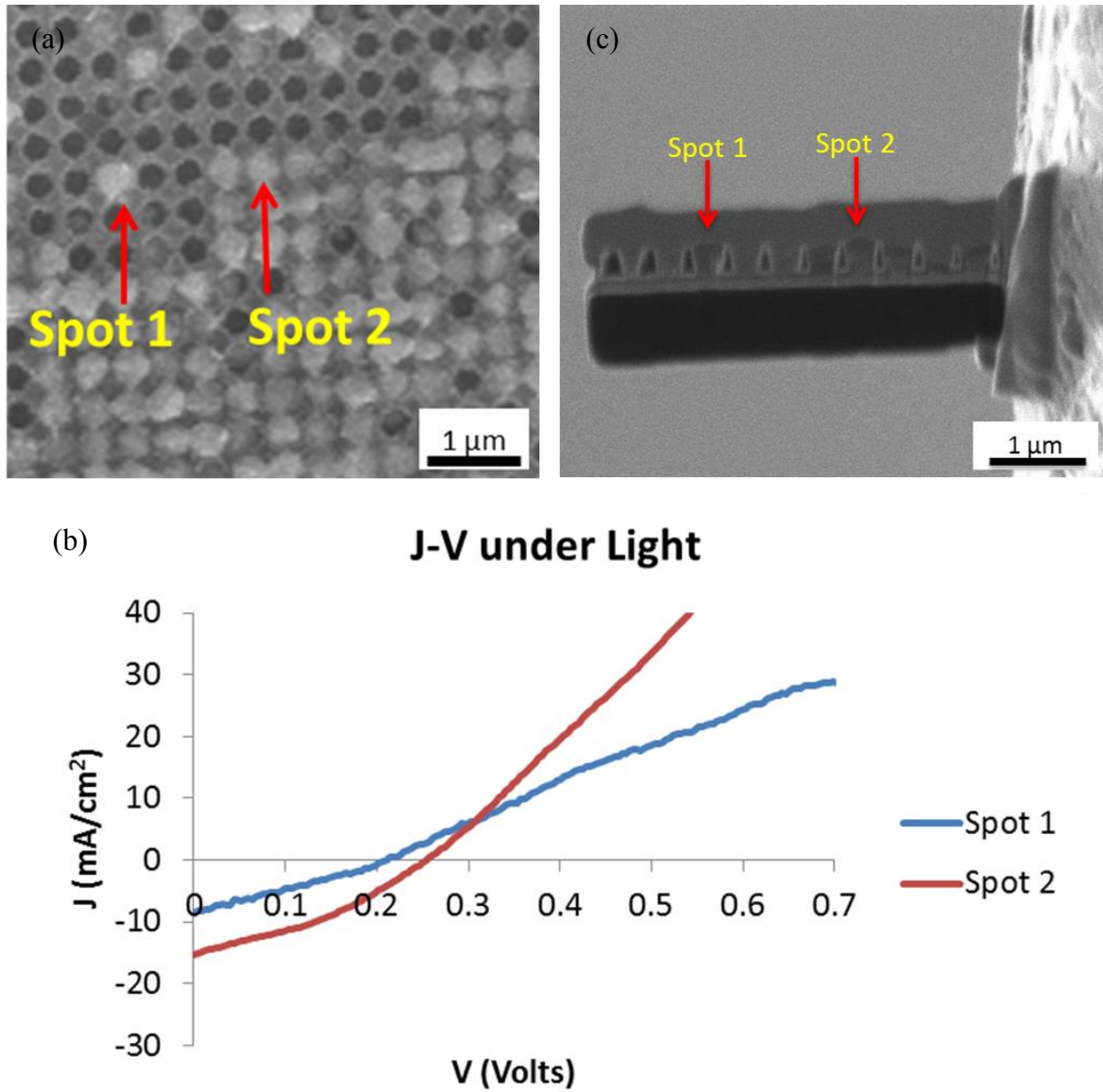


Figure 46 Shows (a) SEM plan view of two islands of interest and (b) their corresponding J-V characteristics. Also, (c) shows the SEM cross-section view of a lamella that contains the two islands shown in (a).

7.4 J-V DEVICE SIMULATIONS

Device simulations were performed in wxAMPS [58] to analyze the effect of CdTe thickness and surface recombination on the electrical performance of CdTe solar cells. A CdS/CdTe structure was made in wxAMPS using the baseline device proposed by Gloeckler [59]. SnO₂, CdS and CdTe film thicknesses were adjusted to represent the nano-pn junctions

fabricated in section 7.3. Device simulations were run for devices with constant SnO₂ and CdS thickness but variable CdTe thickness and bulk defect density.

The effect of CdTe thickness and defect density on V_{oc} is shown in Figure 47. The maximum CdTe thickness was limited to 1.25 μm to study devices with thicknesses close to the thicknesses fabricated in the experimental section of this work. As the bulk defect density increased, the V_{oc} decreased. This was expected since more carriers recombine when there are more defects. However, for small CdTe thicknesses, the thickness dominated the V_{oc} . Figure 47 shows that below 0.7 μm the V_{oc} is dominated by the CdTe thickness. This is because the depletion region in the device is limited by the CdTe thickness and therefore, the electric field in the pn junction is reduced. Since voltage is proportional to electric field, the V_{oc} decrease for very thin CdTe devices.

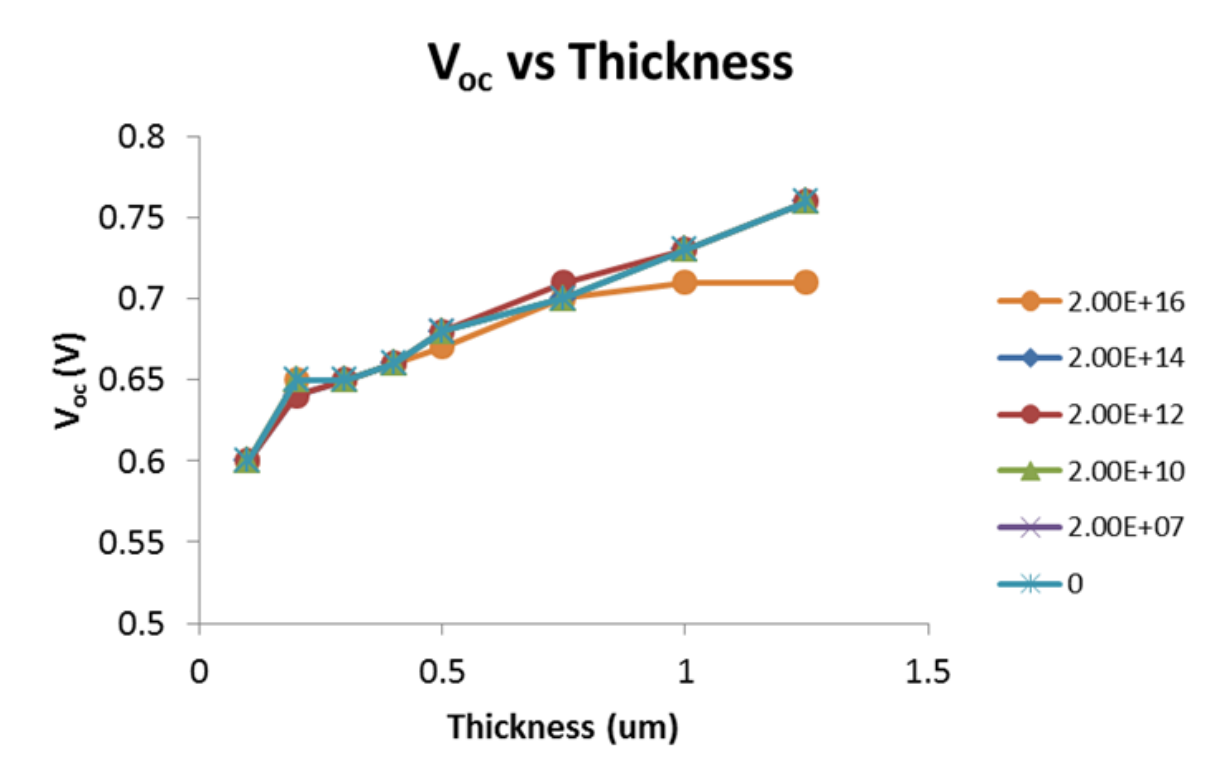


Figure 47 Shows the V_{oc} of a simulated CdS/CdTe device as a function of CdTe thickness and defect density.

The effect of surface recombination on very thin CdTe devices has a big impact on the device performance. To simulate surface recombination in wxAMPS, a 3-nm thick CdTe film with defects was added to the baseline device proposed by Gloeckler. This layer is labeled surface recombination in Figure 48. High surface recombination velocity values were simulated by increasing the defect density in the surface recombination layer. Similarly, low recombination velocities were simulated by decreasing the defect density. The effect of surface recombination on the device of Figure 48 is shown in Figure 49. The CdTe bulk defect density was set to 2×10^7 . As the defect density in the surface recombination layer is increased, the V_{oc} of the device decreases.

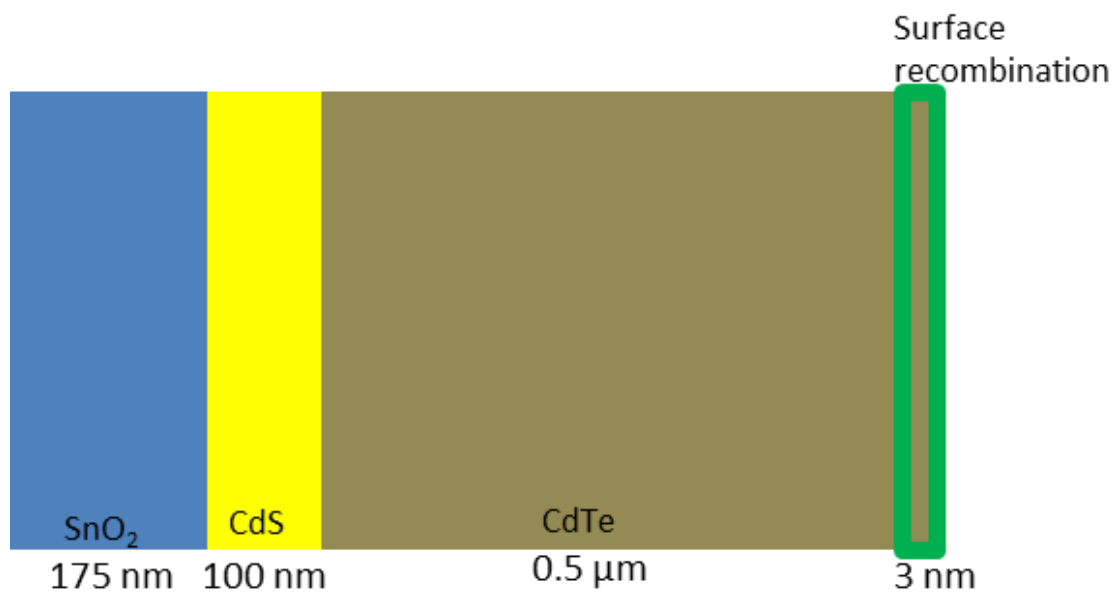


Figure 48 Shows the surface recombination layer added to a CdTe device with a thickness of 0.5 μm .

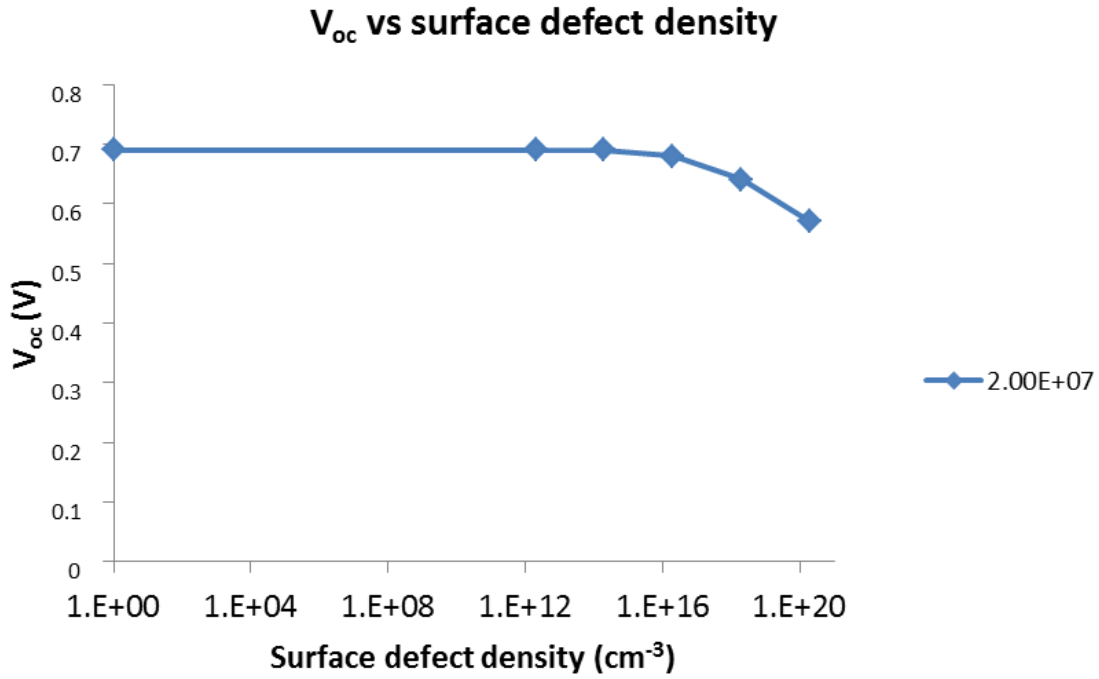


Figure 49 Shows the Voc of a CdS/CdTe solar cell as a function of defect density at the surface recombination layer shown in Figure 48

The effect of CdTe thickness and surface recombination on very thin CdTe devices is critical on their electrical performance. The CdTe nano-pn junctions fabricated in this work have thicknesses below 500 nm and very large surface area. Device simulations indicate the need of a surface passivation layer or treatment to enhance electrical performance of the nano-pn junctions shown in the previous section. Increasing the CdTe thickness of the islands and interconnecting them through lateral overgrowth would prevent the effects of thickness on V_{oc} . Also, islands could be electrically passivated by doping their edges.

Chapter 8: Conclusions

CdTe is an excellent semiconductor for solar cell fabrication; however, its conversion efficiency is limited by low V_{oc} values. Low voltages are attributed to defects in CdTe, but there is still uncertainty in the effect of different kind of defects on the electrical performance. In this work, a method was created to decouple the effect of different kinds of defects on the electrical performance of CdTe through selective area growth. A one-to-one correlation between materials and electrical performance is possible at the nano-scale using this method,

CdTe was successfully grown selectively on patterned glass/ITO/polycrystalline-CdS substrates and on patterned single crystal CdS substrates. Positive selectivity was confirmed with SEM. Reduction of grains and intra-grain boundaries were accomplished by reducing the SiO_2 window size to 300 nm. EBSD and SEM/FIB studies confirmed that CdTe grew as a single grain per nano-window vs. multiple grains per micro-window.

CdTe micro- and nano-islands were successfully prepared for EBSD and TEM studies. FIB planarization of CdTe islands provided smooth surfaces suitable for EBSD analysis. In-situ lift-out process was implemented for TEM lamella preparation. Thin lamellas containing CdTe micro and nano-islands were suitable for electron transparency and TEM characterization.

CdTe micro and nano-islands were successfully indexed and identified by different characterization instruments. FIB marks with various sizes and shapes were used to locate single CdTe nano-islands within a sample using different characterization instruments.

Quality of CdTe was improved by means of selective area growth on patterned single crystal CdS substrates. The lattice mismatch between CdS and CdTe was reduced from 10% to 8.37% by growing CdTe inside a 136-nm window size. FFT analysis showed better alignment between CdS and CdTe when window sizes were reduced to 136 nm.

Micro and nano-CdTe pn junctions were successfully fabricated and tested. pn junctions behaved as diodes and generated power under light conditions. The nano-islands were

electrically isolated from the CdTe side and their electrical behavior depended on their individual material structure.

Simulations showed the effect of CdTe thickness and passivation on the electrical performance of nano-scale CdTe islands. It was found that for CdTe thicknesses below 500 nm, the V_{oc} of pn-junctions was dominated by the thickness of the devices and surface recombination.

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Appendix A

An alternative way to represent TEM images (real space) is using FFTs (reciprocal space). An FFT is an array of spots (or reflections) that represent the atomic planes of a TEM image. Each spot represents a set of planes. Alternatively, if a set of spots (reciprocal space) is given in a form of an FFT, taking the inverse FFT (IFFT) of the set of spots will result in a real space image. To illustrate this, the FFT of Figure 50 (a) is shown in Figure 50 (b). For each reflection corresponding to the CdS, the IFFT was taken and the planes are shown in Figure 51 (a-d).

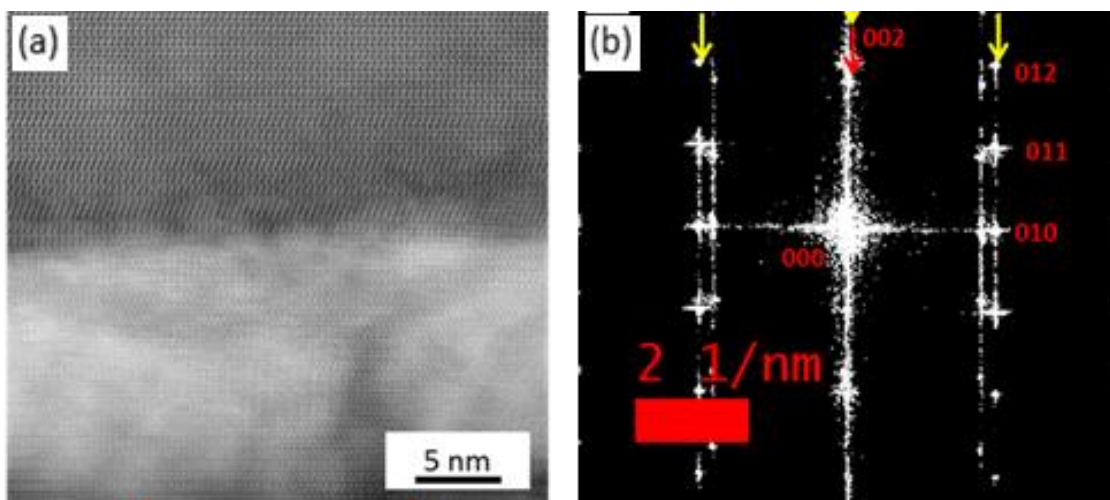


Figure 50 (a) Shows a CdS/CdTe interface and (b) the FFT of (a)

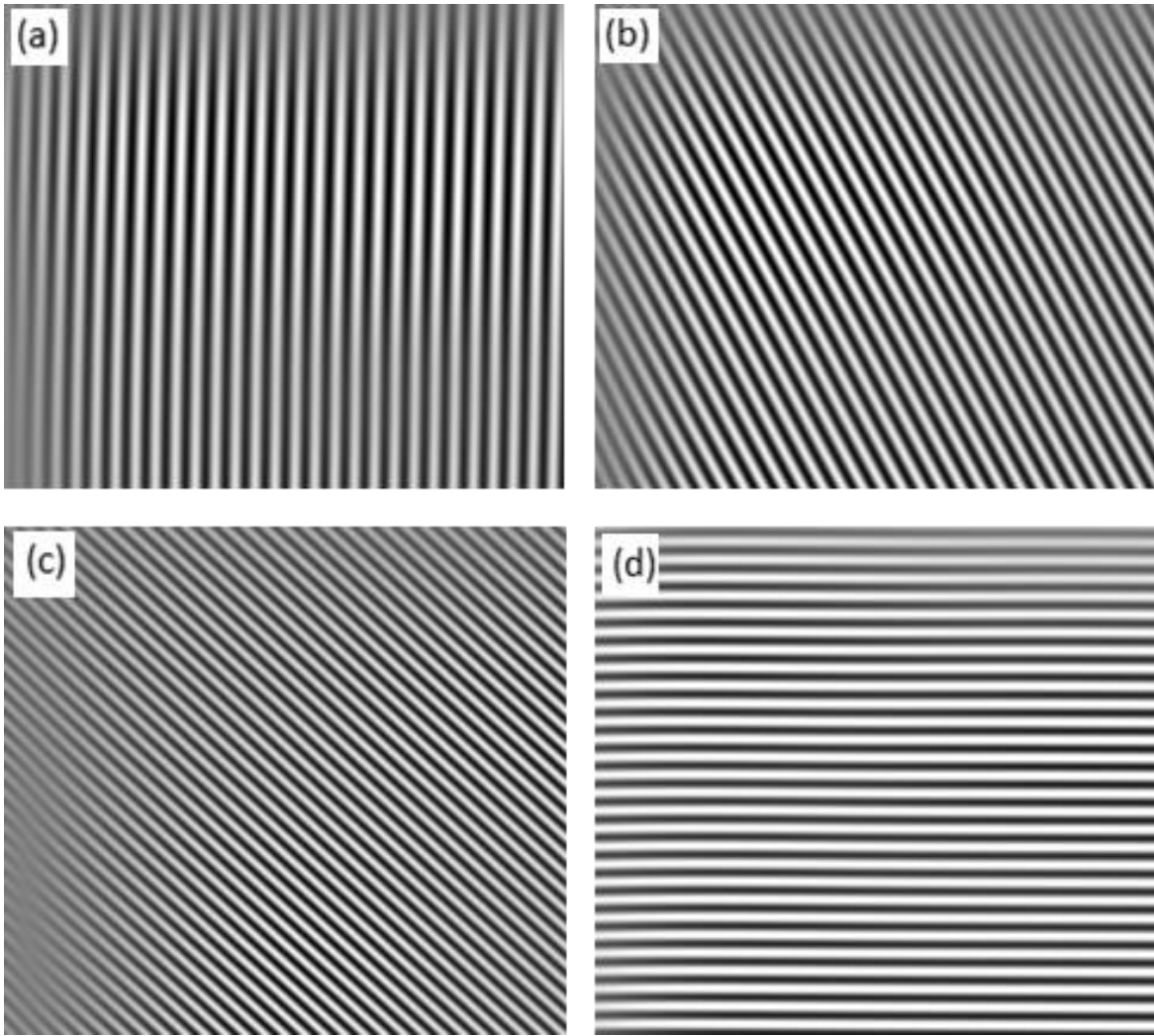


Figure 51 Shows the IFFT of reflections (a) 010, (b) 011, (c) 012, and (d) 002 in Figure 50 (b)

Appendix B

Light intensity estimation was made using a solar simulator and a commercial polycrystalline solar cell. First, the IV characteristics of a polycrystalline solar cell were measured with a calibrated New Port solar simulator under one sun as shown in Figure 53. The current and illuminated area of the solar cell was measured and compared to the current and illuminated area measured when light was focused on a small spot (as shown in Figure 52) in the AFM. A light intensity of 1.67 suns was estimated when light was focused on a small area of the sample placed in the AFM. Current measurements shown in section 8.4 were divided by 1.67 to estimate performance of nano-pn junctions under 1 sun.

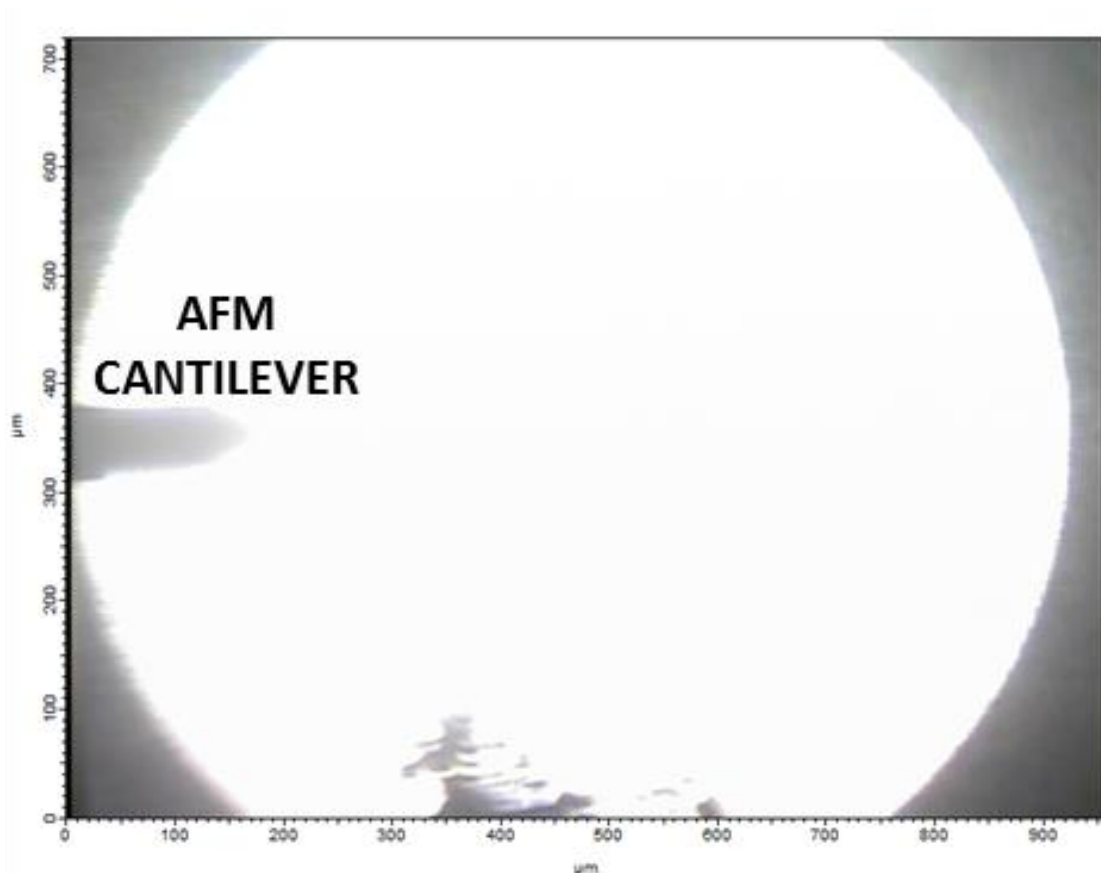


Figure 52 Shows an image from the top of the AFM cantilever sitting on top of a patterned CdTe sample illuminated from below. The light source is focused on the patterned CdTe equipped with an external light source with a xenon arc lamp.

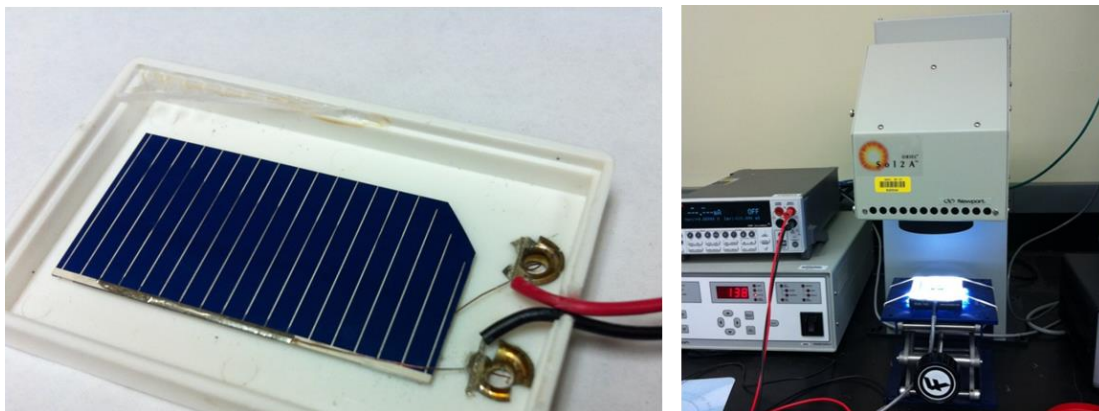


Figure 53 Commercial polycrystalline silicon solar cell and one-sun simulator from Newport used to calculate the light intensity in the AFM system.

Vita

Brandon Aguirre earned his Bachelor of Science in Electrical Engineering and Master of Science in Electrical Engineering from The University of Texas at El Paso in 2006 and 2009 respectively. In 2010 he joined the doctoral program in Electrical and Computer Engineering at The University of Texas at El Paso. Brandon received the Hispanic Engineer National Achievement Awards Conference (HENAAC) Robert and Debbie Amezcua Scholarship for three consecutive years, the National Science Foundation (NSF) Bridge to the Doctorate Fellowship and the NSF Solar Economy Integrative Graduate Education and Research Traineeship (SEIGERT) Fellowship.

Brandon Aguirre performed part of his doctoral research at the Center for Integrated Nanotechnologies (CINT) while interning at Sandia National Laboratories for three years. He participated as a summer visiting scholar in the Center for Energy Efficiency Electronics Science (E³S) at University of California Berkeley. In addition, he was one out of twelve students selected across the United States to participate in the international Winter School for Graduate Students at Indian Institute of Technology in Mumbai, India.

Brandon Aguirre has presented his research at international conference meetings including the Institute of Electrical and Electronics Engineers (IEEE) Photovoltaic Specialists Conference. Additionally he has authored two journal articles and co-authored five conference articles.

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