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# Effect of Si Substrate Orientation on the Quality of CdTe Selective Growth on Si(111) and Si(211) Substrates via Closed-Space Sublimation (CSS) without the use of a Mask.

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## **Dedication**

*I would like to dedicate this dissertation to my husband Hugo Najera for all his support, guidance and patience that I received throughout my Ph.D. career. Thank you for believing in myself to accomplish this milestone in my life, becoming a Doctor of Philosophy in Electrical Engineering.*

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ARYZBE NAJERA, M.S.E.E.

DISSERTATION

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## Abstract

The material, fabrication and operation parameters for mercury cadmium telluride (HgCdTe) detectors require high sensitivity, small pixel size, low defect density, long-term thermal-cycling reliability and large area substrates. The focus of this work is on the epitaxial growth of CdTe thin films on Si(111) and Si(211) for the purpose of using the resulting material as a substrate for the subsequent growth of HgCdTe thin films. Currently, there is an interest to improve the quality of epitaxial thin films associated with the fabrication of HgCdTe infrared and X-ray imaging using the close-spaced sublimation (CSS) technique. The CSS technique is proven to produce high-quality CdTe films and is associated with high growth rates ( $> 1 \mu\text{m/h}$ ) compared to molecular beam epitaxy (MBE) and metalorganic vapor phase epitaxy (MOVPE) [1-3]. The higher cost and size limitation of high quality bulk CdTe substrates make Si substrates a more practical alternative. The use of Si substrates also allows the readout circuitry to be implemented on one chip.

There is a 19% lattice mismatch between CdTe and Si, which results in defects at the interface. The nanoheteroepitaxy (NHE) technique makes it possible to grow CdTe on Si substrates, usually with a ZnTe buffer layer, in order to decrease the defect density at the CdTe/Si interface [4]. It is expected that defects will be minimized for selective growth at the nanoscale as a result of strain partitioning between the substrate and the epilayer, which leads to a reduction in the number of defects at the interface [3,4].

Epitaxial CdTe growth on Si(211) substrates produces the highest quality material [5-9]. In contrast, polycrystalline CdTe grown for solar cell applications, results in CdTe grown predominately in the (111) orientation [10-13]. This study is based on observations from the literature associated with the fabrication parameters that affect the quality of CdTe growth. These include the substrate temperature, source temperature, reactor pressure, substrate orientation, source quality and pattern/pillar size [3,5,6,8,9]. Scanning electron microscopy (SEM) and transmission electron microscopy (TEM) is used

to determine the effect of these fabrication parameters on the quality of the CdTe growth and the misorientation at the CdTe/Si interface.



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## Chapter 1: Introduction

### 1.1. IMPORTANCE OF SELECTIVE NANO-HETEROEPITAXIAL GROWTH OF CdTe FOR THE SUBSEQUENT GROWTH OF HgCdTe

Since 1958, and until recently, mercury cadmium telluride (HgCdTe), has been the substrate of choice for infrared (IR) detectors and Focal Plane Arrays (FPAs). HgCdTe has been shown to have high percent absorption for radiation in the long-wavelength infrared (LWIR) with wavelengths between 8 to 14  $\mu\text{m}$  [14]. Substrates for IR detector thin films require a lattice matched film, preferably grown on silicon (Si), and with low defects. The fabrication of IR detectors not only requires a low defect film, but a substrate that will result in long-term-thermal-cycle reliability [15,16]. One alternative to bulk HgCdTe or CdTe substrates is to use high quality, low defect CdTe grown on Si substrates. The drawback to using the CdTe-Si material system is the large lattice mismatch (19%) between CdTe and Si [17]. The lattice mismatch leads to strain and defects at the CdTe-Si interface. The main factors impacting the quality of HgCdTe IR detectors are threading dislocations. These defects propagate into HgCdTe epilayer, and act as Shockley-Read-Hall recombination centers, limiting the lifetime and performance of the detector.

Currently, there is an interest in the research of HgCdTe Infrared (IR) detectors to reduce the defect density in the substrate used for HgCdTe growth. CdTe layers produced by high lattice-mismatched systems such as CdTe/Si, need to be improved for the subsequent growth of HgCdTe. When the lattice mismatch is high, an alternate growth mechanism is required in order to alleviate strain at the interface [14]. The lowest etch-pit density (EPD) for CdTe growth on buffered Si substrates is in the low  $10^5 \text{ cm}^{-2}$  [18]. Nano-heteroepitaxy (NHE) has been proposed to reduce the high strain in lattice-mismatched material systems [19]. NHE can be used to reduce stress in a three dimensional geometry by selective growth on nanoscale patterned substrates (40-50 nm) with defect free growth for material systems with no more than 4.3% lattice mismatch [17]. The NHE technique can be used to grow CdTe

on Si using the Closed-space Sublimation (CSS) technique, in order to reduce production costs and the fabrication time of CdTe films for infrared detector applications. The ability to selectively deposit CdTe on patterned Si(111) and Si(211) substrates without the use of a mask has not been observed before using the CSS technique.

## **1.2. MOTIVATION OF THIS DISSERTATION**

### **1.2.1 Significance of selective CdTe Growth on Si Substrates**

HgCdTe has been the most widely used compound semiconductor material for military, civil and commercial infrared applications. The choice of CdTe/Si as a suitable substrate is based on efforts to minimize lattice mismatch while considering chemical compatibility and the use of Si for electronic circuit integration [22]. For this reason, special attention has been given to the direct growth of CdTe on Si substrates for the development of large-area substrates suitable for HgCdTe [7,22]. Moreover, Bailly *et al.*[21] have shown from a theoretical model of heteroepitaxial growth that CdTe tends to grow in the <111> direction on Si(100) substrates. The growth of <111> CdTe on Si(100) substrates lowers the lattice mismatch to 3.4 % along the <211> axis [24]. The epitaxial growth of CdTe on Si substrates will help to reduce the thermal mismatch problems during the fabrication process of a silicon readout chip with signal processing electronics that is integrated to detector arrays in hybrid focal plane array technology [7]. In addition, its mechanical strength, the elimination of thermal strain issues, and its availability in large area wafers makes it a suitable substrate for the subsequent growth of HgCdTe [7,14,19,23,24]. The one main drawback with the direct growth of CdTe on Si is the 19% lattice mismatch between CdTe and Si. Consequently, in order to grow low defect density HgCdTe, the selective growth approach of CdTe has been proposed as a possible solution to reduce dislocation densities greater than  $2 \times 10^6 \text{ cm}^{-2}$ . In previous studies by Bhat *et. al.*[7,16], selective growth of CdTe on GaAs and CdTe/Si substrates using Metalorganic Vapor Phase Epitaxy (MOVPE) and Molecular Beam Epitaxy (MBE) has been achieved using different mask materials. High quality CdTe growth also



depends on the orientation of the windows patterned on the substrates [7]. As a result, CdTe/Si substrates are an alternative substrate for HgCdTe if strain due to lattice mismatch can be reduced via selective or NHE growth.

### **1.3. CONTRIBUTION OF THIS DISSERTATION**

#### **1.3.1. Role of selective nano-heteroepitaxy (NHE) technique to reduce interfacial strain due to lattice mismatch**

In this dissertation, a new approach is proposed to grow selective CdTe on patterned Si(111), and Si(211) substrates using the nano-heteroepitaxial (NHE) technique for the subsequent growth of HgCdTe, a technique used to reduce the defects at the CdTe and Si interface. The Si substrates are patterned using the optical lithography method and dry etching is used to create Si pillars at the micron and nano-scale. The goal of the selective CdTe growth is to deposit a single crystal CdTe grain on top of each Si pillar using the closed-space sublimation (CSS) technique. Selective growth is successful for a variety of source and substrate temperatures and deposition times for the first time on Si(111) and Si(211) substrates without the use of a mask. The structural quality of the CdTe grains and the CdTe/Si interface is the focus of this study, and was investigated for both Si(111) and Si(211) substrates using transmission electron microscopy (TEM).

#### **1.3.2. TEM and SEM comparison of CdTe growth on Si(111) and Si(211) Substrates**

The scanning electron microscopy (SEM) characterization method is used to analyze the film morphology of selective CdTe growth for Si(111) and Si(211) substrate orientations. The transmission electron microscopy (TEM) characterization method is used to analyze the structure quality of the single CdTe grains, and the associated CdTe/Si interface for each orientation. Two TEM modes, high resolution transmission electron microscopy (HRTEM) and diffraction mode are used to quantify the

strain at the interface. The TEM samples are prepared using the focused-ion beam (FIB) process, which enables the selection of specific sample regions based on SEM results.

## **Chapter 2: Literature Review**

### **2.1. CdTe AS A SUBSTRATE FOR HgCdTe GROWTH**

#### **2.1.1. HgCdTe Infrared Detectors**

A semiconductor material operates as a radiation detector if it has a large bandgap and low carrier density to minimize current noise. In addition, the semiconductor material must have high carrier mobilities, a high atomic number, and a long carrier lifetime in order for the radiation detector to produce pulses with fast time and efficient stopping power of high energy radiation [25]. Based on these requirements, mercury cadmium telluride (HgCdTe) is the most commonly used semiconductor material for infrared (IR) detectors [15]. HgCdTe is used for infrared (IR) applications such as photoconductors, photodiodes, or metal-insulator-semiconductor (MIS) detectors [15]. The properties that make HgCdTe a perfect semiconductor material for IR radiation include [14]:

1. A direct bandgap material with radiation absorption between 0.7 and 25  $\mu\text{m}$ .
2. High absorption and optical coefficients
3. Low dielectric constant/index of refraction.
4. Low thermal coefficient of expansion.
5. Available for various lattice-matched substrates for epitaxial growth.
6. High mobility of electrons

#### **2.1.2. HgCdTe Epitaxial Growth Techniques**

The use of bulk HgCdTe to fabricate infrared detectors is not practical and processing results in non-uniform properties. Bulk growth was substituted with the growth of thin films in the 1990s. Deposition techniques such as liquid phase epitaxy (LPE), vapor phase epitaxy (VPE), metalorganic

chemical vapor deposition (MOCVD), and molecular beam epitaxy (MBE) have been used to grow thin films of HgCdTe [14,15]. Over the past decade, the MBE growth technique has been the most commonly used vapor phase deposition technique for the growth of HgCdTe, since this technique is able to modify material properties by adding dopants. Improvements in the growth process have resulted in a reduction of etch pit densities to the low  $10^6 \text{ cm}^{-2}$  [15]. Table 2.1 provides a comparison of the various epitaxial HgCdTe techniques.

Table 2.1: Comparison of epitaxial growth methods for HgCdTe thin films [15].

Temperature (°C)	Bulk			Liquid phase epitaxy		Vapour phase epitaxy	
	SSR	Travelling heater method					
			HCT melt	Te melt	Hg melt	Te melt	MOCVD
950	950	500	350–550	400–550	275–400	160–200	
Pressure (Torr)	150 000	150 000	760–8000	760–11400	760–8000	300–760	10 <sup>−3</sup> –10 <sup>−4</sup>
Growth rate (μm/hr)	250	250	80	30–60	5–60	2–10	1–5
Dimensions <i>w</i> (cm)	0.8–1.2 dia	0.8–1.2 dia	2.5 dia	5	5	7.5 dia	7.5 dia
<i>l</i> (cm)	–	–	–	6	5	4	4
<i>t</i> (cm)	15	15	15	0.0002–0.0030	0.0005–0.012	0.0005–0.001	0.0005–0.001
Dislocations (cm <sup>−2</sup> )	<10 <sup>5</sup>	–	<10 <sup>5</sup>	<10 <sup>5</sup>	<10 <sup>5</sup> –10 <sup>7</sup>	5×10 <sup>5</sup> –10 <sup>7</sup>	5×10 <sup>4</sup> –10 <sup>6</sup>
Purity (cm <sup>−3</sup> )	<5×10 <sup>14</sup>	<5×10 <sup>14</sup>	<5×10 <sup>14</sup>	<5×10 <sup>14</sup>	<5×10 <sup>14</sup>	<1×10 <sup>15</sup>	<1×10 <sup>15</sup>
n-Type doping (cm <sup>−3</sup> )	N/A	N/A	N/A	1×10 <sup>14</sup> –1×10 <sup>18</sup>	1×10 <sup>14</sup> –1×10 <sup>16</sup>	5×10 <sup>14</sup> –5×10 <sup>18</sup>	5×10 <sup>14</sup> –1×10 <sup>19</sup>
p-Type doping (cm <sup>−3</sup> )	N/A	N/A	N/A	1×10 <sup>15</sup> –1×10 <sup>18</sup>	1×10 <sup>15</sup> –5×10 <sup>16</sup>	3×10 <sup>15</sup> –5×10 <sup>17</sup>	1×10 <sup>16</sup> –5×10 <sup>18</sup>
X-ray rocking curve (arc sec)	–	–	20–60	<20	<20	50–90	20–30
Compositional uniformity (Δ <i>x</i> )	<0.002	<0.004	<0.005	<0.002	<0.002	±0.01–0.0005	±0.01–0.0006

### 2.1.3. HgCdTe Epitaxial Growth on Suitable Substrates

The quality of HgCdTe thin films depends on the substrate and on the mismatch between the lattice constants [15]. Figure 2.1 illustrates a comparison of the bandgap versus lattice constant for II-VI

alloy systems. A great advantage of the II-VI alloy systems is the narrow range of lattice constant variation from CdTe (6.48 Å) to HgCdTe (6.45 Å).

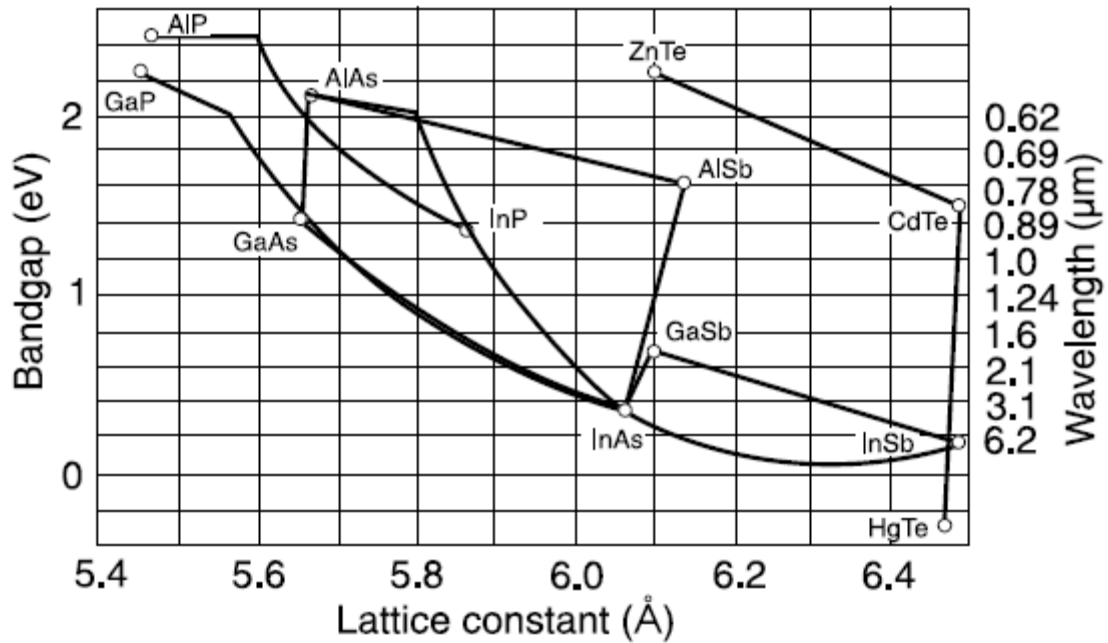


Figure 2.1. Bandgap vs. lattice constant for III – IV compounds [15].

### 2.1.3.1 HgCdTe Epitaxial Growth on CdZnTe Substrates

Large area substrates with transparency out to 30 μm make bulk CdTe a suitable substrate for the fabrication of HgCdTe thin films. However, there is a ~0.2% lattice mismatch between bulk CdTe LWIR and MWIR HgCdTe, which affects the film quality and device performance [14,15,29, 30]. It was found that this lattice mismatch can be reduced if a few percent (4%) of ZnTe is added to bulk CdTe substrates, producing a bulk CdZnTe substrate. However, CdZnTe substrates are not available in large sizes, and have high thermal expansions mismatch between the detector and the read-out circuit (ROIC), which results in etch pit densities (EPD) in the mid  $10^4 \text{ cm}^{-2}$  [15,16,31,32].

### ***2.1.3.2 HgCdTe Epitaxial Growth on Si Substrates***

The planar growth of CdTe films on Si substrates are currently being used as substrates for thin film HgCdTe infrared detectors. SWIR and MWIR detectors on Si have comparable performance to those fabricated on CdZnTe. The epitaxial growth of HgCdTe on Si(100) and Si(211) substrates is beneficial for the fabrication of silicon-based integrated circuits for HgCdTe [14,15,16,18,20,24,25,30,31,36]. It is believed that HgCdTe infrared detectors and the signal processing electronics of the focal plane array can be combined on the same wafer when a high quality HgCdTe thin film is grown on Si [7]. The main problem to overcome is the lattice mismatch (19%) between the two materials, since results in a low quality CdTe/Si interface. Dislocation densities above  $10^5 \text{ cm}^{-2}$  range have been reported for CdTe films grown on Si substrates, which affect the detector's performance [34].

### ***2.1.3.3 HgCdTe Epitaxial Growth on ZnTe/Si Substrates***

The efforts to reduce the defects resulting from the growth of CdTe layers on Si using the molecular beam epitaxy (MBE) technique have been extensive [14,15,26,31,32,35,36]. In order to minimize the effect of the lattice mismatch between CdTe and Si (19%), a ZnTe buffer layer is usually deposited between CdTe and Si, since the lattice parameter of ZnTe is 6.103 Å, which is between the values for CdTe (6.48 Å) and Si (5.431 Å). The introduction of a ZnTe buffer layer is proven to reduce the lattice mismatch to 12%, and dislocation densities to as low as  $10^5/\text{cm}^2$  [30,36-39].

### **2.1.4 Defect Formation in CdTe/Si Substrates**

HgCdTe/CdTe/Si detectors designed to absorb in the LWIR region are greatly affected by the lattice and thermal mismatch, and the high threading dislocation density at the interface [40]. A study compares the lattice mismatch on the (111) planes of a CdTe/Si film to the thermal mismatch generated after a cool down process to room temperature. The results of this study indicate that the lattice

mismatch is the cause of dislocation formation in the film, which is modeled as the critical CdTe epilayer thickness as a function of mismatch [41],  $\epsilon$ , as follows:

$$h_c = \frac{0.45}{\epsilon^{3/2}} \text{ (nm)} \quad \text{Eq. 2.1}$$

where  $h_c$  is the critical CdTe epilayer thickness, and  $\epsilon$  is the mismatch. Table 2.2 summarizes the critical CdTe epilayer thickness ( $h_c$ ) above which dislocations will form spontaneously for several material systems, along with the mismatch formulas ( $\frac{\Delta L}{L}$ ), and percent lattice misfit. The thermal expansion coefficients ( $\alpha$ ) for Si and CdTe are constant values equal to  $2.6 \times 10^{-6} \text{ K}^{-1}$  and  $4.9 \times 10^{-6} \text{ K}^{-1}$ , respectively, for cool down temperatures ( $\Delta T$ ) of  $\sim 300 \text{ K}$  [42]. The CdTe and Si lattice constants are  $6.48 \text{ \AA}$  and  $5.43 \text{ \AA}$ , respectively. According to Table 2.2, the lattice mismatch should dominate in the formation of misfit dislocations in thin films ( $\sim 0.5 \text{ nm}$ ). For thicknesses less than the critical thickness ( $h_c$ ), growth can be achieved with fewer dislocations, although still bearing stress due to the interface [41]. Fahey reports that the lateral lattice mismatch dominates in the formation of dislocations for CdTe(111) grown on Si(111). For CdTe(211) grown on Si(211), the results are similar to the (111) orientation along the (111) surfaces of the stepped (211) surface, along with (100) surface planes. It is believed that the (100) planes will not introduce stress or strain into the CdTe film [43]. Therefore, as the film grows, the stress contribution due to the step edges will saturate without generating dislocations. However, the thermal stress will nucleate dislocations if the CdTe film is grown beyond  $8 \text{ }\mu\text{m}$  thickness. Therefore, a high quality film can be achieved for film thickness between  $6 - 8 \text{ }\mu\text{m}$  [44].

Table 2.2: Material mismatch of CdTe/Si involves lattice mismatch and thermal mismatch [44].

	<i>Formula</i> $\frac{\Delta L}{L}$	<i>Misfit</i>	<i>Critical Thickness</i>
<i>Bulk Lattices</i>	$\frac{a_{CdTe} - a_{Si}}{a_{Si}}$	19.3%	0.5 nm
<i>5 X 6 Misfit Array</i>	$\frac{5 \cdot a_{CdTe} - 6 \cdot a_{Si}}{6 \cdot a_{Si}}$	-0.55 %	110 nm
<i>Thermal</i>	$\frac{e^{a_{CdTe} \cdot \Delta T} - e^{a_{Si} \cdot \Delta T}}{e^{a_{Si} \cdot \Delta T}}$	-0.069%	24839 nm

## 2.2. NANO-HETEROEPITAXY (NHE) GROWTH TECHNIQUE

### 2.2.1. Reduction of Interfacial Strain using the NHE Technique

The nano-heteroepitaxy (NHE) technique is used to reduce the stress present at the interface between two lattice-mismatched materials, such as gallium nitride (GaN) and Si [18,45]. NHE growth consists of four different approaches to reduce defects, these include (1) substrate patterning, (2) epitaxial lateral overgrowth (ELO), (3) strain partitioning in thin compliant substrates, and (4) epitaxial necking [19]. The substrate patterning technique is applied to selective CdTe growth on silicon on insulator (SOI), Si(111) and Si(211) substrates using growth methods such as MBE and CSS [9,18,19,30,36], where dislocation densities are reported in the mid- $10^5 \text{ cm}^{-2}$  to mid- $10^6 \text{ cm}^{-2}$  [4]. The lateral epitaxial overgrowth technique is applied to the selective CdTe growth on  $\text{SiO}_2/\text{As}/\text{Si}(111)$  and CdTe/ZnTe/Si(111) substrates using MBE [17]. Strain partitioning in thin compliant substrates is reported on patterned SOI substrates using the MBE epitaxial growth technique [18,46,47] where similar strain is observed in selective and planar growth on SOI. Finally, the epitaxial necking approach is



reported on the selective Ge growth on patterned SiO<sub>2</sub>/Si substrates [48] where TEM results show stacking faults from the Ge/Si interface at the SiO<sub>2</sub> sidewall resulting in a perfect Ge surface on Si.

For CdTe on GaN substrates, a planar growth film with low dislocations is accomplished when CdTe seeding areas merge to form a planar film [18,49]. These seeding areas are small before merging and have a larger free surface area per volume with fewer dislocations compared to planar growth of CdTe on Si [40]. Furthermore, when the interface of a film is composed of an inert material and CdTe, the CdTe layer is expected to have less dislocations, since dislocations will tend to be attracted by the interface. This results from the bonding across the interface which propagates stress across the interface and leads to weak bonds at the interface [50]. For this reason, it is expected for small CdTe volumes on Si to have relatively lower threading dislocations within their small volumes when compared to large-area films of CdTe on Si.

### **2.2.2. Effect of Pattern Size on Quality of Selective Growth**

The NHE technique proposes the fabrication of three dimensional nanopillars with dimensions less than 100 nm in diameter and greater than 100 nm in height. When these pillars are fabricated at the nanoscale they can deform when grains are grown on top of these pillars. The deformation of these nanopillars is known as the compliant substrate effect [35]. Figure 2.2 (a) and (b) illustrates the concept of the conventional planar growth and nano-heteroepitaxy growth, respectively. For a planar growth film, only some of the mismatch stress is reduced, since the epilayer will only deform in the vertical direction. Therefore, the strain energy in the epilayer will increase as the thickness of the epilayer increases. In contrast, selective growth is able to reduce the overall strain, since the substrate and the epilayer will deform in the vertical and lateral directions [51]. The reduction of stress and strain generated at the interface is associated with the diameter of the nanopillars [52]. However, the implementation of this technique results in one challenge, which is the defect formation when a thin film

starts to form on top of the pillars. If the pillars are reduced to the nanoscale, the pillars will elastically deform, which will lead to a reduction of defects as a planar growth film begins to coalesce [51].

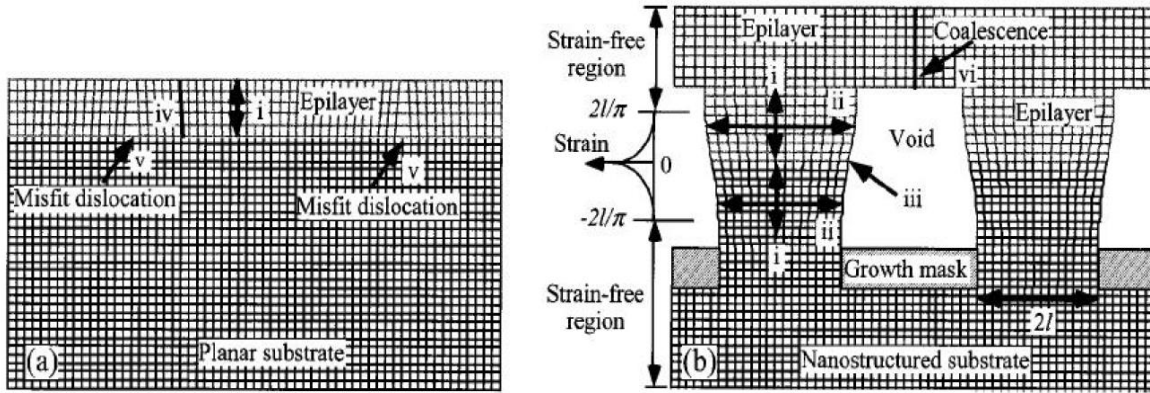


Figure 2.2. Schematic of (a) planar and (b) selective growth [51].

### 2.2.3. Parameters Affecting Selective Growth

#### 2.2.3.1 Selective CdTe Growth on Si and GaAs Substrates

Selective growth of CdTe has been performed on various patterned substrates, using epitaxial growth techniques such as MBE, MOVPE, and CSS, and the results of these studies are summarized in Table 2.3 [3,7,9,17,18,30,33,53].

Table 2.3: Summary of Selective CdTe Growth Results from the Literature [8].

Ref. No.	Substrate	Selective Deposition	Deposition Method	Mask	Type of Growth
29	CdS Si(100)	CdTe CdTe	CSS CSS	SiO <sub>2</sub> Si <sub>3</sub> N <sub>4</sub>	Selective Inverse Selectivity
28	CdTe(211)/Si	CdTe	CSS	Si <sub>3</sub> N <sub>4</sub>	Selective
27	CdS/ITO/Glass CdS/ITO/Glass	CdTe CdTe	CSS CSS	SiO <sub>2</sub> Si <sub>3</sub> N <sub>4</sub>	Selective Selective
24	Si GaAs(100) CdTe(211)B/Si	CdTe CdTe CdTe	MOVPE MOVPE MOVPE	SiO <sub>2</sub> SiN <sub>x</sub> SiN <sub>x</sub>	Inverse selectivity Selective Selective
26	As/Si(111) Si(111)	CdTe CdTe	MBE MBE	SiO <sub>2</sub> none (CdTe seed layer)	No Selectivity Selective
22	SOI(100)	CdTe	MBE	SiO <sub>2</sub>	Selective
23	CdTe/As/Si(211)	CdTe	MBE	As/Si(211)	Selective
25	Si(100) GaAs(100) Si(100)	CdTe CdTe CdTe	MOVPE MOVPE MOVPE	SiO <sub>2</sub> Si <sub>3</sub> N <sub>4</sub> CaF <sub>2</sub>	Inverse selectivity Selective Selective

The selective growth of MB is documented for, (1) Si(111) using a patterned CdTe seed layer and no mask layer, (2) Si(111) substrates using a SiO<sub>2</sub> mask layer [17], (3) silicon-on-insulator (100) substrates using the SiO<sub>2</sub> buried layer as a mask layer [18], and (4) CdTe/As/Si(211) substrates using an As/Si(211) mask layer [9]. The results presented in these studies demonstrate that selective growth of CdTe can be possible using either a mask layer or a CdTe seed layer prior to the selective growth. The MOVPE technique is associated with selective growth of CdTe on GaAs (100), CdTe(211)B/Si, and Si(100) substrates using SiN<sub>x</sub>, Si<sub>3</sub>N<sub>4</sub>, and CaF<sub>2</sub> mask layers, since it is believed that a high quality CdTe film can be achieved with the use of a proper mask and growth parameters [7,53]. In order to obtain a high quality film, high temperatures and low pressures are used. Therefore, high quality selective growth depends on the temperature and pressure, as well as the type of substrate and mask layer.

Selective CdTe growth is also possible using the CSS technique on (1) CdTe(211)/Si substrates with a Si<sub>3</sub>N<sub>4</sub> mask layer [30] for source and substrate temperatures of 530°C and 450°C, respectively, and (2) on CdS using a SiO<sub>2</sub> mask layer [54] for source and substrate temperatures of 550°C and 500°C, respectively. In contrast to the above studies, Diaz *et al.* achieved selective CdTe growth on micron patterned Si(100) substrates without the use of a mask layer using the CSS technique [3] for source temperatures ( $T_{\text{sou}}$ ) between 540°C - 570°C and a substrate temperature ( $T_{\text{sub}}$ ) of 450°C. In the latter, the system pressure was adjusted between 0.5-5 Torr to control the CdTe grain size. Several of the selective growth experiments are discussed in more detail in the next section (Section 2.2.3.2).

### ***2.2.3.2 Selective CdTe Growth on Si(100) via CSS***

Diaz, Quinones and Ferrer [3] report the growth of CdTe on patterned Si(100) substrates using the CSS technique without the use of a mask layer. The selective growth is achieved for a variety of source temperatures, deposition times and pattern sizes, with varying degrees of uniformity and structure quality. The highest quality selective CdTe growth is achieved for a source and substrate temperature of 550° and 450°, respectively. Selective growth is not possible for source temperatures above 550°C and substrate temperatures below 450°C. As the source temperature is increased above 550°C, the CdTe growth uniformity starts to diminish, and as the substrate temperature is decreased below 450°C, no selectivity is observed, since growth occurs on the pillars and in between the pillars. Figures 2.3(a) and 2.3(b) include scanning electron microscopy (STEM) and TEM micrographs, respectively, of selective CdTe growth on one micron Si(100) pillars. The cross-sectional micrograph in Fig. 2.3(a) illustrates the misorientation between the substrate and the film and a propensity of CdTe to grow twins along the  $\langle 111 \rangle$  direction[3]. Defects such as facets and stacking faults can be clearly seen in CdTe grains grown in these experiments and can be attributed to the lattice mismatch that exists between the Si substrate and the CdTe grains. Previous reports indicate that CdTe crystals may have a growth front that is not primarily perpendicular to the growth direction [55].

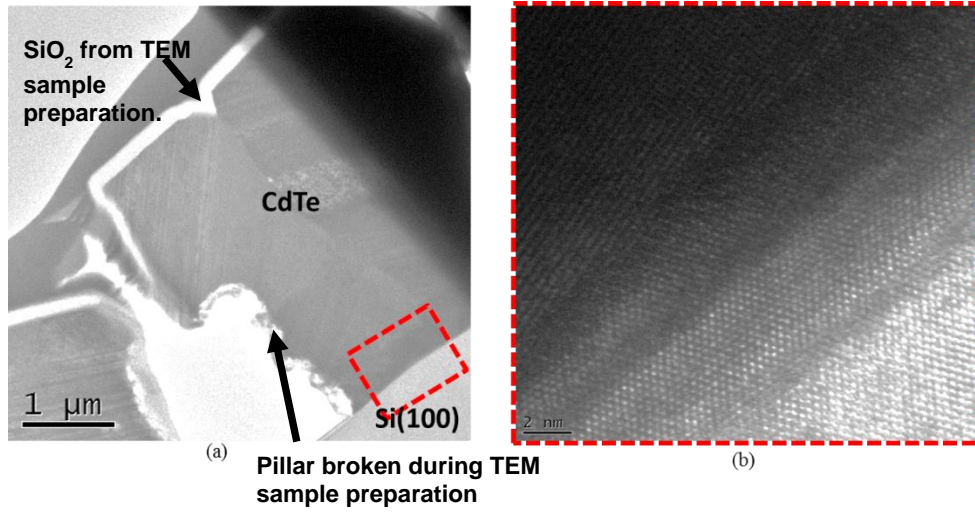


Figure 2.3. (a) SEM image of Selective CdTe growth on Si(100) and (b) TEM image of CdTe grain [3].

### 2.2.3.3 Selective CdTe Growth on Ge/Si(211) via MOVPE

S. Shintri et al.[5] explores a novel patterning technique to reduce defects in CdTe films grown on Ge/Si(211) substrates. A 60 nm layer of thermal SiO<sub>2</sub> is grown on a 3" Si(211) substrate which is patterned using molecular transfer lithography (M<sub>x</sub>L) to produce circular holes with a diameter of ~380 nm and a pitch of ~540 nm. A thin Ge layer is used to help with the lattice mismatch grading and to improve the quality of subsequent CdTe layer. One of the challenges in this study is to achieve the selective growth of both Ge and CdTe. Ge is first selectively grown inside the holes until the growth adjacent to the holes is close to merging. At the end of the Ge growth, As is grown on top of the Ge nanostructures to obtain the 'B' polarity of (211) CdTe. The quality of CdTe growth is characterized by X-Ray Diffraction (XRD), with FWHM of 2900 arcsec for selective growth compared to 472 arcsec for planar growth. Selective growth is achieved for temperatures higher than 500°C and for low pressures. Figure 2.4 (a) and (b) shows a SEM image of selective CdTe grown on Si(211) at 505°C and 520°C,

respectively. When the islands start to merge to form a thin layer, defects start to form at the junction of each grain. Shintri recommends an annealing process at the initial stages of the growth process.

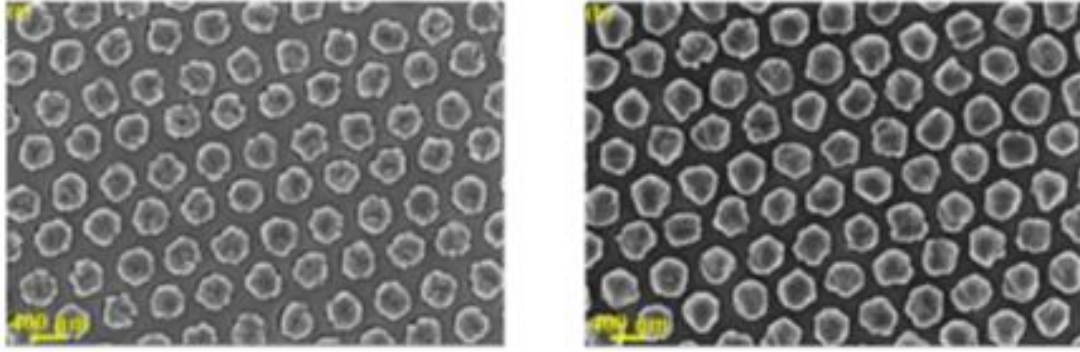


Figure 2.4. Selective growth of CdTe at (a) 505°C and (b) 520°C on Ge/Si(211) substrates [5].

#### ***2.2.3.4 Selective CdTe Growth on $\text{Si}_3\text{N}_4/\text{CdTe}/\text{Si}(211)$ Substrates via MOVPE***

Bhat et al. [6] reports a high quality (211)B CdTe film using the MOVPE technique with Everson etch pit densities (EPD) of  $3 \times 10^5 \text{ cm}^{-2}$ . The selective growth of CdTe is achieved using a  $\text{Si}_3\text{N}_4$  mask with windows 5  $\mu\text{m}$  in diameter. Selective growth was achieved for temperatures greater than 500°C and pressures lower than 25 Torr. The CdTe layers passed the  $\text{Si}_3\text{N}_4$  mask, the CdTe layers start to grow in the vertical and lateral direction on top of the  $\text{Si}_3\text{N}_4$  mask layer. Figure 2.5(a) and (b) shows SEM images of CdTe growth at 400°C and a pressure of 100 Torr, and at 500°C and 35 Torr, respectively. These temperature ranges correlate with selective CdTe growth achieved on patterned Ge/Si(211) substrates by S. Shintri et al.[5]. Furthermore, high quality CdTe growth results when it is grown on windows oriented in the  $[0\ 1\ \text{bar}1]$  direction and  $90^\circ$  to the  $[\text{bar}\ 1\ 1\ 1]$  direction. In this study, the quality of the CdTe films depends on the growth window orientation. If any misorientation is present between the stripes, defects will form when the merge. According to the results obtained by Bhat *et al.*, on the selective growth of CdTe on  $\text{Si}_3\text{N}_4/\text{Si}(211)$ , it is recommended that the substrate

patterning be reduced to the nanometer scale in order to reduce dislocations at the interface of adjoining grains.

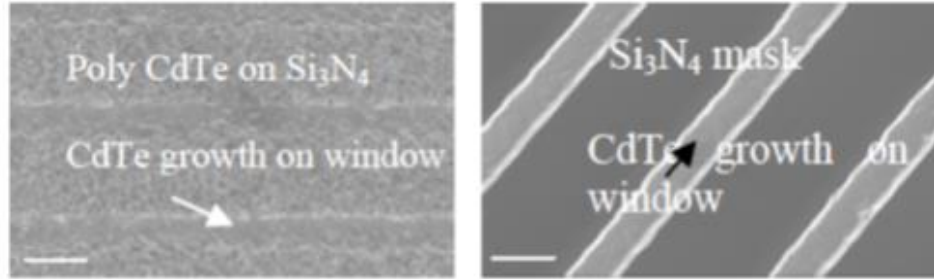


Figure 2.5. SEM images for selective CdTe growth on Si<sub>3</sub>N<sub>4</sub>/CdTe/Si(211) substrates at (a) 400°C and (b) at 500°C [6].

#### ***2.2.3.5 Selective CdTe Growth on CdTe/ZnTe/Si(211) Substrates via MBE***

S. Fahey et al.[8], achieved selective - area epitaxy and coalescence of CdTe grains on CdTe/ZnTe/Si(211) substrates with 0.5  $\mu\text{m}$ -pitch arrays exposed through a Si<sub>3</sub>N<sub>4</sub> mask using the molecular beam epitaxy (MBE) technique. First, a 250 nm CdTe layer is grown by MBE on a blanket Si substrate. The samples are then coated with Si<sub>3</sub>N<sub>4</sub> and patterned by ultraviolet interferometric lithography, resulting in windows 500 nm in diameter. CdTe is then selectively grown on the exposed CdTe using MBE. Figure 2.6 includes an SEM image of the best quality film achieved in this study from the center of the sample after 90 minutes of CdTe growth at a reactor temperature of 345°C. In particular, this study focuses on analyzing the merging of the CdTe window islands. A comparison is made between selective growth on patterned 0.5  $\mu\text{m}$ -pitch samples of CdTe/ZnTe/Si(211) to planar growth using the same growth parameters. The XRD FWHM values for the patterned samples are seven times greater than the unpatterned samples. For this reason, it is confirmed that the merging of the islands might reduce the film quality due to (1) the presence of dislocations on the surfaces of the islands, (2) the lateral to vertical growth is small, which results in a poor quality film, and (3) when the

islands have different orientations, they will likely generate dislocations upon merging. These results correlate with the selective CdTe growth on  $\text{Si}_3\text{N}_4/\text{CdTe}/\text{Si}(211)$  substrates by Bhat et al.[6]

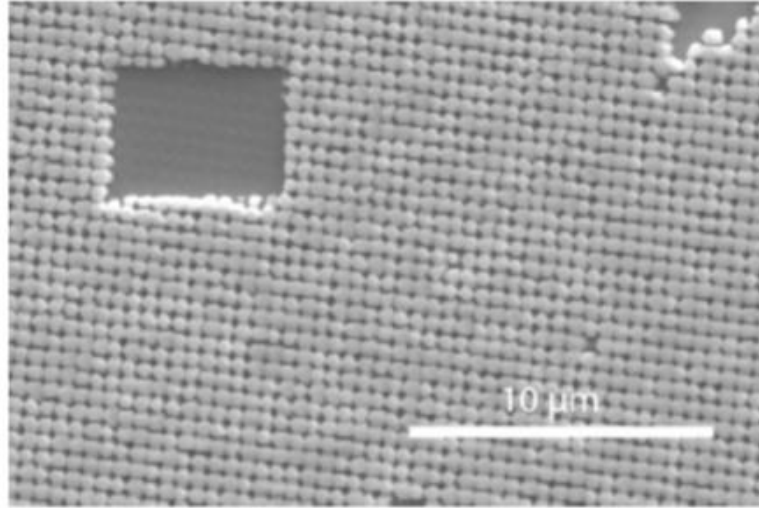


Figure 2.6. SEM image of selective CdTe growth on patterned ZnTe/Si(211) at 345°C for 90 minutes [8].

#### ***2.2.3.6 Selective CdTe Growth on CdTe/As/Si(211) Substrates via MBE.***

T. Seldrum et al.[9] achieved the selective CdTe growth on patterned CdTe/As/Si(211) substrates using the molecular beam epitaxy (MBE) technique. In this study a mechanism based on a difference in the physisorption energy is proposed in order to explain selectivity between Si and CdTe. First, the Si substrates are passivated with arsenic (As), which prevents nucleation of contaminants on Si [56]. Second, a 2 μm CdTe nucleation layer is grown on Si(211) substrates with a reactor temperature of 310°C for 2 minutes, annealed at 460°C for 10 minutes, with a last stage growth at 380°C for 2 hours. The CdTe/As/Si(211) substrates are then patterned using the optical lithography technique resulting in CdTe islands or pillars with diameters in the range of 80 – 320 μm with a height of 0.8 μm separated by Si. A preliminary planar CdTe growth study on Si(211) demonstrates that CdTe does not grow on As



passivates surfaces at temperatures above 385°C. When a selective growth study was conducted at 400°C reactor temperature at a pressure of  $5 \times 10^7$  Torr for 2 hours, growth is observed only on CdTe. Selective growth of CdTe is achieved because the substrate temperature is high enough (400°C) in order for CdTe to nucleate only on the CdTe surface and not on the Si surface. The results from the physisorption energy analysis indicate that the growth rate on Si(211) substrates changes from 1.4 nm/s at 385°C to 0.2 nm/s at 400°C. Furthermore, the growth is possible because the physisorption energy is slightly smaller on Si than on CdTe. If CdTe growth is prolonged, CdTe will eventually nucleate at defects or impurities on the Si surface.

#### 2.2.4. Comparisons of Planar to Selective Growth

Fahey [8,40], studied the selective and planar CdTe growth of Si(211) substrates using the MBE technique. Planar substrates consist of a ~250 nm single crystal film of CdTe on Si(211) with a ~15 nm thick ZnTe buffer layer, and patterned substrates with a similar layered structure using a ~40 nm Si<sub>3</sub>N<sub>4</sub> mask. Planar and selective growth of CdTe is achieved for substrate temperatures equal to or greater than 320°C. X-Ray Diffraction (XRD) characterization analysis is used to analyze the quality of the patterned and unpatterned samples using the full-width half-maximum (FWHM) values to calculate the dislocation densities. The FWHM results obtained from the XRD analysis are 1650 arcsec for a patterned 9.4 µm thick layer and 238 arcsec for an unpatterned 10 µm layer [8,40]. The calculated dislocation density for both samples is calculated using the FWHM values obtained in this study using the following equation:

$$N \approx \frac{F^2}{9 \cdot b^2} \quad \text{Eq. 2.2}$$

Where  $F$  is the FWHM value, and  $b$  is the magnitude of the dislocation burgers vector for CdTe (0.458 nm) [17,36]. This results in a dislocation density of  $3.4 \times 10^9 \text{ cm}^{-2}$  for the patterned samples and  $7.0 \times$

$10^7 \text{ cm}^{-2}$  for the unpatterned samples. According to the XRD analysis of these samples, the crystalline quality of the patterned samples is significantly lower compared the unpatterned samples.

Bhat *et al.*[6] also examined the planar and selective growth of CdTe on ZnTe/Si(211) substrates using the MOVPE technique. Planar growth consists of a thin ( $\sim 300 \text{ nm}$ ) Ge layer grown at  $525^\circ\text{C}$ , follow by a thin ( $\sim 200 \text{ nm}$ ) ZnTe layer grown at  $350^\circ\text{C}$ . The patterned substrates consist of  $2 \text{ }\mu\text{m}$  windows in diameter and pitch of  $38 \text{ }\mu\text{m}$ . In order to calculate the dislocation density in  $12 \text{ }\mu\text{m}$  thick layers, the Everson etch process was performed for 30 seconds. He reports the best planar CdTe growth on Si(211) which resulted in a FWHM value of 64 arcsec and Everson etch pit density (EPD) of  $3 \times 10^5 \text{ cm}^{-2}$  [6]. In this case, the rocking-curve FWHM increased from 64 arcsec for the planar CdTe growth to 184 arcsec for the selective CdTe growth, indicating no improvement in crystal quality. Consequently, it is once again recommended to decrease the pattern size to the nanoscale in order minimize interfacial strain.

## **2.3. STRUCTURE ANALYSIS OF SELECTIVE AND PLANAR CdTe GROWTH**

### **2.3.1. Interface Studies of Planar CdTe Growth**

Large area planar films of single crystalline CdTe on Si have proven to be useful as alternative substrates to bulk CdZnTe for HgCdTe infrared detectors and have been designed to absorb in the long-wavelength infrared (LWIR). However, the main drawback of Si substrates is the high lattice and thermal mismatch between CdTe and Si, which results in an increase of dislocations at the CdTe/Si interface [41,60,61]. According to the latest research, high quality HgCdTe layers grown by MBE are possible using substrates consisting of CdTe films grown on Si(211) substrates [62].

### ***2.3.1.1. Planar CdTe Growth on ZnTe/Si(211) Substrates via TEM***

In 1996, A. Million *et al.* reported the epitaxial growth of CdTe on ZnTe/Si(211) substrates using the MBE technique [63]. The first step in the fabrication process is to desorb the passivated hydrogen by heating the Si substrate at 540°C. During the desorption process, the substrate is treated with arsenic (As) in order to maintain the Si bonds together and prevent a polycrystalline CdTe film. Second, a 60 nm ZnTe buffer layer is grown at 250°C in order to reduce the lattice mismatch between Si and CdTe to ~12.3%. Multiple CdTe layers are grown, each with a one minute annealing cycle at 370°C between each grown CdTe layer in order to reduce misfit dislocations. A FWHM value of 156 arcsec is observed for a 4.4 µm layer CdTe film, and a FWHM value of 196 arcsec for an 8 µm layer. The dislocation density at the surface is  $5 \times 10^6 \text{ cm}^{-2}$  for the best samples. It is also noted that the crystal quality decreases when CdTe layers are grown with an improper growth step or annealing temperature, since high FWHM values greater than 200 arcsec are reported.

Similar results are shown by T.J. De Lyon *et al.*, where he reports the planar CdTe growth on ZnTe/Si(112) substrates by MBE [64]. For an 8 µm thick film, x-ray rocking curves FWHM of 72 arcsec are reported for the CdTe (224) reflection with corresponding etch pit densities (EPD) of  $2 \times 10^6 \text{ cm}^{-2}$ . Etch pit density measurements show that as the epilayer thickness increases up to 5 µm, threading dislocations decrease away from the interface. Threading dislocations decrease as the epilayer thickness increases to approximately 5 µm, and saturate at  $2 \times 10^6 \text{ cm}^{-2}$  for layers above 5 µm [64]. In addition, S. Rujirawat *et al.* report the planar growth of CdTe(211)B/ZnTe/Si(211) by MBE, where he analyzes the microstructure at the interface between ZnTe and Si(211) [65]. According to these results, the lattice mismatch (12%) between ZnTe and Si causes twin formation. Therefore, the orientation of the CdTe layers will be determined by the ZnTe orientation. It was also noticed from the experiments performed in Rujirawat's study that the ZnTe orientation depends on the Si substrate temperature during the ZnTe

growth. Furthermore, the highest quality CdTe films are for ZnTe growth at 220°C, annealing at 380°C, and subsequent CdTe growth at 300°C.

Zhao[66] reports the structural analysis of CdTe(211)B layers grown on ZnTe/Si(211) substrates with MBE. The first step in the fabrication process is to desorb and passivate the oxide layer with an As flux on the Si(211) substrates. Then, a ZnTe layer is grown at approximately 300°C, followed by 60 cycles of annealing at 450°C. During the CdTe growth, 10 annealing cycles at 560°C are performed in order to reduce dislocations [41]. Figure 2.7 is a high resolution TEM image showing structural defects generated at the ZnTe/Si(211) interface and ending 50 nm above the interface. The structural defects identified were (111) stacking faults. The associated diffraction pattern (inset) illustrates a misorientation angle of 3.5 ° between Si and CdTe.

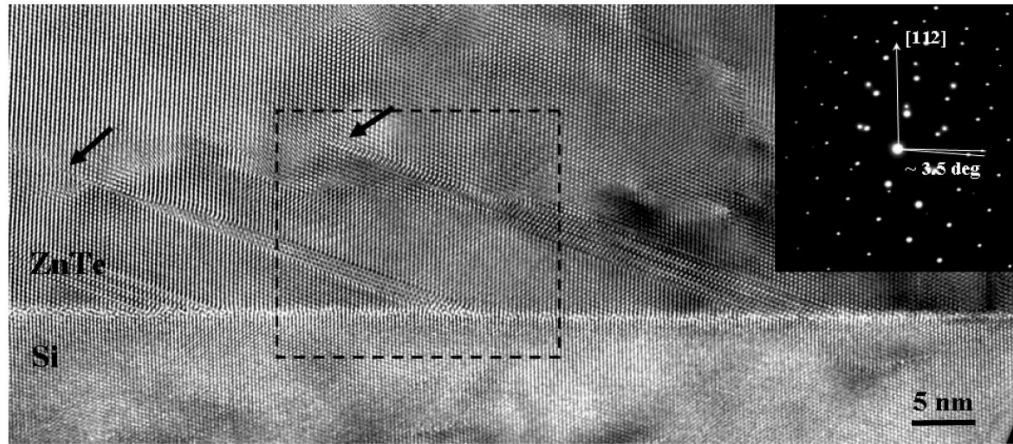


Figure 2.7. High resolution TEM image and diffraction pattern of ZnTe/Si(211) interface [66].

### 2.3.2. Interface Studies of Selective CdTe Grain Growth via TEM

Many efforts have been tested and proposed to control and reduce the dislocation density at the CdTe/Si interface including (1) in-situ and ex-situ annealing, (2) introduction of buffer layers, and (3) selective growth on patterned substrates.

### 2.3.2.1. Selective CdTe Growth on nanopatterned Ge/Si(211) Substrates

Stacking faults are observed in CdTe grains, as well as, at the CdTe/Si interface. Some of the defects created due to the lattice mismatch are being annihilated at the mask surface, as identified in Fig. 2.8 as F1 and F2 [4]. The generation of additional defects occurs when adjacent grains merge to form a single layer. The nucleation around defects or impurities may also play a significant role in the generation of additional defects. S. Shintri et al.[5] and S. Fahey et al.[8], demonstrate that the patterned growth can produce lower crystalline quality compared to planar growth, and both report that additional defects are created when individual grains from selective area growth merge as they form the planar layer [5,8].

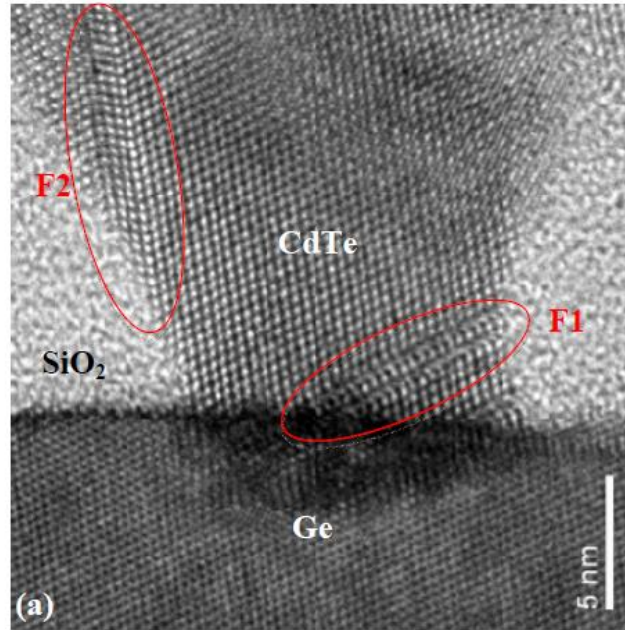


Figure 2.8. High resolution TEM image of CdTe/Ge interface illustrating the annihilation of defects at mask walls [4].

Bhat et al.[6] and S. Fahey et al.[8] recommend a reduction in the substrate pattern to less than 500 nm in order to decrease the dislocation density. Fahey et al. indicates that in order to reduce the diffusion of defects from the interface to the epilayer, a barrier provided by the mask wall will reduce

the diffusion of these defects to the epilayer surface. Therefore, when HgCdTe layers are grown on coalesced CdTe structures, dislocations confined to the merged island areas will not affect the HgCdTe layers [8,57,58].

#### ***2.3.2.2. Selective CdTe Growth on patterned Si(100) Substrates***

Diaz *et al.*[3] reports on the analysis of the structure quality for selective CdTe growth on Si(100) substrates (Sample NPR-2) without the use of a mask layer using a TECNAI TF20 transmission electron microscope (TEM). Cross-sectional TEM specimens are prepared by a two-step process using a semiautomatic dicing saw and focused ion-beam (FIB) milling instrument. Figures 2.9 and 2.10 show cross-sectional TEM micrographs of a CdTe/Si(100) sample (NPR-2) grown at source and substrate temperatures of 530°C and 450°C, respectively, system pressure of 5 Torr, and deposition time of 15 minutes. Two individual grains are considered for this analysis, grains A (Fig. 2.9a-c) and B (Fig. 2.9d-f). Grains A and B consist of two subgrains, with misorientation angles of 35° and 32°, respectively. Twins are also present in both grains, and are highly visible in grain B (Fig. 2.9f). The interface between grain A and the Si(100) substrate is highlighted in Fig. 2.10, illustrating the evolving misorientation between the substrate and the film. In this study, examination of the CdTe/Si(100) region by high-resolution transmission electron microscopy (HRTEM) exhibits a smooth interface free of Si native oxide. Nevertheless, defects such as facets and stacking faults can be clearly seen in the CdTe grains and can be attributed to the lattice mismatch that exists between the substrate and the grains. Previous reports indicate that CdTe crystals may grow in a direction that might not be perpendicular to the substrate surface [59]. This study demonstrates that it maybe possible to grow high quality CdTe growth using the CSS method, and that other Si substrate orientations should be examined, as well as selective growth at the nanoscale.

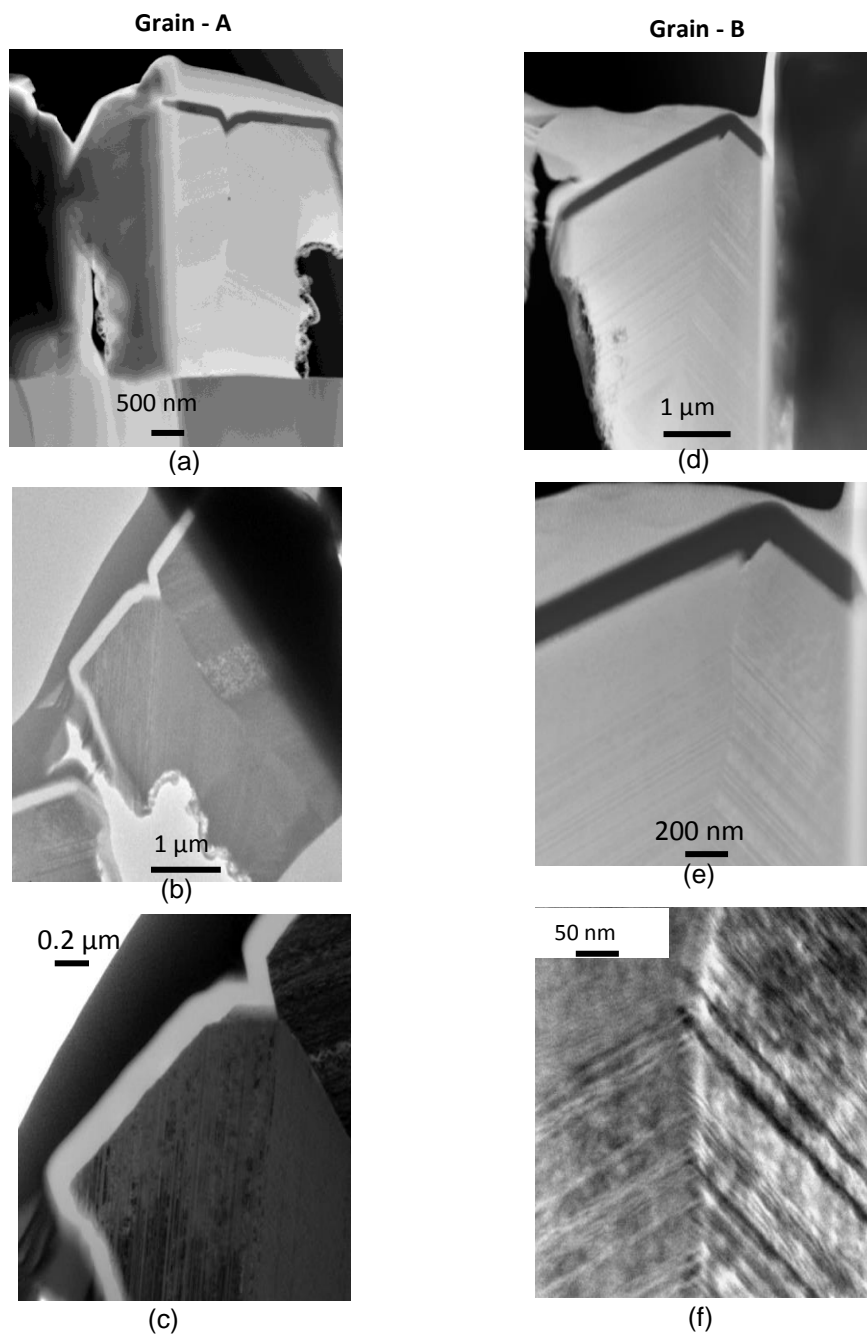


Figure 2.9. TEM images of grain A (a-c) and grain B (d-f) from sample NPR-2 [3].

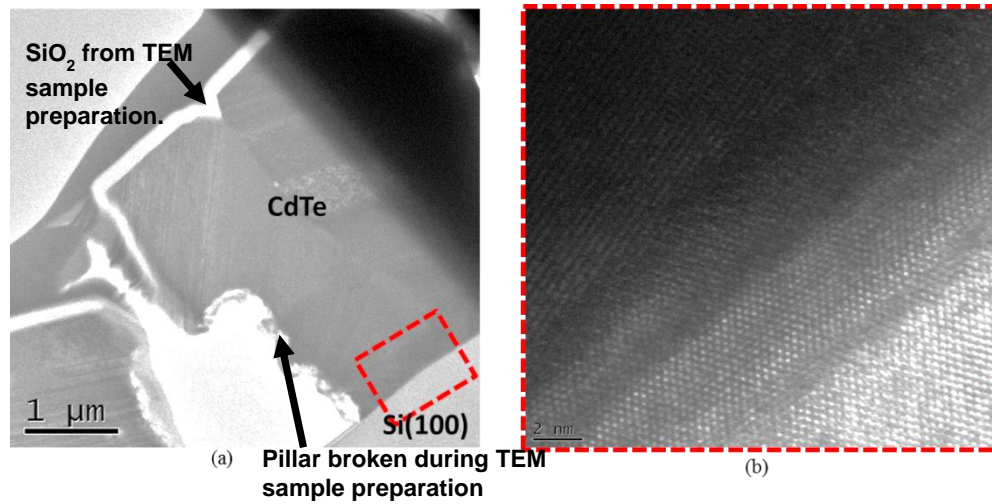


Figure 2.10. High-magnification TEM images for grain A for sample NPR-2 [3].

### 2.3.3. Interface Studies of Selective CdTe Growth via XRD

S. Fahey *et al.* [8] examined the selective-area epitaxy of CdTe on ZnTe/Si(211) substrates using a smaller pattern, where substrates are patterned with 0.5  $\mu\text{m}$ -pitch arrays of holes on a silicon nitride layer. Selective CdTe growth is performed for source temperatures between 320°C to 350°C and short annealing steps at 370°C using the MBE. The results from this study are compared to unpatterned samples using X-Ray diffraction (XRD) characterization. The XRD rocking curve for a 4.5  $\mu\text{m}$  film on a patterned sample resulted in a CdTe (422) FWHM of 1047 arcsec. For unpatterned substrates with a film thickness of 5  $\mu\text{m}$ , the corresponding FWHM was 152 arcsec. The dislocation density for the patterned and unpatterned films is calculated using the FWHM values, resulting in  $1.4 \times 10^9 \text{ cm}^{-2}$  and  $2.9 \times 10^7 \text{ cm}^{-2}$ , respectively. The merging of the islands may be the cause of the increase in the FWHM value for selective CdTe films compared to the planar growth films. The work in this dissertation can be viewed as an effort to improve upon these results by proposing a new approach for high quality selective CdTe growth on patterned Si substrates without the use of a mask layer.



## 2.4. THERMODYNAMICS OF CdTe GROWTH IN THE CSS REACTOR

### 2.4.1. CdTe Properties in the CSS Reactor

Cadmium telluride is an excellent semiconductor material due to its high effective atomic number (50), high absorption capacity, and radiation resistance infrared (IR) detector applications. Table 2.4 summarizes the basic properties of CdTe in comparison with other materials used as substrates for HgCdTe growth [20]. However, CdTe is one of the most challenging materials to manufacture with preset and reproducible properties [20,69].

Table 2.4: Comparison of Relevant Characteristics of Materials used as substrates for HgCdTe [24].

	Materials				
	CdTe	(Cd,Zn) Te4% Zn	Al <sub>2</sub> O <sub>3</sub>	GaAs	Silicon
Melting Point (°C)	1092	1088	—	1237	1412
Thermal Conductivity (mWcm <sup>-1</sup> K <sup>-1</sup> )	55	55	419	500	1235
Vickers Hardness at 300K (kg mm <sup>-2</sup> )	40	60	2500–3000	360	1150–1330
Lattice Constant (Å)	6.482	6.466	—	5.6532	5.4307
Structure	zincblende	zincblende	hexagonal	zincblende	diamond
Etch Pit Density (cm <sup>-2</sup> )	10 <sup>5</sup>	10 <sup>4</sup>	4 × 10 <sup>3</sup>	10 <sup>3</sup>	0
Rocking Curve Width (arc-s)	60	20	<60	14	7
Thermal Expansion Coefficient (10 <sup>-6</sup> K <sup>-1</sup> )	5.31	—	5.0	6.7	2.6
Available Sizes (diam in)	2	2	2,3	2,3	5

There are obstacles for obtaining high quality CdTe growth, such as (1) the low CdTe thermal conductivity which makes it difficult to control the solid-liquid interface, and (2) due to the high ionicity of the Cd-Te bond, the structure that forms near the CdTe melting point can be either hexagonal or cubic, which forms twins [70]. For this reason, the Cd vapor pressure must be controlled in order to maintain CdTe stoichiometry and avoid the presence of Te precipitates.

### 2.4.2. CdTe Growth using Close-Spaced Sublimation

The close-spaced sublimation (CSS) technique is used for the epitaxial growth of CdTe, since this system is able to control the structural properties of the CdTe material by varying the source and substrate temperatures, deposition time, and gas pressures of the system. Figure 2.11 illustrates the

CdTe phase diagram as a function of Te concentration, showing that above 1000°C, stoichiometric CdTe (50% Cd, 50% Te), is the most stable phase for CdTe. This means that as the CdTe deposits it should maintain stoichiometric growth. Moreover, Cd and Te have very similar atomic masses which also support the stoichiometric growth. As a result, the vapor pressure above CdTe will contain very nearly equal parts of Cd and Te [71]. As Te sublimates from the CdTe source, it forms dimers,  $\text{Te}_2$ , and in order for the total number of Cd and Te atoms to remain the same in this vapor, the  $\text{Te}_2$  pressure must be half of the Cd pressure. In order for deposition to occur, the CdTe source temperatures must be kept at higher temperatures than the substrate [71].

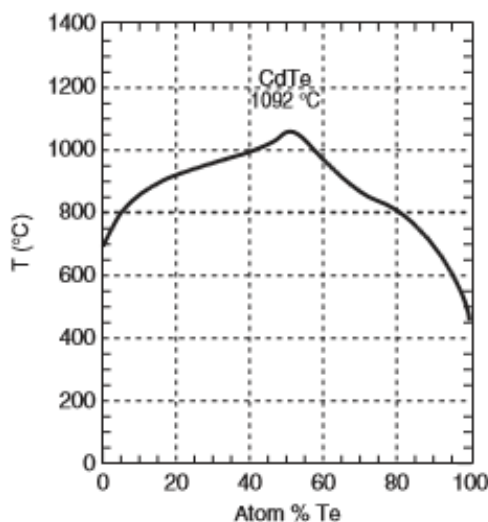


Figure 2.11. CdTe Phase Diagram [35,37,72].

The CSS technique is used for the deposition of CdTe on Si substrates in order to achieve direct growth from the source to the substrate. The mean free path of the Cd atoms or  $\text{Te}_2$  must be approximately the same as the spacing between the source and the substrate [72]. Therefore, the system pressure must be adjusted to maintain a mean free path on the order of the source to substrate spacing.

### **2.4.2. Critical Planar and Selective Growth Parameters**

Previous studies at the University of Texas at El Paso (UTEP) result in three observations associated with the epitaxial growth of CdTe using the CSS, (1) significant amounts of CdTe deposit on the contours of the CSS reactor liner, (2) different source orientations result in different sublimation rates, and (3) sublimation depends on atomic density, bonding density, and bond strength [71,73]. These observations are validated based on planar growth of CdTe on a 0.9 mm thick plain soda line glass substrate using a powder source. Successful growth can be achieved for deposition temperatures from 400° to 600°C, chamber pressures from  $10^{-2}$  to 5 Torr, and substrate to source distances range from 0.87 mm to 1mm. Four CSS parameters need to be taken into consideration in order to produce a high quality planar CdTe film. These include (1) high source temperatures, (2) high temperature differences between the source and the substrate of approximately 100°C, (3) low pressures (< 5 Torr), and (4) the distance between the source and the substrate (~1 mm) [71]. The experiments presented in this dissertation apply the four CSS parameters mentioned above for the selective CdTe growth on Si substrates [3,54,55].

### **2.4.3. CdTe CSS Growth Models**

As mentioned above, and also demonstrated by Cruz-Campa, Colegrove, Anthony, Alamri, and Schumm [13,71-74 ,83], the CdTe growth rate depends on several CSS parameters including the source and substrate temperature, the distance between the source and the substrate, the pressure of the system, and the interaction of the gas molecules in the chamber. As a result, the CSS can be operated under the diffusion limited or the sublimation limited models [7-72,74,83].

#### ***2.4.3.1. Diffusion-Limited Model***

The first model, diffusion-limited, is when the film growth is controlled by two system parameters, (1) the pressure and (2) the separation distance between the source and the substrate. Since

the pressure of the ambient gas is controlled by the substrate and source temperatures, this results in sublimation of CdTe stoichiometrically [4,9,28,52,71,73]. The separation between the source and substrate is the growth driving force based on the system pressure, since Cd atoms and Te<sub>2</sub> molecules collide with the gas molecules before they condense on the substrate. Therefore, the deposition rate is the inverse function of the gas pressure and proportional to the exponential factor which can be express as follows:

$$e^{-E_a/kT_{so}} \quad \text{Eq. 2.3}$$

where  $E_a$  the activation energy, and k is Boltzmann's constant, and T is temperature in Kelvin [83]. According to this model, when the distance between the source and the substrate is decreased, the growth rate increases, due to fewer collisions. If the pressure is increased, the number of interactions increases, and the growth rate decreases. When the pressure is greater than 1 Torr, the distance between the source and the substrate is longer than the mean free path. If this is the case then the growth is diffusion-limited.

#### 2.4.3.2. Sublimation-Limited Model

In the sublimation-limited model, it is assumed that there are no collisions as the Cd atoms and Te<sub>2</sub> molecules migrate from the source to the substrate. The sublimation-limited model is based on studies done by Hertz *et al.*, which states that the sublimation rate is control by the system temperature [71]. Therefore, if all atoms condense on the substrate, the net mass transport rate is given by:

$$GR_{subl} (m/s) = \frac{\alpha\beta (P_{sou}^i T_{sou} - P_{sub}^i T_{sub}) N_A}{\sqrt{\pi m_i R T_{av}}} \left( \frac{m_i}{\rho_i} \right) \quad \text{Eq. 2.4}$$

where  $\alpha$  and  $\beta$  are coefficients with values between 0 and 1;  $P_{sou}^i$  and  $P_{sub}^i$  are the vapor pressure (Pa) of the material evaporated at the source and substrate, respectively,  $m_i$  is the molar mass of CdTe (kg/mol);  $R$  is the universal gas constant (J/(kg mol));  $T_{sou}$  and  $T_{sub}$  are the source and substrate temperatures (K), respectively,  $T_{av}$  is the average temperature (K);  $N_A$  is Avogadro's number; and  $\rho_i$  is the density of the substance evaporated (kg/m<sup>3</sup>) [72]. The deposition rate increases as a function of source temperature, since the pressure is assumed to be sufficiently low so that there are few interactions with background gas molecules [72]. This model is valid for temperature ranges between 400°C to 600°C, pressures from 10<sup>-2</sup> to 760 Torr, and source/substrate separation distances between 0.8 mm. and 1mm. The sublimation-limited model is valid for pressures around 10<sup>-5</sup> Torr, since at this pressure the distance between the substrate and the source is equal or smaller than the mean free path. The experiments performed in this dissertation are in line with the diffusion-limited model mentioned above, since the CdTe growth conditions consist of system pressures in the range of 0.1 to 5.0 Torr. In conclusion, the source temperature and source/substrate separation control the growth rate since the pressure is high enough for the growth to be diffusion-limited. However, the quality of CdTe growth is highly influenced by the substrate temperature [1].

### Chapter 3: Experimental Procedure

The nanoheteroepitaxy technique is proposed in order to improve the selective growth of CdTe on patterned Si(111) and Si(211) substrates without a buffer layer. This research focuses on improving the quality of CdTe growth on Si and the resulting CdTe/Si interface, for the subsequent growth of HgCdTe for infrared detector applications. This work proposes to use the close-space sublimation (CSS) technique to characterize the selective growth of CdTe on Si(111) and Si(211) substrates.

According to the literature, the quality of CdTe growth on Si substrates can be improved by growing on the (211) orientation [3,5,6,25]. The (211) orientation is expected to result in superior CdTe growth, since HgCdTe likes to grow on (211)CdTe layers, which leads to the reduction of dislocations on HgCdTe layers [14-16,18,20,24,25,30,31,36]. When the nanoheteroepitaxy (NHE) technique is applied, there is a theoretical reduction of defects at the interface as a result of the strain reduced between the patterned substrate and the epilayer, which also leads to a reduction of defects in the planar film which results when selective growth merges [18,19,45]

The growth parameters examined as part of this study include the source and substrate temperatures, the reactor pressure (0.1 Torr – 5 Torr), the pattern size (500 nm – 1  $\mu$ m), and the substrate orientation (111 and 211). High quality samples and selective growth is confirmed using the scanning electron microscope (SEM). The quality of the CdTe film and the CdTe/Si interface is examined for high quality samples for each of the substrate orientations using two different TEM modes, high resolution transmission electron microscopy (HRTEM) and diffraction modes.

CdTe/Si films are fabricated by creating an array of 2  $\mu$ m posts with a 2  $\mu$ m pitch on the Si substrate surface using the photolithography method. The photoresist is etched using a dry etching process in an Oxford PlasmaLab. The CSS reactor is used to selectively grow CdTe grains on top of each Si pillar. The detail fabrication process used in this study is explained in this section.

### 3.1. PHOTOLITHOGRAPHY METHOD

A photolithography process consist of transferring a geometric pattern from a photomask to a substrate using ultraviolet light and a light sensitive organic material called photoresist. The photoresist is a photosensitive chemical containing a photoactive compound (PAC), a matrix or resin material, and a solvent. The PAC changes the solubility of the resin only in regions where it is exposed to UV light, the resin is a polymer, and the solvent is used to dissolve and adjust the viscosity of photoresist. One main characteristic of the photoresist is that the photosensitive chemical can change its properties by a UV light exposure and heat treatment. Two types of photoresist can be used in a photolithography process; negative and positive (Figure 3.1). When positive photoresist areas are exposed to UV light, these areas turn out to be soluble to the developer solution. The negative photoresist work the opposite of the positive photoresist, since the photoresist areas exposed to UV light will be in soluble to the developer solution, whereas the unexposed areas will turn out to be soluble to the photoresist. Both, the positive and negative photoresist processes are illustrated in Figure 3.1.

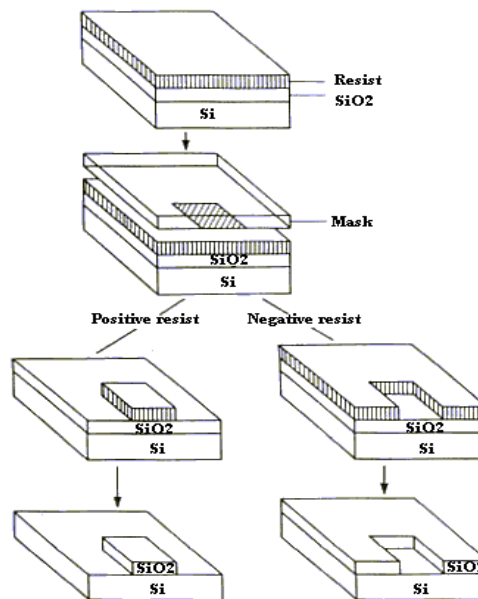


Figure 3.1. Comparison of positive and negative photoresist [75].

The patterning of the Si substrates in this study is accomplished by using a positive photoresist (AZ5214). However, one of the goals of this study is to produce patterned substrates that consist of Si pillars, which can normally be achieved using negative photoresist. Since positive photoresist is used in these experiments, an image reversal process is applied to the positive photoresist, which then works as a high resolution negative photoresist. This is accomplished using two UV light exposures and one heat treatment. The first exposure makes the exposed areas more soluble as a result of the PAC, and a reaction prepares the resist with a cross-linking agent that can be activated at temperatures above 110°C. The hard bake at 110°C activates the cross-linking agent, which neutralizes the PAC, and makes it more insensitive to further radiation and insoluble to the developer solution. The PAC in the unexposed areas is still active, and removing the mask and performing a flood UV exposure makes these areas soluble to the developer solution. As a result, the areas associated with the first exposure remain on the substrate and, a negative/opposite image is achieved. Figure 3.2 is a summary of the process for the image reversal lithography process explained further in sections 3.1.1 – 3.1.6.

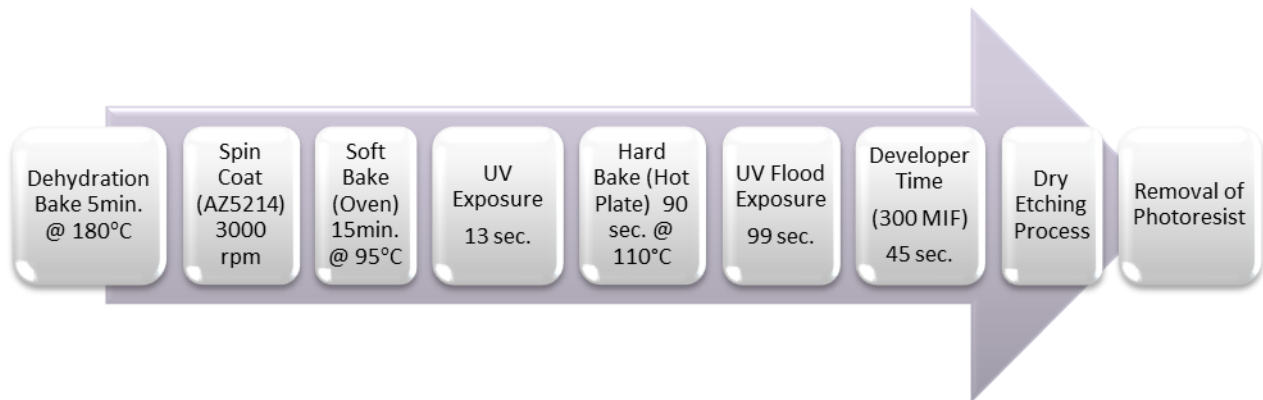


Figure 3.2. Steps for image reversal photolithography process.

### 3.1.1. Sample Cleaning for Photolithography Process

The substrates are cleaned in order to remove contaminants and surface oxides before the photoresist is applied. The cleaning process consists of: (1) immersion of the substrate in acetone for 5



minutes, (2) immersion in methanol for 5 minutes, (3) rinse in DI water for 5 minutes, and (4) drying with N<sub>2</sub> gas [76]. The oxide layer on the Si substrate is removed with a buffered oxide etch (BOE) solution by immersing the substrate in the BOE solution for 1 minute, then the sample is rinsed with DI water and dried with N<sub>2</sub> gas. This cleaning process is performed prior to all deposition or major processing steps.

### 3.1.2. Photoresist (AZ5214) Application Process

The optimum parameters for a high quality, well defined pattern are identified based on a series of processes. The sample is first dehydrated on a hot plate at 180°C for 5 minutes and then a thin layer of positive photoresist (AZ5214) is applied on the substrate using a spin coater, at 3000 rpm to produce a uniform thin 1 µm layer (Figure 3.3).

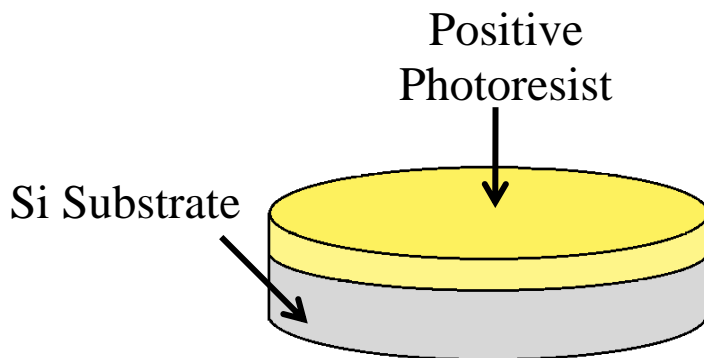


Figure 3.3. Positive Photoresist on Silicon Substrate [89]

A “soft bake” process is performed at 95°C for 15 minutes to evaporate the solvents in the photoresist. The dehydration, spinning, and soft bake time parameters used in this study are based on prior work by Lopez *et al.* [76].

### 3.1.3. Exposure Step

After the soft bake, a UV light exposure for 13 seconds occurs with the MJD3 mask aligner under hard contact mode with energy of  $100 \text{ mJ/cm}^2$  (Figure 3.4). Next, a hard bake at  $110^\circ\text{C}$  for 90 seconds activates the cross-linking agent and neutralizes the PAC. This hard bake step makes the exposed areas insensitive to further radiation and insoluble to the developer solution. The mask is removed and a flood exposure for 99 seconds makes the previously unexposed areas to become soluble to the developer solution.

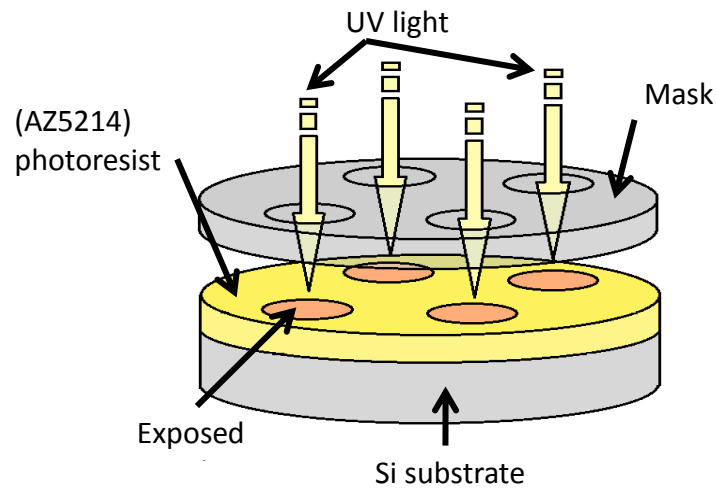


Figure 3.4. UV exposure process of photoresist [89].

The photomask consists of square window arrays of  $2 \mu\text{m}$ ,  $1.5 \mu\text{m}$ , and  $1 \mu\text{m}$  in diameter as shown in Figure 3.5. As the size of the windows decreases, the geometric shape of the photomask changes from a square to a circle, since the low resolution affects the smallest windows when the mask is fabricated.

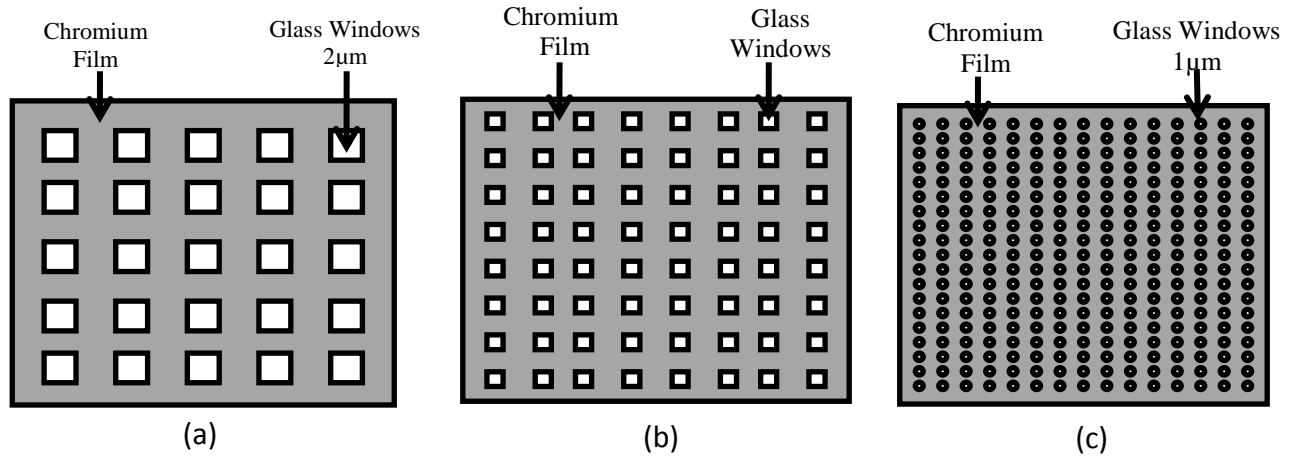


Figure 3.5. Photomask feature sizes (a) 2  $\mu\text{m}$ , (b) 1.5  $\mu\text{m}$ , (c) 1  $\mu\text{m}$  (Images are not to scale) [89].

The photomask is a glass plate coated with a layer of chromium film, which prevents UV light from transmitting through it. There are two mask polarities that can be used depending on the desired pattern, the light field polarity or the dark field polarity [76]. The dark field polarity is the one used in this study, since the pattern is created by removing a small amount of the chromium film as illustrated in Figure 3.5. The gray part of the mask is the chromium coated glass.

#### 3.1.4. Development Process

The next step of the photolithography process is to develop the photoresist. The substrate is immersed in a 726MIF developer solution for 40 sec to remove the soluble photoresist. The insoluble material remains on the substrate and a reversal image of the mask is obtained. Figure 3.6 illustrates the pattern on the substrate after the developer step is complete.

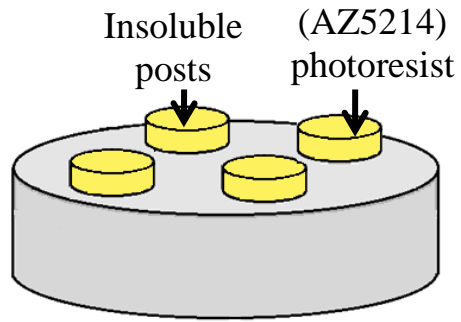


Figure 3.6. Patterned Si substrate with positive (AZ5214) photoresist [89].

The pattern shown in Fig. 3.6 is confirmed using the scanning electron microscope (SEM). Several experiments are required in order to determine the optimal exposure and developer times to obtain a high quality pattern. Table 3.1 includes a summary of all the experiments performed to determine the optimal exposure and developer times for the (AZ5214) photoresist. These experiments helped to identify the optimum process, a 13 second UV exposure, a 99 second flood exposure, and a developer time of 40 seconds.

Table 3.1. Summary of Photolithography Experiments.

<b>Negative -AZ5214 Photoresist (PR)</b>				
<b>Sample</b>	<b>Exposure Time (sec.)</b>	<b>Flood Exposure Time (sec.)</b>	<b>Developer Time (sec.)</b>	<b>Quality</b>
<b>1-NPR</b>	14	28	25	PR left
<b>2-NPR</b>	16	32	30	Poor Pattern
<b>3-NPR</b>	18	36	35	PR left
<b>4-NPR</b>	20	40	35	No Pattern
<b>5-NPR</b>	17	34	15	PR left
<b>6-NPR</b>	13	26	10	PR left
<b>7-NPR</b>	13	52	20	No Pattern
<b>8-NPR</b>	13	104	60	No Pattern

<b>9-NPR</b>	13	102	50	No Pattern
<b>10-NPR</b>	13	99	40	High Quality Pattern

### 3.1.5. Dry Etching Process

Dry etching is an anisotropic etch that uses an ionized gas to selectively remove material, and has the capability of defining small feature sizes  $< 100$  nm [77]. An anisotropic etch removes material preferentially in one direction with high aspect ratios and etches vertically at greater rate. In contrast, an isotropic etch occurs equally in all directions at similar rates and low aspect ratios. For the purpose of this study, an Oxford PlasmaLab 80 Plus radio frequency (RF) plasma-based is used to create the Si pillars illustrated in Figure 3.7.

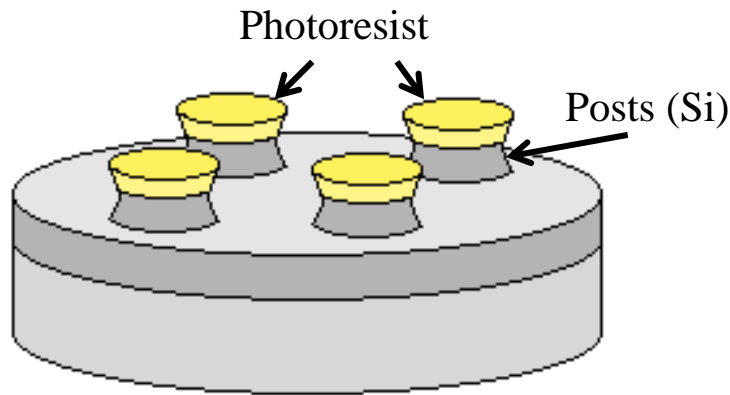


Figure 3.7. Patterned substrate after dry etching procedure [89].

Sulfur hexafluoride ( $\text{SF}_6$ ) is the ionized source of gas used to provide the fluorine, since the use of fluorine based chemistry is needed to etch silicon. The gas is introduced into the plasma chamber where RF power is applied to a pair of electrodes within the processing chamber. The applied power accelerates the electrons increasing their kinetic energy, resulting in the collision of electrons and neutral

gas molecules creating ions. The reaction in the plasma etching process is physical and chemical. The physical reaction is when collisions occur between the plasma chamber and the wafer, whereas the chemical reaction occurs when ions react with the atoms of the wafer and diffuse as bulk gas. (See Figure 3.8)

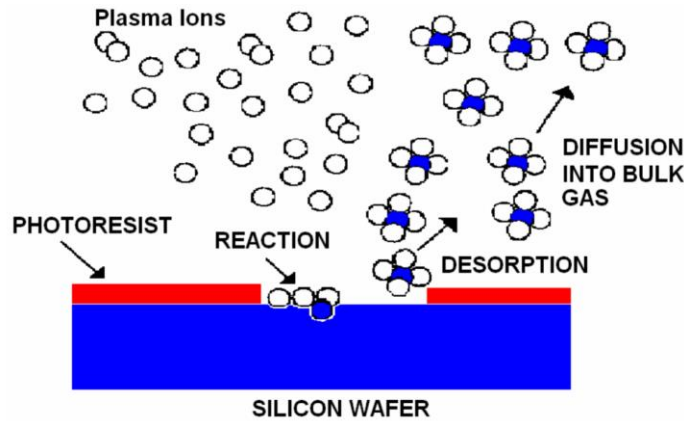


Figure 3.8. Illustration of Plasma Dry Etching Process [78].

Anisotropic etch occurs in a plasma-based dry etching process, where the pressure of the system controls the horizontal etch rate and RF power of the chamber controls the vertical etch rate. As a result, the higher the pressure and RF power, the higher the etch rate will be in both direction directions, resulting in the formation of Si pillars [78].

In this study, the anisotropic dry etching process is studied and optimized in order to obtain a high quality pattern with well-defined pillars and a smooth surface. Several parameters are examined such as the flow of gas (SCCM), RF power (Watts), gas pressure (Torr) and the etch time, in order to achieve Si pillars with a diameter between 1.5  $\mu\text{m}$  – 500 nm. (as reported by Syau and Perry [79,80,81]). Table 3.2 includes a list of the experiments used to optimize the parameters for the etching process in order to obtain pillars down 450 nm in diameter.

Table 3.2. Summary of Dry Etch Experiments for Silicon using SF<sub>6</sub> gas.

<b>Dry etching for Silicon-PlasmaLab</b>					
<b>Sample</b>	<b>Gas Flow (sccm)</b>	<b>RF Power (watts)</b>	<b>Gas Pressure (Torr)</b>	<b>Etching Time (min./sec.)</b>	<b>Results -Diameter Size</b>
<b>2-NPR</b>	30	160	0.05	4	1.5 μm
<b>3-NPR</b>	30	170	0.07	3/45	1 μm
<b>5-NPR</b>	30	180	0.1	3/45	500 nm
<b>6-NPR</b>	30	170	0.09	3	700 nm

### 3.1.6. Removal of Photoresist

Photoresist remains on the substrate after the etching process and is removed when the substrate is immersed into a piranha solution. A piranha (H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>) solution with a corresponding ratio of 5:1 is heated at 130°C for 10 minutes and is used to remove the photoresist [76].

## 3.2. OPERATION AND IDENTIFICATION OF PARAMETERS FOR CSS REACTOR

### 3.2.1. Basic Operation of CSS

The set-up of the source and the substrate consists of three steps: (1) placing the source on top of the bottom graphite block, (2) two 1 mm glass spacers are placed on top of the source, and (3) the substrate and bottom block are placed on top of the two glass spacers, as shown in Figure 3.9. K-type thermocouples are used in order to monitor the temperature of each graphite block by inserting one thermocouple in each graphite block. The set-up mentioned above is placed inside the liner and vacuum chamber as illustrated in Figure 3.10. Four 1000 W halogen lamps are located outside the reactor, two above the substrate and two below the source, and are used to provide thermal energy to each of the graphite blocks. The temperature of each graphite block is monitored by two thermocouples, which measure the temperature in Kelvin (K) and send the signal to a eurotherm. LabVIEW 7.1 software compares the thermocouple temperature reading to the temperature setting in LabVIEW for the source

and substrate graphite blocks independently, and the power to the lamps is adjusted using a proportional integral derivative (PID). In order to control the systems pressure, MKS Instruments mass flow controllers are used to adjust the flow of helium and oxygen gas. In this study helium gas is used to establish a clean growth environment, the growth rate and nucleation sites [82]. For each experiment, 1 mm spacers were used between the source and the substrate, which results in fast deposition rates between 0.01  $\mu\text{m/hr}$  and 4680  $\mu\text{m/hr}$  [3,6,18], depending on the temperature and pressure values. The software displays a table, where the user inputs the parameters to create a growth recipe.

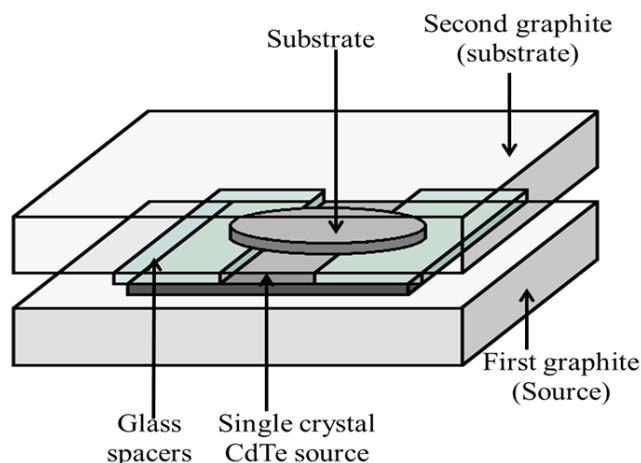


Figure 3.9. Source and Substrate Set-up [89].

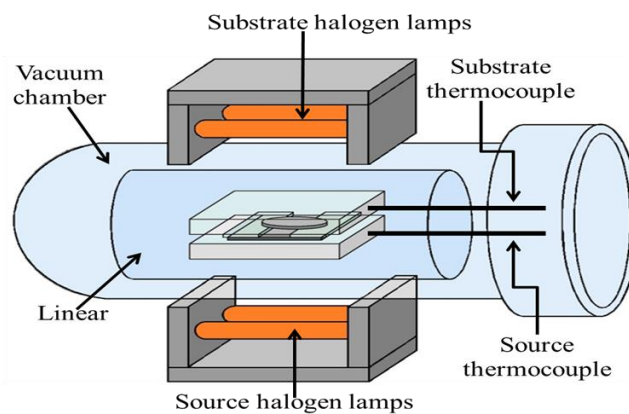


Figure 3.10. Schematic of CSS reactor [89].



### 3.2.2. CSS Growth Parameters

When using the CSS, the deposition parameters can be adjusted through the CSS LabVIEW software such as the source and substrate temperatures, the systems pressure, the deposition time, and the gas flow inside the reactor. Table 3.3 includes the parameters of a typical CSS recipe recommended for optimal CdTe growth based on CdTe planar and selective growth studies by Escobedo *et al.* and Diaz *et al.* The deposition process of selective CdTe growth consists of the following steps: purging cycle, warm-up, deposition ramp, deposition, and cooling steps. (Table 3.3)

Table 3.3. Deposition Recipe.

	Purging Steps						Warm-up	Dep. Ramp	Deposition	Cooling
<b>Time (sec.)</b>	60	60	60	60	60	60	290	150	300	180
<b>He Flow (SLPM)</b>	0	4	0	4	0	4	0.1	0.1	0.1	0
<b>O<sub>2</sub> Flow (SLPM)</b>	0	0	0	0	0	0	0	0	0	0
<b>Sub. Temp. (°C)</b>	0	0	0	0	0	0	400	450	450	0
<b>Sou. Temp. (°C)</b>	0	0	0	0	0	0	450	550	550*	0
<b>Pressure (Torr)</b>	0.1	100	0.1	100	0.1	100	5	5	5*	0.1

\*Additional experiments performed with varying source temperature and system pressure as shown in Tables 3.4, 3.5, and 3.6 in the following sections.

In order to improve the quality of the CdTe grains during selective growth, a warm-up and deposition ramp step is performed during the initial stages of growth. Since Y. Xin *et al.* [76] reported that pinholes on CdTe films can be prevented when a pre-treatment is performed to the substrate at the warm-up and deposition ramp steps of the CdTe growth. Furthermore, J.G. Major *et al.* [82] reported that when CdTe layers are grown using the CSS, the sublimation rate is control by the systems pressure, since high pressures decreases the sublimation rate. Consequently, it is expected that high system pressures will increase the CdTe grain size [82]. In this study, the source temperature is varied between 550°C and 560°C, and the pressure of the system is varied between 5 – 0.25 Torr. The substrate

temperature and deposition time are maintained at 450°C and 5 minutes, respectively, throughout the study.

During the warm-up step, the substrate and source temperatures are increased to 400°C and 450°C, respectively, in a 5 minute ramp. The substrate temperature is set to 450°C and the source temperature to 550°C for 3 minutes during the deposition ramp step. The deposition ramp step is followed by a 5 minutes deposition step, after which the temperatures of the substrate and source are allowed to cool to room temperature. Figure 3.11 illustrates the time-temperature profile sequence described above.

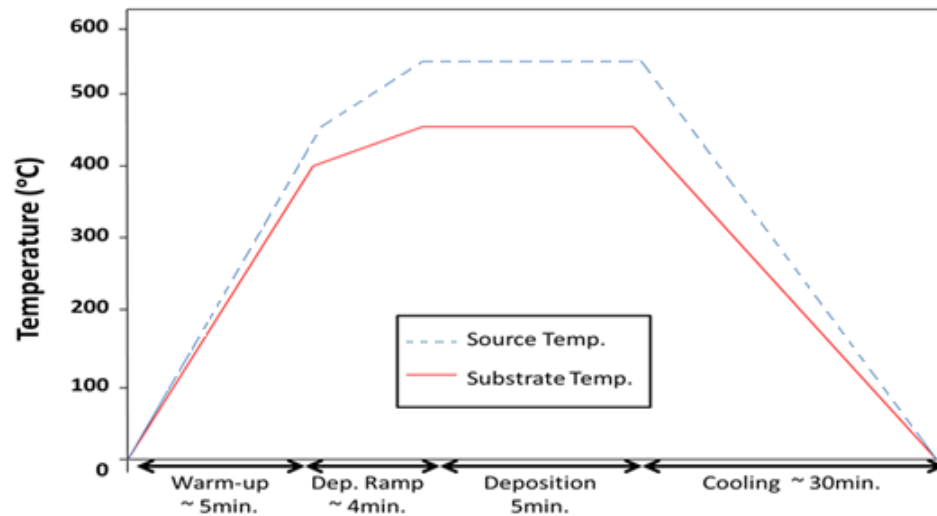


Figure 3.11. Time vs. temperature graph for CdTe growth [89].

### 3.2.3. Parameter Comparison to other studies for Selective CdTe Growth on Si(111) and Si(211) using MOVPE and MBE

Prior epitaxial CdTe growth studies on Si substrates have focused on the (211) orientation [5-9]. Shintri [5] and Bhat [6] explored a pattern technique to grow CdTe on Si substrates using the MOVPE epitaxial growth technique. Shintri [5] used a thin Ge buffer layer and Bhat [6] used a Si<sub>3</sub>N<sub>4</sub> mask layer prior to achieving selective CdTe growth. Selective CdTe growth was achieved for growth temperatures

higher than 500°C and pressures lower than 25 Torr. According to the two studies mentioned above, the quality and surface morphology of the epitaxial lateral overgrowth (ELO) of CdTe is very sensitive to the orientation of the growth windows [7]. These studies recommended that the substrate pattern be reduced to the nanometer scale in order to reduce the number of dislocations at the interface of the adjoining grains. Fahey [8] and Seldrum [9] achieved selective CdTe growth by using ZnTe as buffer layer and by As passivation, respectively, on Si(211) substrates using the MBE epitaxial growth technique. The selective growth for these studies was achieved for substrate temperatures higher than 345°C. This dissertation is based on growth studies like those mentioned here, in addition to other observations from the literature associated with the fabrication parameters that affect the quality of CdTe growth. These include substrate/source temperature, reactor pressure, substrate orientation and selective growth (pattern/pillar size) [3,5,6,8,9]. In this study, micron to nano-scale pillars are used to examine CdTe selective growth for various source temperatures, reactor pressures, and pillar (pattern) sizes on Si(111) and Si (211) substrates. The purpose of this study is to examine the CdTe growth structure based on the two substrate orientations by using TEM to identify the growth orientation and to quantify the misorientation at the interface. In this study, a single crystal CdTe(111) source with twins is used as a sublimation source in order to improve the quality of the growth and prevent the process of making a powder source [55]. Prior to CdTe deposition, the source is annealed for 30 minutes at 600°C, in order to produce repeatable growth rates.

### **3.2.4. CSS Selective Growth Study Procedure**

#### ***3.2.4.1. Sample Cleaning Procedure***

The Si substrates are cleaned in the same manner as described in Section 3.1.1 for the lithography procedure using a piranha solution with a 5:1 ratio ( $H_2SO_4:H_2O_2$ ) to remove surface contaminations and a BOE solution to remove the native oxide on the surface. The sample is placed into the CSS reactor immediately after the cleaning procedure.

### 3.2.4.2. Selective CdTe Growth Studies

The parameters for selective CdTe deposition using the CSS technique are based on results by Escobedo [55], where CdTe is selectively deposited on patterned CdTe(211)/Si(211) using a  $\text{Si}_3\text{N}_4$  mask layer, and based on a study by Diaz, where CdTe is grown on patterned Si(100) without a mask layer. Escobedo achieved selective growth by using a source temperature of 530°C, substrate temperature of 450°C, and system pressure of 5 Torr. Diaz used the same reactor but deposited on patterned Si(100) without a mask layer and achieved selectivity by using a source temperature of 550°C, a substrate temperature of 450°C, and a system pressure of 5 Torr. Figure 3.12 (a-d) illustrates and compares the results of these two studies, where (a) and (b) include SEM and TEM images of selective CdTe deposited on CdTe/ZnTe/Si(211) substrates using  $\text{Si}_3\text{N}_4$  as a mask layer, and (c) and (d) include corresponding images of selective CdTe growth on Si(100) substrates without a mask layer.

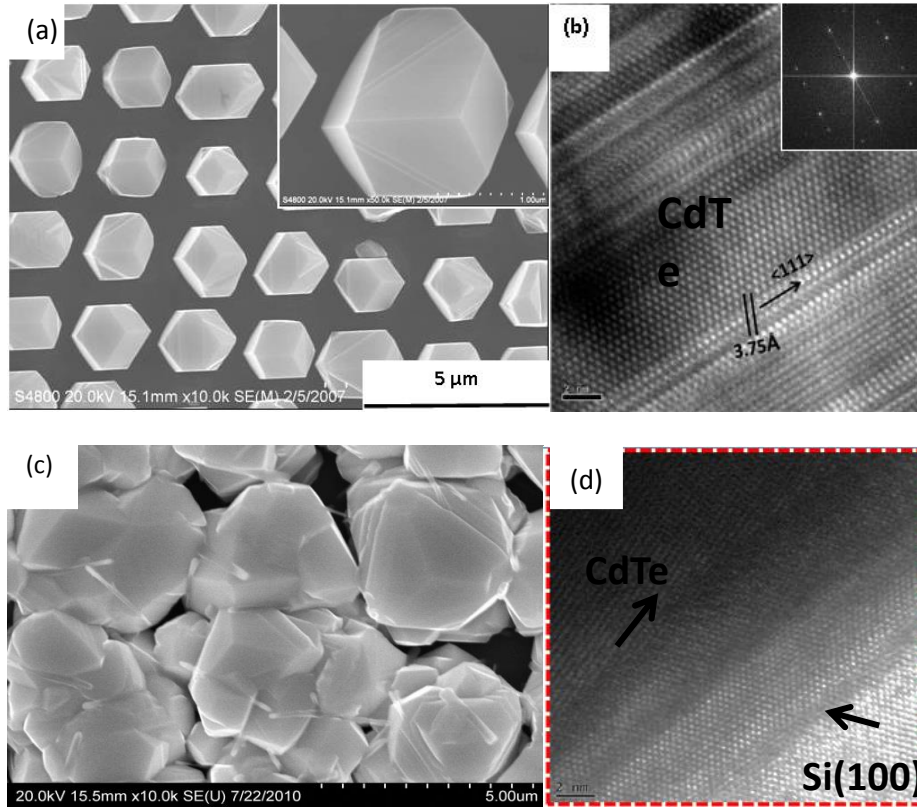


Figure 3.12. SEM and TEM images of (a-b) selective CdTe growth on CdTe/ZnTe/Si(211) substrates [26] and (c-d) selective CdTe growth on Si(100) substrates[3].

In this study, an attempt is made to improve the quality of CdTe growth by choosing two different substrate orientations, Si(111) and Si(211). The deposition parameters used by Escobedo and Diaz are optimized, and selective CdTe growth on Si pillars without the use of a mask is successful for these orientations. In addition, selective growth studies are conducted on 1  $\mu\text{m}$  and 500 nm patterned substrates in order to observe the effect of the pattern size on the quality of the CdTe grains and corresponding CdTe/Si interface. Tables 3.4 and 3.5 include a summary of the parameters studied for selective CdTe growth on Si(111) and Si(211) substrates, respectively. The parameters are the source and substrate temperatures, system pressure, deposition time, and pattern size.

### **Set I: Si(111) Study**

For the selective growth of CdTe on Si(111) substrates (Table 3.4), the source temperature and substrate temperature are kept constant at 550°C and 450°C, respectively, and the deposition time is 5 minutes for all the samples. Major *et al.*[82] reports the control of grain size for planar growth of CdTe by CSS to improve the performance of CdTe/CdS solar cells. It is observed that at high system pressures, the size of CdTe grains increases, which could be due to lower deposition rates at high pressures and low nucleation density with fewer grains growing at a high rate [82]. Consequently, in this set of experiments the system pressure (Torr) is varied between 5 Torr and 0.25 Torr to observe the effect on grain size. In addition, CdTe growth on 1  $\mu\text{m}$  and 500 nm patterned substrates are analyzed to observe the effect the pattern size on the CdTe grain size and growth quality.

Table 3.4 Summary of experiments performed for the selective CdTe epitaxial growth on Si(111) Substrates.

<b>Sample</b>	<b>Tsub (°C)</b>	<b>Tsou (°C)</b>	<b>Pressure (Torr)</b>	<b>Deposition Time (min.)</b>	<b>Pattern Size</b>
<b>S111-2</b>	450	550	5	5 min.	1 $\mu\text{m}$
<b>S111-10</b>	450	550	2	5 min.	1 $\mu\text{m}$
<b>S111-12</b>	450	550	1	5 min.	1 $\mu\text{m}$
<b>S111-14</b>	450	550	0.5	5 min.	1 $\mu\text{m}$
<b>S111-16</b>	450	550	0.25	5 min.	1 $\mu\text{m}$
<b>S111-18</b>	450	550	1	5 min.	1 $\mu\text{m}$
<b>S111-23</b>	450	550	0.5	5 min.	1 $\mu\text{m}$
<b>S111-25</b>	450	550	0.25	5 min.	1 $\mu\text{m}$
<b>S111-1</b>	450	550	5	5 min.	500 nm
<b>S111-19</b>	450	550	2	5 min.	500 nm
<b>S111-17.2</b>	450	550	0.5	5 min.	500 nm
<b>S111-15</b>	450	550	0.25	5 min.	500 nm

### **Set II: Si(211) Study**

Previous studies by Shintri<sup>5</sup> and Bhat<sup>6</sup> focused on the selective CdTe growth on Si(211) substrates to improve the quality of CdTe films for the subsequent growth of HgCdTe films using Ge as a buffer layer and Si<sub>3</sub>N<sub>4</sub> as a mask layer, respectively [5-9]. It has been reported that epitaxial growth on Si(211) substrates reduces dislocations in the film using the MBE deposition technique, making (211)B the preferred orientation for CdTe growth on Si since twin formation is avoided [5,7,83]. For this reason, the second set of experiments in this dissertation consists of selective CdTe growth on patterned Si(211) substrates (Table 3.5). It is desirable to add to the literature by comparing the effect of the substrate orientation using the inexpensive CSS technique. The source temperature is varied between 550°C and 560°C to improve growth uniformity. The substrate temperature is kept constant at 450°C and the deposition time for all samples is 5 minutes. The system pressure is varied between 5

Torr and 0.25 Torr to observe the effect on grain nucleation and grain growth/grain size. The pillar size is also varied between 500 nm and 1  $\mu\text{m}$  in order to compare the CdTe growth for this set to the first set of experiments with Si(111) substrates.

Table 3.5. Summary of experiments performed for the selective CdTe epitaxial growth on Si(211) Substrates.

<b>Sample</b>	<b>Tsub (°C)</b>	<b>Tsou (°C)</b>	<b>Pressure (Torr)</b>	<b>Deposition Time (min.)</b>	<b>Pattern Size</b>
<b>S211-6</b>	450	550	0.5	5 min.	1 $\mu\text{m}$
<b>S211-8</b>	450	560	0.5	5 min.	1 $\mu\text{m}$
<b>S211-11</b>	450	550	0.25	5 min.	1 $\mu\text{m}$
<b>S211-12</b>	450	560	0.25	5 min.	1 $\mu\text{m}$
<b>S211-13</b>	450	550	5	5 min.	1 $\mu\text{m}$
<b>S211-14</b>	450	550	1	5 min.	1 $\mu\text{m}$
<b>S211-9</b>	450	550	0.25	5 min.	700 nm
<b>S211-10</b>	450	550	0.5	5 min.	500 nm
<b>S211-5</b>	450	550	0.5	5 min.	700 nm

### 3.3. CHARACTERIZATION OF CdTe GRAIN STRUCTURE AND CdTe/Si INTERFACE

The CdTe selective growth morphology, orientation and quality, along with strain at the CdTe/Si interface is analyzed in this study. The morphology of selective CdTe growth is characterized using the scanning electron microscopy (SEM) for each sample in order to identify high quality CdTe films. A single sample characterized as being “high quality” from each set is further analyzed using transmission electron microscopy (TEM). “High quality” CdTe grains are identified based on features indicating that the grain structure consists of a single grain with a smooth flat surface or with planar facets as illustrated in Figure 3.13, from the CdTe growth study on Si(100) substrates (from same study as growth shown in Figure 3.12 (c) and (d)).

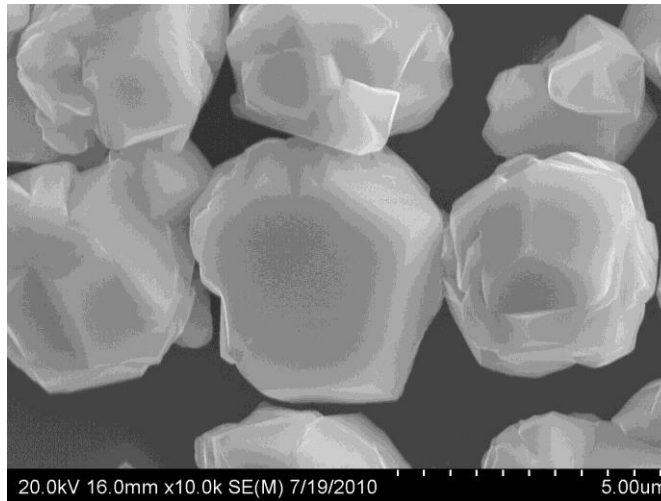


Figure 3.13. SEM image of selective growth on Si(100) substrate[3].

The TEM characterization analysis is conducted in order to examine the structural features of the CdTe grains and the strain at the CdTe/Si interface at the atomic scale. Two different TEM modes of operation are used, high resolution transmission electron microscopy (HRTEM) mode and diffraction mode. The HRTEM mode is capable of resolving individual rows of atoms or planes, the distance between each plane, and lattice defects such as dislocations, twins and stacking faults. The diffraction mode provides information on the crystal structure, defects (twins), and misorientation at the CdTe/Si interface. TEM samples are prepared using the focused ion beam (FIB) procedure at The Center for Integrated Nanotechnologies (CINT) located in Albuquerque, NM. The TEM diffraction pattern and HRTEM image for each sample are used to identify and compare the following structural features:

1. Identification of the orientation of the CdTe growth and Si substrate based on indexing of the CdTe and Si diffraction patterns.
2. Identification of planes on the HRTEM CdTe and Si images based on indexing of the diffraction patterns.
3. Measurement of the CdTe film d-spacings using the indexing of the diffraction patterns and corresponding planes on the HRTEM image, and comparison to theoretical CdTe d-spacings.



4. CdTe/Si interface misorientation angle measurement based on the diffraction pattern at the interface.
5. Identification of defects and stacking faults at the CdTe/Si interface on the HRTEM images.

### **3.3.1. Scanning Electron Microscope (SEM) Instrumentation**

A Hitachi 2-4800 scanning electron microscope (SEM) is used as the first characterization tool since it is able to provide a high resolution images. This instrument consists of an electron gun that accelerates electrons to the sample, where these electrons are focused by electromagnetic coils, and the focused electron beam makes a scan of the sample. Secondary and backscatter electrons are produced from the electrons that interact with the sample, and are detected by the backscatter detector, which creates an image of the sample surface.

### **3.3.2. Transmission Electron Microscope (TEM) Instrumentation**

Transmission electron microscopy (TEM) is used in the fabrication of semiconductor devices, since it is a versatile characterization tool to analyze samples from the atomic scale (nanoscale range) to the micron scale [84]. The TEM system consists of a FEI Tecnai F30 scanning electron microscope (STEM) (Hollisboro, OR) with quasi-monochromatic beam of electrons emitted by a monochromatic field-emission source and accelerated with a working voltage of 300 kV [85]. The relationship between accelerating voltage (energy of electrons) and wavelength is based on the Louis de Broglie's relationship [84]:

$$\lambda = \frac{1.22}{E^{1/2}} \quad \text{Eq. 3.1}$$

where E is the energy of the electrons (eV) and  $\lambda$  is the electron wavelength in nm. The TEM is composed of a series of magnetic, diffraction, intermediate, and projector lenses that select an area on

the sample, where the area size can be change by the current of the magnetic lenses, making the area size as low as 1  $\mu\text{m}$ . This area on the sample sets the field view of the TEM and projects an image of the area on the screen. The sample holder in a TEM has a tilting stage to adjust the sample orientation in order to satisfy the Bragg condition and allow small amount of electrons to transmit or scatter through the sample forming parallel arrays from the sample [85].

The TEM can be operated in imaging or diffraction mode. Figure 3.14(a) and (b) shows the operation of the diffraction mode and image mode, respectively. The diffraction mode operates when diffraction lens and electron beam created by the electron source emits parallel arrays to the back focal plane, giving a magnified diffraction spot pattern of the sample area [85]. Under the image mode operation the electron beam produced by the electron source emits parallel arrays to the 1<sup>st</sup> image plane aperture, where the aperture allows selecting a specific area of the sample and then is magnified by the intermediate lens. The electron beam from the intermediate lens brings into focused the area sample from the 1<sup>st</sup> plane aperture to the projector lens, which forms a magnified image of the sample area on the screen [85]. Therefore, the diffraction apertures in a TEM result in electrons that have undergone different Bragg reflections, creating different levels of image contrast. Furthermore, image mode is used to measure the distance between the planes and diffraction mode is used to identify the film orientation and measure the misorientation at the interface.

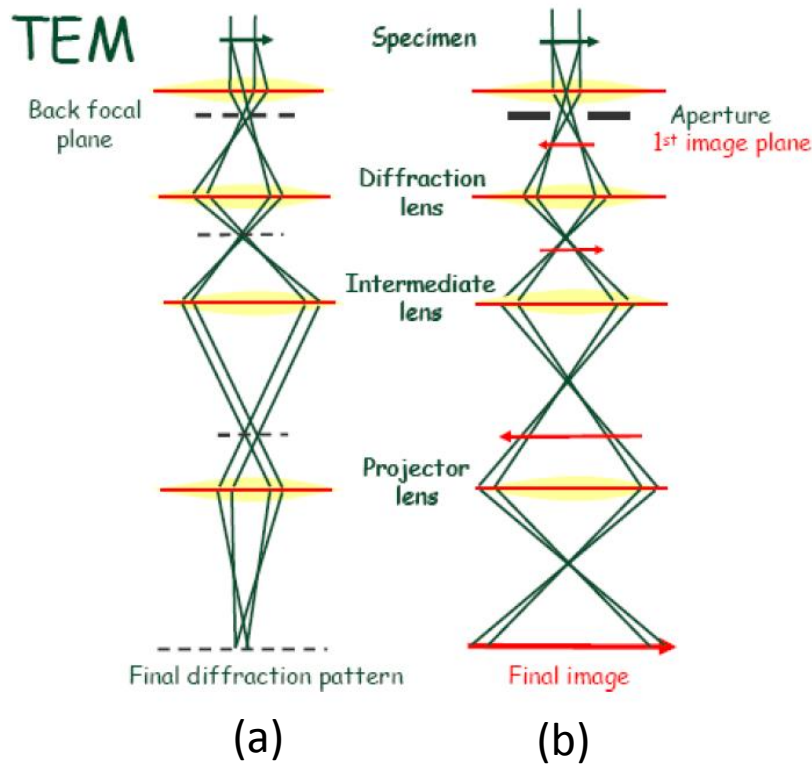


Figure 3.14. TEM operation of (a) diffraction mode and (b) image mode [85].

### 3.3.3. TEM sample preparation: Focused Ion Beam (FIB)

The preparation of a TEM sample requires thinning of the sample to less than 100 nm so that the sample is transparent to the electron beam. It is required for the sample to be thin enough in order for the electrons to be able to travel through the sample and generate a high intensity image on the photographic plate [84]. TEM samples can be prepared using several techniques, including, the focused ion beam (FIB) technique. The FIB technique has a major advantage over conventional methods since samples can be extracted from specific areas, and large uniform thin areas can be obtained. A Nova 600 NanoLab DualBeam™-SEM/FIB system is used to prepare two samples identified as high quality CdTe growth on Si(111) and Si(211) substrates. Figure 3.15 illustrates the major steps associated with the FIB process. The first step is to identify a region of interest on the sample, Figure 3.15(a). A

platinum layer is deposited on top of the region of interest to protect it from the ion milling process which can damage the material, making it amorphous, Figure 3.15(b). The sample is ion milled at 10.0 kV and 2.1 nA to a thickness of approximately 100 nm, Figure 3.15(c). Next, the sample is tilted approximately 35° to make u-cuts on both ends by ion milling at 20.0 kV and 4.2 nA, Figure 3.15(d). The sample is lifted using a needle, where the needle is used to deposit a small amount of platinum on top of the sample to pull it out, Figure 3.15(e). Once the sample is extracted, it is attached to a copper grid by depositing a small amount of platinum between the edge of the sample and the grid, Figure 3.15(f). Following the FIB procedure, the sample is placed in the TEM to confirm that it is transparent and provides the desired information about the area of interest.

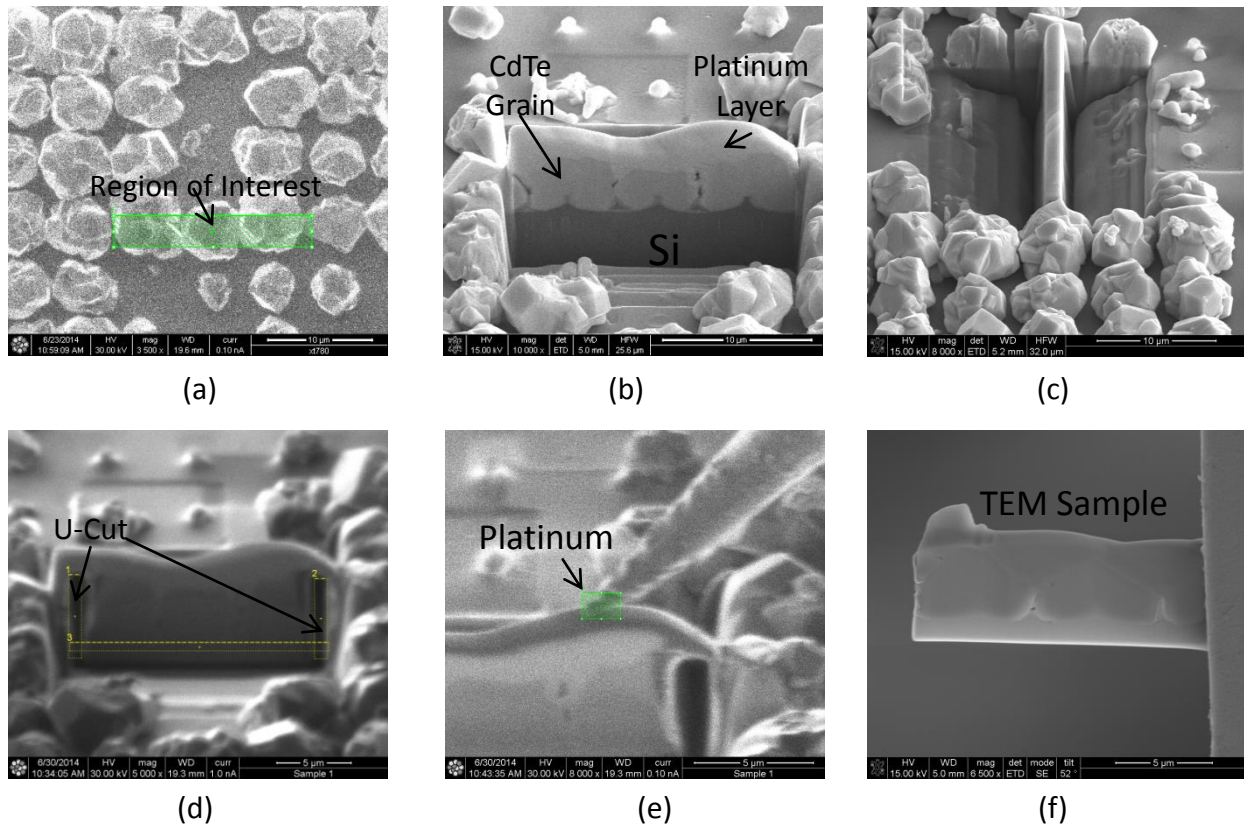


Figure 3.15. Major Steps associated with the FIB process.

### 3.3.4. TEM Analysis of CdTe Selective Growth and CdTe/Si Interface

The quality of the CdTe grains are examined using a FEI Tecnai F30 scanning electron microscope (STEM) (Hillsboro, OR) operating at 300 kV with an FEI double-tilt, top-entry-type sample holder. The image mode of the TEM gives a high resolution image of the sample at the atomic scale, resulting in resolutions of less than 1 nm. The top-entry-type sample holder provides high stability against sample drift, which is necessary for high resolution images.

#### Growth Orientation

The TEM provides information on the orientation of the CdTe growth and Si substrates based on indexing of the CdTe and Si diffraction patterns. Indexing of diffraction patterns is performed by the principles of crystallography using a low-index diffraction patterns for face centered cubic (FCC) materials as a reference to identify the planes for each diffraction spot. Figure 3.16, shows examples of three diffraction patterns for (a) a Si(113) substrate, (b) ZnTe having a [111] growth direction, and (c) a ZnTe/Si interface. These planes are transferred onto the corresponding high resolution TEM analysis in order to identify the orientation of the growth direction.

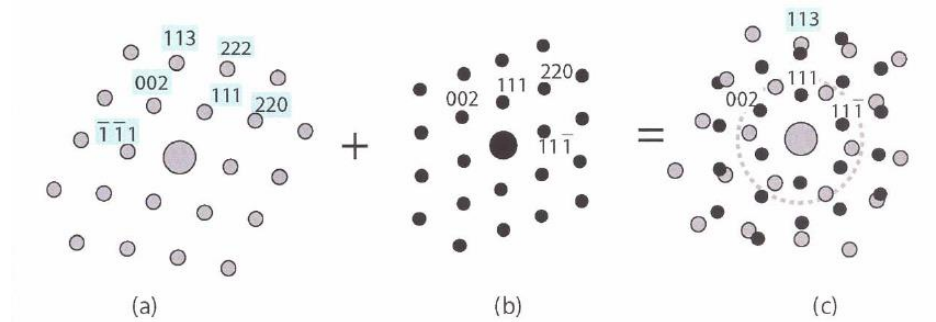


Figure 3.16. Diffraction patterns for (a) Si(113), ZnTe(111), and (c) ZnTe/Si interface[86].

## **Identification of Planes**

Using the TEM diffraction mode, the objective lens is placed on the first order spots of the diffraction pattern and HRTEM image is obtained as shown in Figure 3.17. In order to identify the lattice planes on the HRTEM image (Figure 3.17), the corresponding diffraction patterns (Figure 3.16) can be used once the lattice planes are identified on the diffraction pattern. The first step is to draw a vector from the transmitted beam to one of the planes (spots) on the diffraction pattern. Secondly, a line is drawing perpendicular to the vector (plane). The perpendicular line is transfer to the HRTEM image, which will give the direction on the HRTEM image for that specific plane. This procedure is performed for each plane (spot) identified on the diffraction pattern.

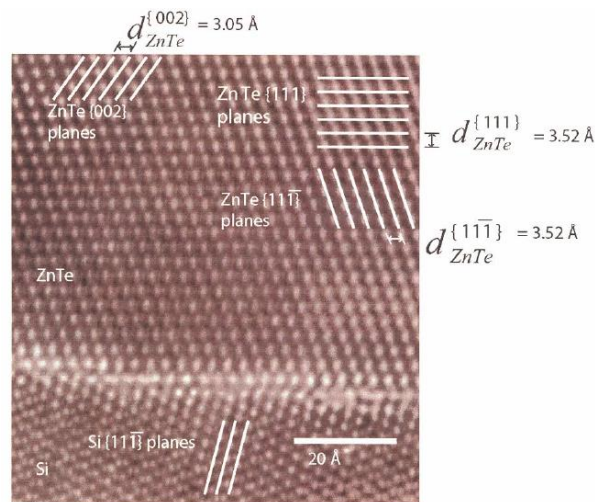


Figure 3.17. HRTEM image of ZnTe/Si interface [86].

## **Measurement of d-Spacing**

Once the planes are identified on the HRTEM image, the lattice spacings (d-spacing) can be measured from the HRTEM image directly using the bar scale, or the corresponding diffraction pattern (Figure 3.20) using the following equation:

$$R = \frac{\lambda L}{d_{hkl}} \quad \text{Eq. 3.2}$$

where R the is radius between the transmitted beam and a spot in the diffraction pattern,  $\lambda$  is the electron beam wavelength, and L is the TEM camera length. Once the d-spacing of the film is obtained, the strain at the interface can be calculated by comparing the measure d-spacing of the grown layer with the theoretical d-spacing using the following equation:

$$d_{hkl} = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \quad \text{Eq. 3.3}$$

where  $a$  is the lattice parameter of the material,  $(hkl)$  are the plane indices,  $d_{hkl}$  is the lattice spacing.

### **Misorientation at Interface**

The misorientation at the interface is calculated by measuring the misorientation angle on the diffraction pattern at the interface. Figure 3.18 shows an example of a diffraction pattern where the Si substrate and the ZnTe film have the same orientation, resulting in a close alignment of the Si and ZnTe spots, which indicates an interface with fewer defects, i.e. low misorientation between the film and substrate. Therefore, if there is a low misorientation at the interface, this results in less strain on the material.

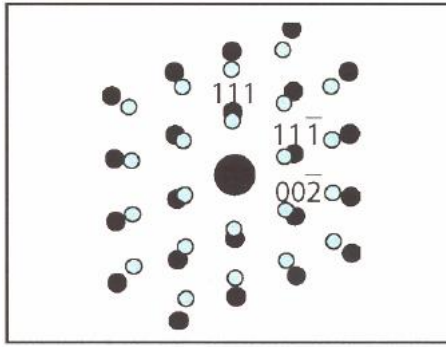


Figure 3.18. Diffraction pattern of ZnTe/Si interface [86].

In addition, two studies on planar CdTe growth on ZnTe/Si(211) substrates have been reported by Rijarawat [65] and Zhao [66] using ZnTe as a buffer layer. Figure 3.19 and 3.20 (a-b) illustrates the HRTEM and diffraction pattern image of these two studies. On the diffraction pattern (Figure 3.19), the misorientation angle at the interface is  $< 1^\circ$ , which confirms that CdTe has grown with the same orientation as the Si substrate. In Fig. 3.20, a misorientation angle of  $\sim 3.5^\circ$  is measured for the CdTe/Si interface from the image electron diffraction pattern (Figure 3.20 (a) inset).

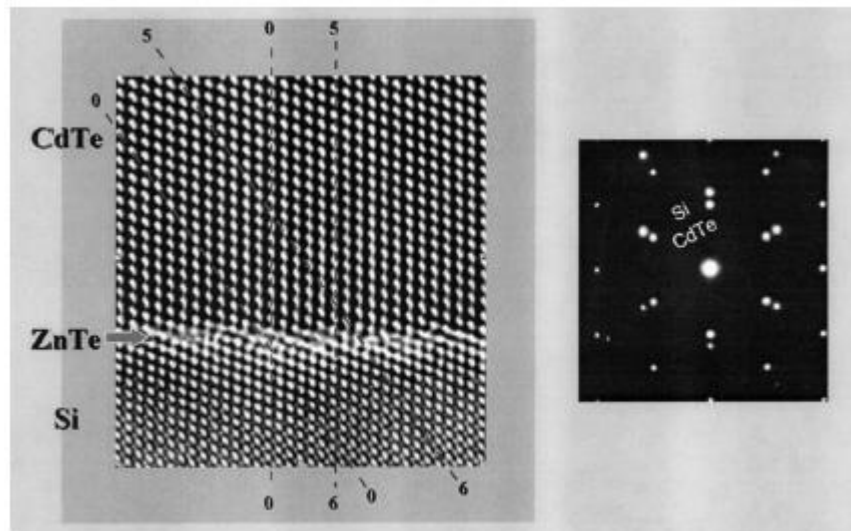


Figure 3.19. HRTEM image and diffraction pattern of CdTe(211) growth on ZnTe/Si(211) substrate [65].



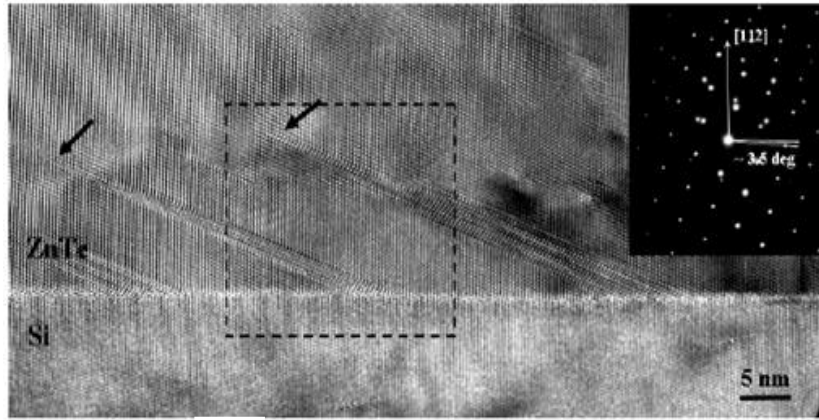


Figure 3.20. HRTEM image of CdTe(211)B growth on ZnTe/Si(211) interface with its corresponding diffraction pattern (inset) [66].

### **Defects and Stacking Faults**

The TEM provides information about the strain and the interface, along with defects that are created to accommodate the strain. For example, Rijarawat [65] reported the growth of unstrained CdTe layers using a buffer layer. His result was confirmed by measuring the d-spacing of the CdTe layers from the HRTEM image (Figure 3.19), which resulted in similar d-spacing compared to bulk CdTe. Furthermore, Zhao [66] reported that short structural defects most of which consisted of stacking faults formed at the Si substrate in the (111) direction and extending 50 nm away from the interface as indicated by the arrows (Figure 3.20 (a)). The defects present at the ZnTe/Si interface reduce the strain associated with the 12% lattice mismatched. Figure 3.21 is a HRTEM image of a CdTe/Si(100) interface on a micro-patterned Si(100) substrate, where the evolving misorientation between the film and the substrate is noticeable [3].

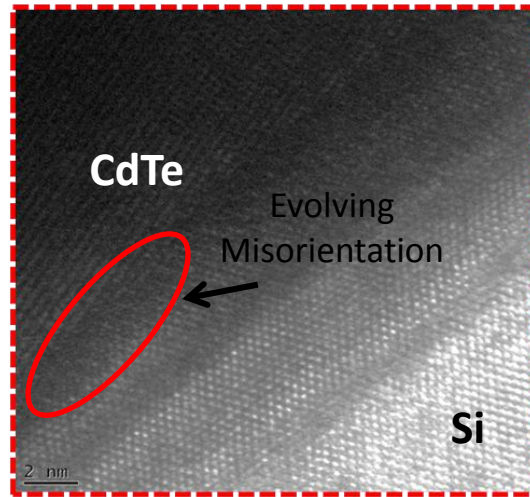


Figure 3.21. High-magnification TEM images of CdTe/Si interface on micropatterned Si(100) substrate [3].

## Chapter 4: Data and Results

In this study, selective CdTe grains are grown on patterned Si(111) and Si(211) substrates using the CSS technique. Si substrates were patterned by the photolithography method at the micron and nanoscale then dry etched to create pillars on the Si surface, followed by the selective growth of CdTe on the pillar surface using the CSS technique. The first set of experiments done in this study involved the growth of CdTe on patterned Si(111) substrates via CSS technique. This orientation was selected since polycrystalline CdTe grows predominantly in the (111) orientation for solar cell applications. The second set of experiments consisted of the selective growth of CdTe on Si(211) substrates using the CSS technique. When CdTe is grown selectively on windows of nanopatterned Si substrates, dislocations are reduced in the resulting CdTe film, since dislocations propagate to the side walls [21]. Selective CdTe growth on Si(211) surfaces have shown less twinning and lower dislocation densities of  $\sim 10^5 \text{cm}^{-2}$  to  $\sim 10^6 \text{cm}^{-2}$  [1,4,5,38,87,88]. High quality selective CdTe/Si(100) growth has also been achieved by Diaz *et. al*, using the CSS technique [3].

SEM and TEM characterization methods were used to analyze the surface morphology and the structure quality of the CdTe grains, along with the CdTe/Si interface for the growth of CdTe on Si(111) and Si(211) substrates. The SEM characterization was performed in order to confirm selective growth, analyze the quality of the CdTe growth based on the facet nature of the growth, and observe the effect pattern quality on the uniformity of growth. The TEM characterization was conducted using two different TEM modes, HRTEM and diffraction mode. The HRTEM mode provides information on the quality of the CdTe grain and the CdTe/Si interface at the atomic structure, by identifying any strain and defects such as twins and stacking faults according to the alignment of the atoms. In contrast, the diffraction mode results in diffraction patterns that provide information about the CdTe/Si interface, the lattice spacing, and the growth orientation with respect to the substrate orientation.

## 4.1 PHOTOLITHOGRAPHY OBSERVATIONS

The Si substrates were patterned at the micro- and nano-scale using negative photoresist. Figure 4.1 (a) and (b) illustrates the patterned substrates for the two different orientations (Si(111) and Si(211)), respectively, as a result of the photolithography process. The high quality patterned substrates were obtained by exposing the photoresist to the UV light through the windows in the mask for 13 seconds followed by a flood UV light exposure for 99 seconds without the mask. The UV light flood exposure step is done to achieve an image reversal from the positive photoresist. The last step was to develop the pattern for 40 seconds using a developer solution.

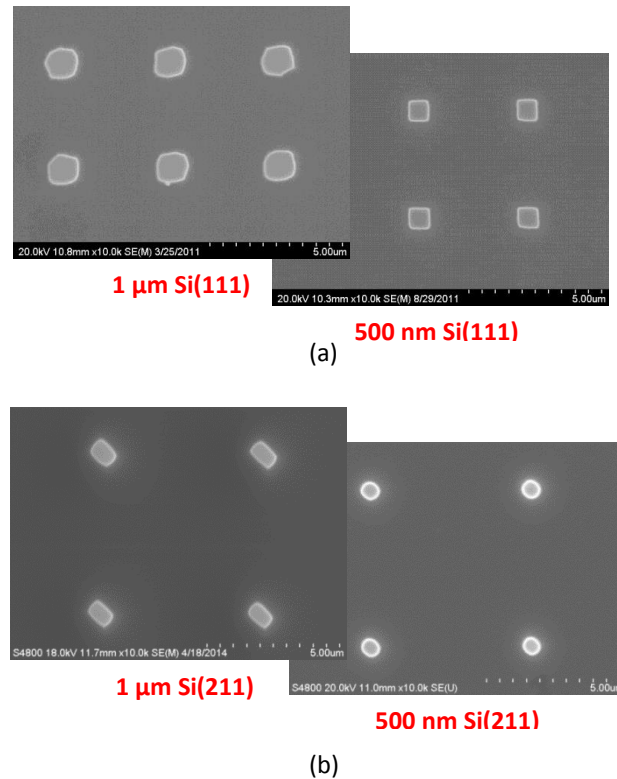


Figure 4.1. Si(111) and Si(211) Lithography Patterns.

## 4.2 DRY ETCHING OBSERVATIONS

The formation of well-defined pillars was accomplished after a series of experiments (which are explained in detail in Section 3.2). The pattern size was decreased from 1  $\mu\text{m}$  to the 500 nm during the dry etching process. Table 4.1 shows a summary of the parameters used to obtain high quality pillars using an anisotropic dry etch method.

Table 4.1. Summary of successful parameters used to create pillars on Si Substrates

Post Size	Gas Flow (sccm)	RF Power (Watts)	Gas Pressure (Torr)	Etch Time (min.)
<b>1 <math>\mu\text{m}</math></b>	30	120	0.06	5
<b>500 nm</b>	30	170	0.09	3
<b>450 nm</b>	30	180	0.1	3.45

Three different sizes of pillars were obtained for this set of experiments (Table 4.1). A longer etch time was used in order to decrease the pattern size from 1  $\mu\text{m}$  to 500 nm. Figures 4.2 (a) and (b) include tilt SEM images for two different sizes of pillars achieved for the Si(111) substrates, resulting in 1  $\mu\text{m}$  and 500 nm pillars. Moreover, Figures 4.2 (c) and (d) include corresponding SEM images for the Si(211) substrates, also for 1  $\mu\text{m}$  and 500 nm pillars. A high quality CdTe grain grown on top of a Si pillar requires a pillar to have a flat and smooth top surface. Therefore, a set of experiments was carried out to obtain an optimum etch rate ( $\sim 200$  nm/min.) that produces well-defined pillars, while not overetching the pattern. It is evident from Fig. 4.2 that the Si pillars have flat surfaces, which are needed to achieve high quality selective CdTe growth on the Si pillars.

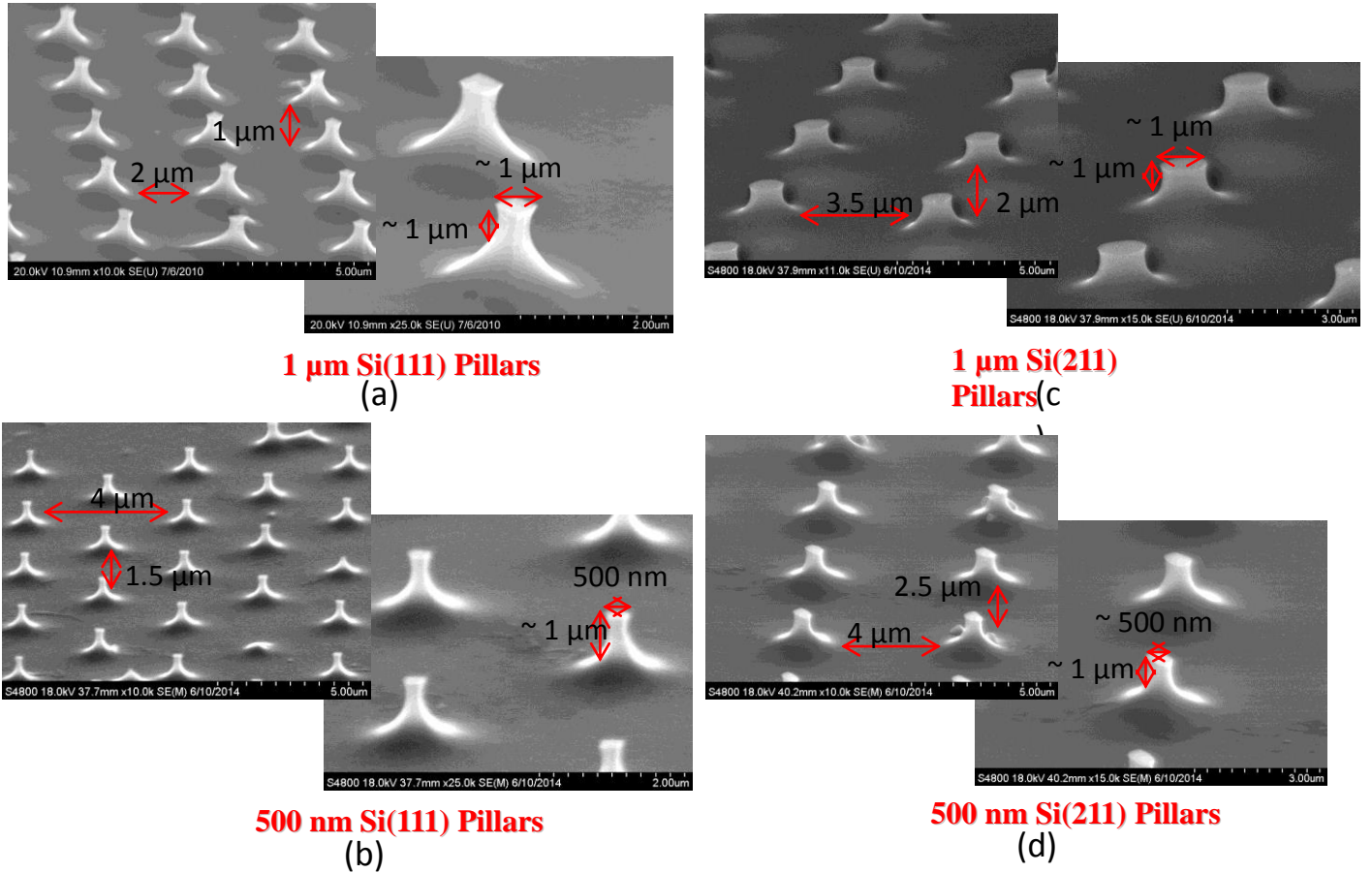


Figure 4.2. SEM images of (a) 1  $\mu\text{m}$  Si(111) Pillars, (b) 500 nm Si(111) Pillars, (c) 1  $\mu\text{m}$  Si(211) Pillars, and (d) 500 nm Si(211) Pillars.

### 4.3 SELECTIVE CDTE GROWTH VIA CSS

CdTe was grown on patterned Si(111) and Si(211) substrates using the CSS technique. Although the pillars on the Si substrates varied between 450 nm-1  $\mu\text{m}$  after dry etching, CdTe deposition was limited to patterned substrates with 1  $\mu\text{m}$  pillars and substrates with pillars ranging between 450-700 nm. The experiments were designed to grow a single CdTe grain on top of each pillar, while optimizing pattern uniformity throughout the substrate surface. Figure 4.3 includes a schematic of the desired selective growth.

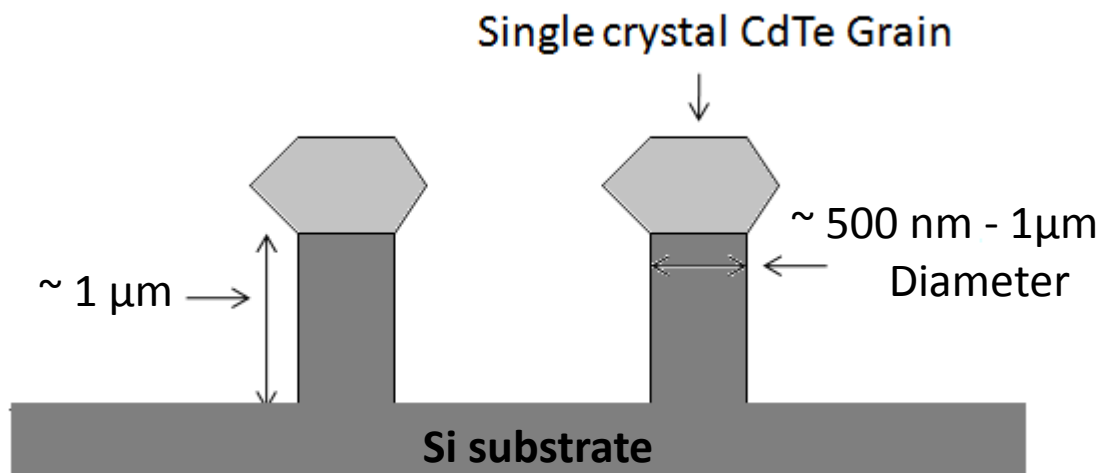


Figure 4.3. Schematic of selective CdTe growth on Si(100) substrate via CSS [89].

The CSS parameters that defined the selective CdTe growth were the substrate and source temperatures, the deposition time, and the pressure of the system, which assume that the growth follows the diffusion-limited model described by *Cruz Campa et. al.* [71]. The initial deposition parameters used were based on the work performed by *Diaz et. al.* [3], where she selectively deposited CdTe on a patterned CdTe/Si(100) substrate without a mask layer (See Fig. 2.3, in section 2.2). The CSS parameters developed by Diaz consisted of  $T_{\text{sub}}=450^{\circ}\text{C}$  and  $T_{\text{sou}}=550^{\circ}\text{C}$ , a pressure of 5 Torr, and a deposition time of 5 minutes. These parameters were modified in this study in order to selectively deposit CdTe on patterned Si(111) and Si(211) substrates. In this study, selective CdTe deposition occurred for almost all substrate and source temperature values tested.

In order to analyze the morphology of the CdTe films, the SEM was used to confirm selectivity and growth uniformity. The SEM characterization provides information on how the deposition parameters, as well as the pattern structure, affect selective growth and the growth of high quality single CdTe grains on the Si pillars. Other factors include, a reactor warm-up deposition step and annealing of the CdTe source prior to deposition, where the source was annealed for 30 minutes at  $600^{\circ}\text{C}$  in order to remove the thin oxide layer and produce repeatable growth rates for all set of experiments.

#### 4.3.1. Selective CdTe growth on Si(111) with 1 $\mu\text{m}$ pattern (Set I)

The first set of experiments were performed with Si(111) substrates in order to analyze the effect of the system pressure on the quality of the selective CdTe growth and the CdTe grain size. Reactor warm-up steps were included and the CdTe source was annealed prior to each deposition. Table 4.2 includes results pertaining to pattern size, uniformity of selective growth, and grain size as a function of temperature, pressure, and deposition time. Each deposition was carried out for 5 minutes for a substrate temperature of 450°C and source temperature of 550°C. The system pressure was varied between 5 – 0.5 Torr for this set of experiments. Since sample S111-23 and S111-25 resulted in the highest quality selective CdTe growth, the rest of the experiments in this growth study of CdTe on Si(211) substrates were carried out at these pressures (0.5 and 0.25 Torr).

Table 4.2. Summary of experiments performed on Si(111) substrates with 1  $\mu\text{m}$  pattern (Set I).

Sample	Pattern Size	$T_{\text{sub}}$ (°C)	$T_{\text{sou}}$ (°C)	Pressure (Torr)	Dep. Time	Uniformity (Poor, Fair, Good)	Grain Size
S111-2	1 $\mu\text{m}$	450	550	5	5 min.	Fair	5.1 $\mu\text{m}$
S111-12	1 $\mu\text{m}$	450	550	2	5 min.	Fair	4.7 $\mu\text{m}$
S111-10	1 $\mu\text{m}$	450	550	1	5 min.	Fair	4.3 $\mu\text{m}$
S111-23	1 $\mu\text{m}$	450	550	0.5	5 min.	Good	3.9 $\mu\text{m}$
S111-25	1 $\mu\text{m}$	450	550	0.25	5 min.	Good	3.8 $\mu\text{m}$

SEM images for the samples listed in Table 4.1 are shown in Figures 4.4 through 4.8. These images include a surface view of the substrate before and after CdTe deposition. Multiple micrographs are provided for the CdTe growth at low and high magnification. For this set of experiments, all samples were patterned at the micron-scale, resulting on Si pillars of 1  $\mu\text{m}$  diameter and 2  $\mu\text{m}$  pitch. The CdTe deposition for Sample S111-2 was performed for 5 minutes at  $T_{\text{sou}}=550^\circ\text{C}$  and  $T_{\text{sub}}=450^\circ\text{C}$ , where the average grain size was 5.1  $\mu\text{m}$  in diameter (Fig. 4.4). When the pressure was decreased from 5 Torr to 2 Torr (sample S111-12), the grain size decreased from 5  $\mu$  to 4.7  $\mu\text{m}$  for the same temperatures and deposition times (Fig. 4.5). Lowering the pressure further to 1, 0.5 and 0.25 Torr



resulted in grain sizes of 4.3, 3.9, and 3.8  $\mu\text{m}$ , respectively (samples S111-10, S111-23, S111-25 in Figs. 4.6, 4.7, and 4.8). The last two samples performed in this set of experiments resulted in the best quality selective CdTe growth. Figures 4.7 and 4.8 show SEM images for these two samples conducted with a system pressure of 0.50 and 0.25 Torr, respectively. According to this set of experiments, the CdTe grain size decreases as the system pressure decreases. This is consistent with the work done by Major *et al.* [82], where the number of nucleation sites increases at lower pressures, resulting in smaller grains. For this reason, the next set of experiments were performed with similar CSS parameters as those listed in Table 4.2, but the pattern of the Si(111) substrates was reduced to the nanoscale.

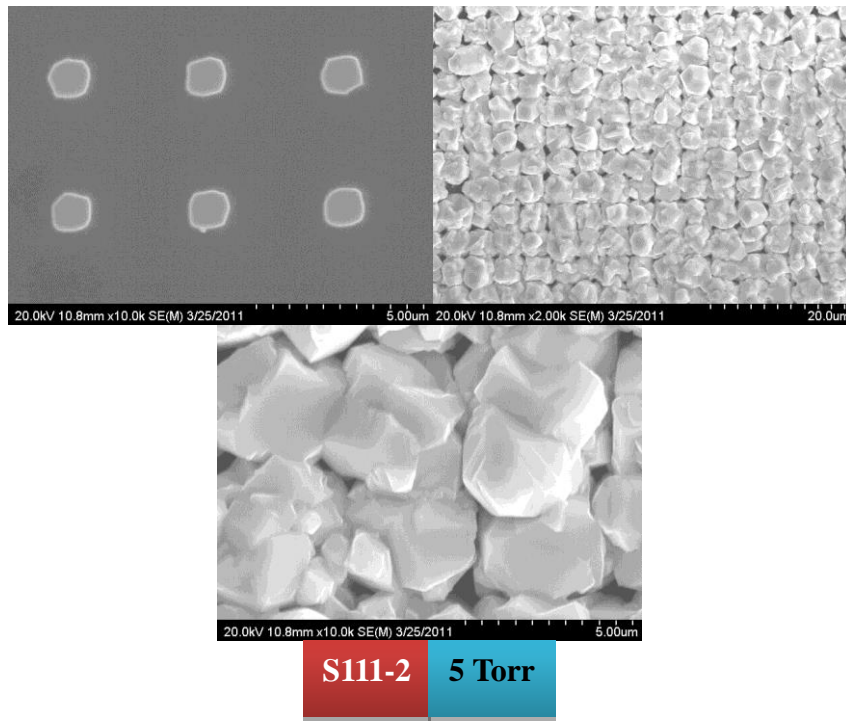


Figure 4.4. Selective CdTe Deposition on patterned Si(111) at  $T_{\text{sou}} = 550^{\circ}\text{C}$ ,  $T_{\text{sub}} = 450^{\circ}\text{C}$ , and pressure system of 5 Torr.

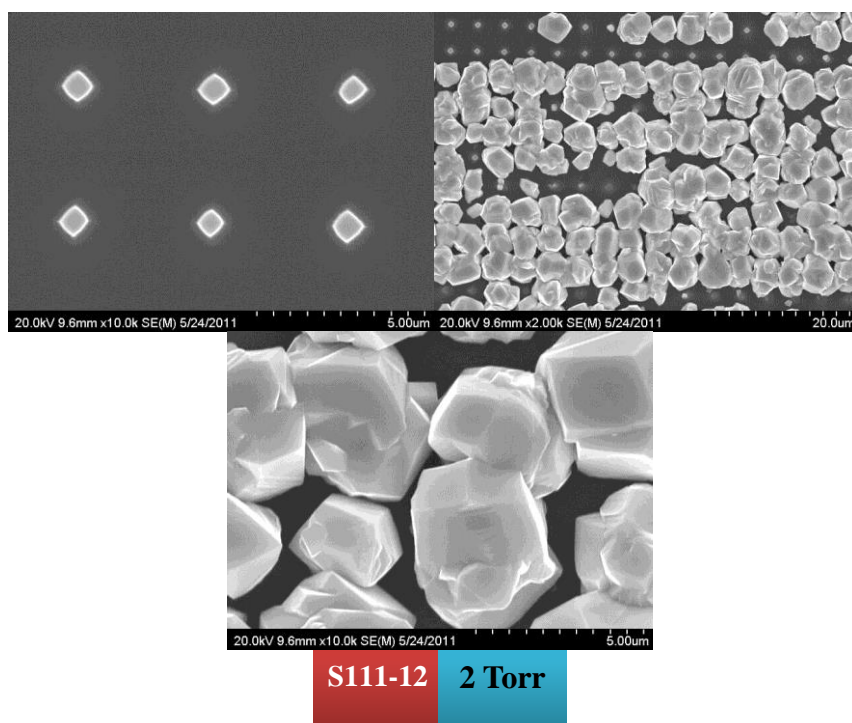


Figure 4.5. Selective CdTe Deposition on patterned Si(111) at  $T_{\text{sou}} = 550^{\circ}\text{C}$ ,  $T_{\text{sub}} = 450^{\circ}\text{C}$ , and pressure system of 2 Torr.

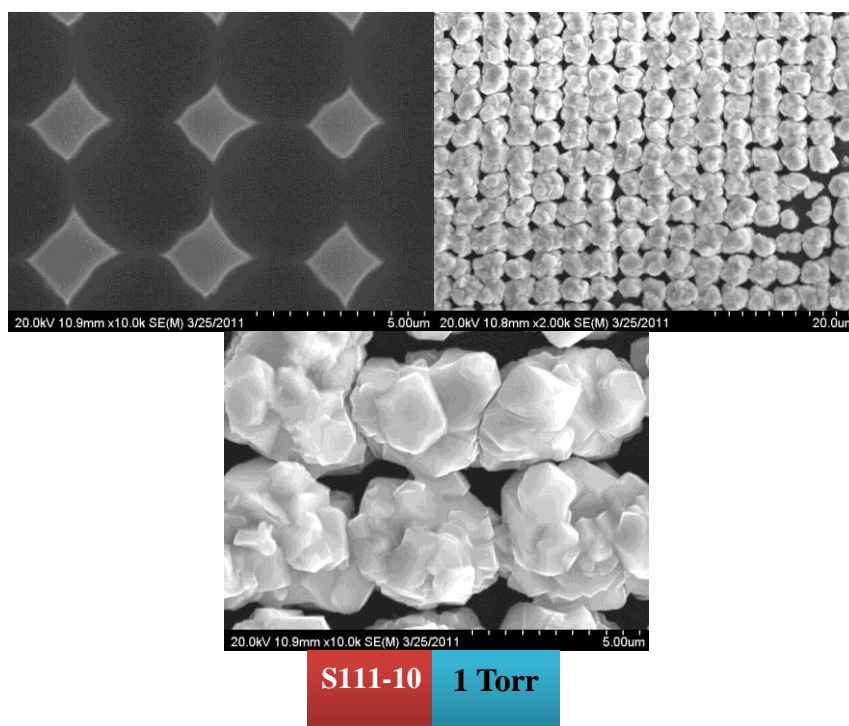


Figure 4.6. Selective CdTe Deposition on patterned Si(111) at  $T_{\text{sou}} = 550^{\circ}\text{C}$ ,  $T_{\text{sub}} = 450^{\circ}\text{C}$ , and pressure system of 1 Torr.

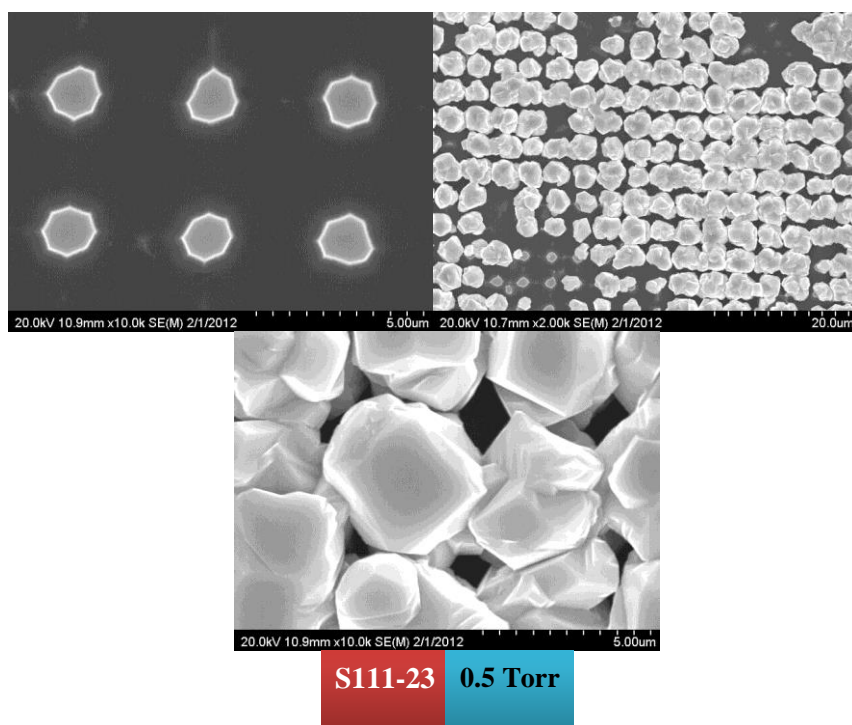


Figure 4.7. Selective CdTe Deposition on patterned Si(111) at  $T_{\text{sou}} = 550^{\circ}\text{C}$ ,  $T_{\text{sub}} = 450^{\circ}\text{C}$ , and pressure system of 0.5 Torr.

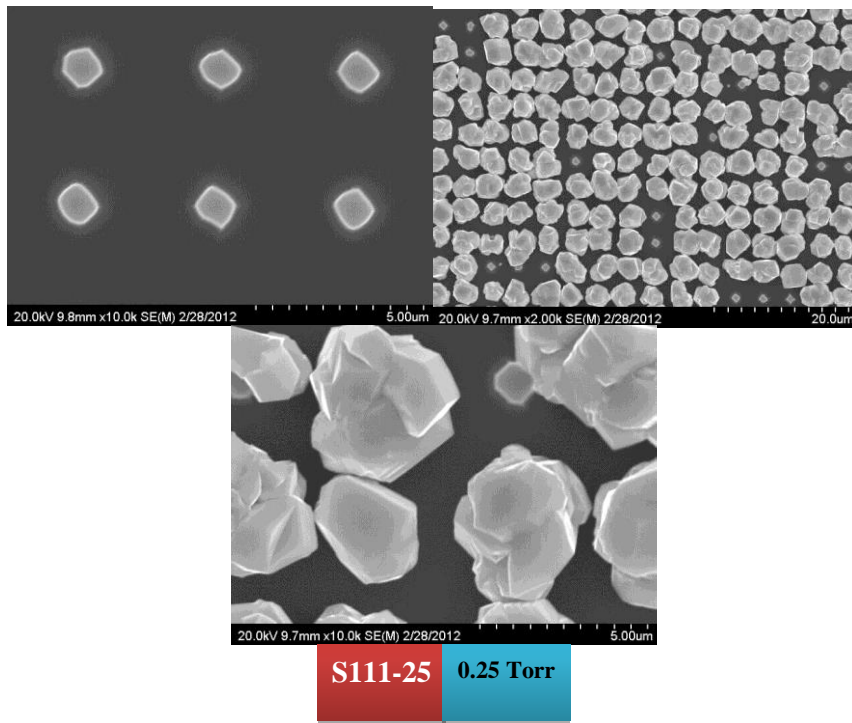


Figure 4.8. Selective CdTe Deposition on patterned Si(111) at  $T_{\text{sou}} = 550^{\circ}\text{C}$ ,  $T_{\text{sub}} = 450^{\circ}\text{C}$ , and pressure system of 0.25 Torr.

#### 4.3.2. Selective CdTe growth on Si(111) with 500 nm pattern (Set II)

The second set of experiments are similar to set I but with Si(111) substrates patterned at the nanoscale. As in the previous experiments, the reactor warm-up steps were included and the CdTe source was annealed prior to each deposition. Table 4.3 includes the results for this set as a function of temperature, pressure, and deposition time. The highest quality and most uniform growth was observed for pressures of 0.5 and 0.25 Torr, similar to set I.

Table 4.3. Summary of experiments performed on Si(111) substrates with 500 nm pattern (Set II).

Sample	Pattern Size	T <sub>sub</sub> (°C)	T <sub>sou</sub> (°C)	Pressure (Torr)	Dep. Time	Uniformity (Poor, Fair, Good)	Grain Size
S111-1	500 nm	450	550	5	5 min.	Fair	4.2 μm
S111-19	500 nm	450	550	2	5 min.	Fair	4.1 μm
S111-17.2	500 nm	450	550	0.5	5 min.	Good	4 μm
S111-15	500 nm	450	550	0.25	5 min.	Good	3.9 μm

SEM images for the samples listed in Table 4.3 are shown in Figures 4.9 through 4.12. These images include a surface view of the substrate before and after CdTe deposition. Multiple micrographs are provided for the CdTe growth at low and high magnification. For this set of experiments, all samples were patterned at the nano-scale, resulting on Si pillars of ~500 nm diameter and 2 μm pitch. As with Set I, the grain size decreased with a decrease in pressure. The last two samples performed in this set of experiments also resulted in the highest quality selective CdTe growth, consistent with the results from Set I. Figures 4.11 and 4.12 show SEM images for these two samples conducted with a system pressure of 0.50 and 0.25 Torr, respectively. For this reason, the next set of experiments using the Si(211) substrates were performed using these CSS parameters.

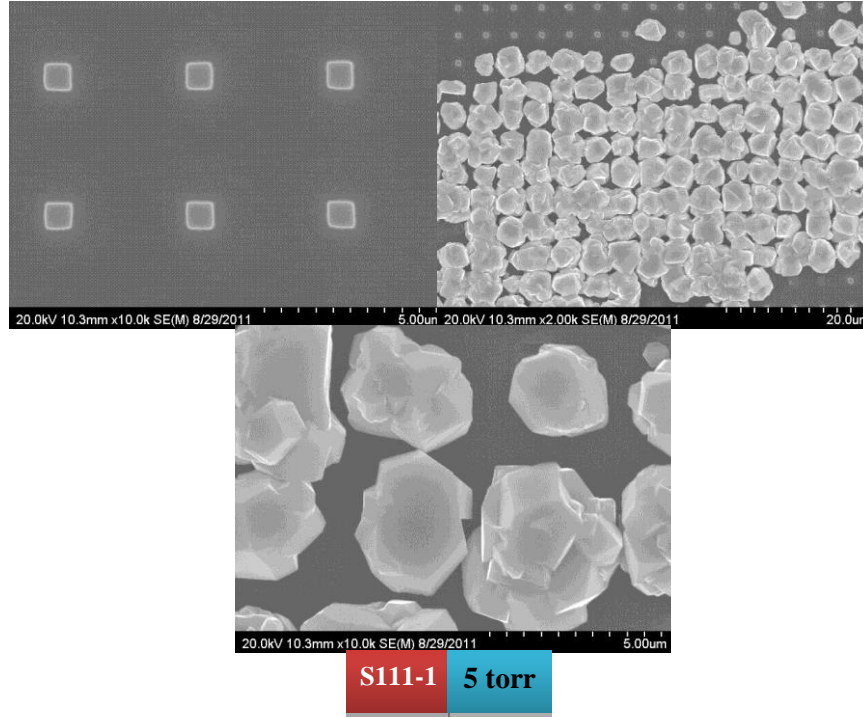


Figure 4.9. Selective CdTe Deposition on patterned Si(111) at  $T_{\text{sou}} = 550^{\circ}\text{C}$ ,  $T_{\text{sub}} = 450^{\circ}\text{C}$ , and pressure system of 5 Torr.

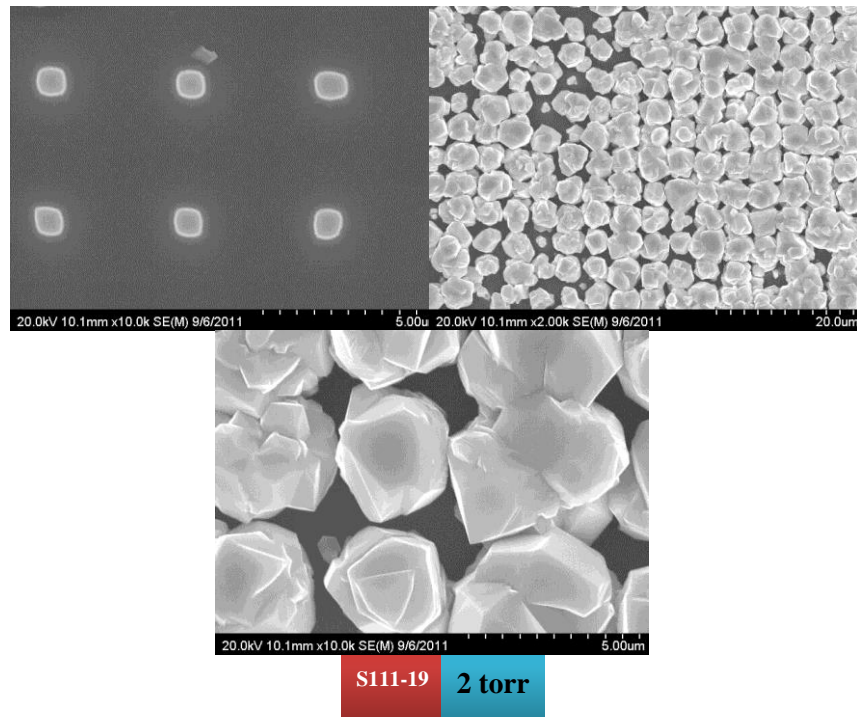


Figure 4.10. Selective CdTe Deposition on patterned Si(111) at  $T_{\text{sou}} = 550^{\circ}\text{C}$ ,  $T_{\text{sub}} = 450^{\circ}\text{C}$ , and pressure system of 2 Torr.



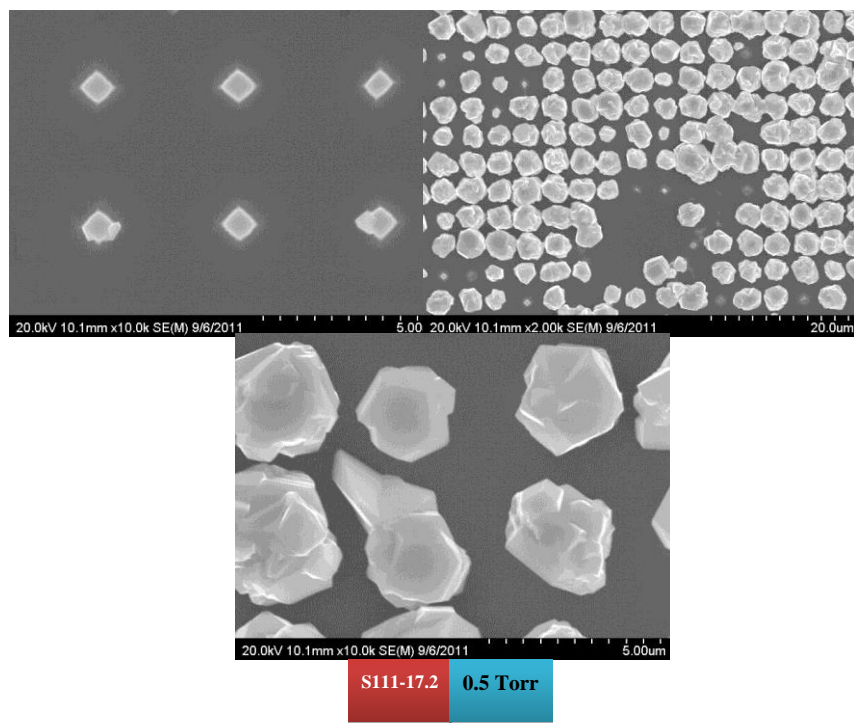


Figure 4.11. Selective CdTe Deposition on patterned Si(111) at  $T_{\text{sou}} = 550^{\circ}\text{C}$ ,  $T_{\text{sub}} = 450^{\circ}\text{C}$ , and pressure system of 0.5 Torr.

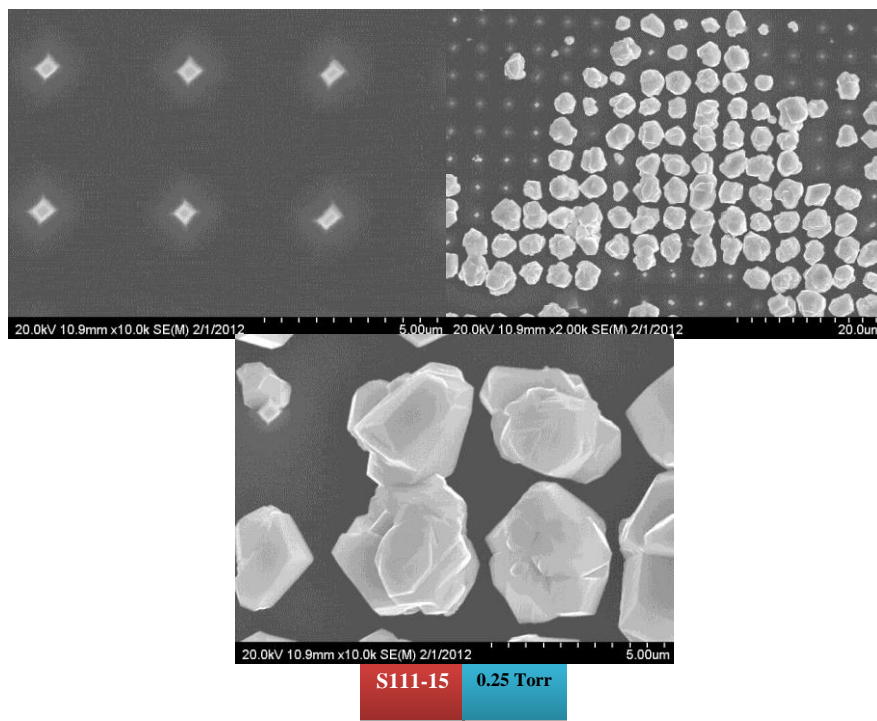


Figure 4.12. Selective CdTe Deposition on patterned Si(111) at  $T_{\text{sou}} = 550^{\circ}\text{C}$ ,  $T_{\text{sub}} = 450^{\circ}\text{C}$ , and pressure system of 0.25 Torr.

#### 4.3.3. Selective CdTe growth on Si(211) with 1 $\mu\text{m}$ pattern (Set III)

The third set of experiments was performed with Si(211) substrates patterned at the micron-scale in order to analyze the effect of the system pressure and the source temperature on the quality of the selective CdTe growth and the CdTe grain size. Reactor warm-up steps were included and the CdTe source was annealed prior to each deposition. Table 4.4 includes, pattern size, source and substrate temperatures, pressure of the system, deposition time, uniformity selective CdTe growth, and grain size for each sample. Moreover, each deposition was carried out for 5 minutes for a substrate temperature of 450°C and source temperature was vary between 550°C and 560°C. The pressure was varied between 5 – 0.5 Torr for this set of experiments, based on the results from Sets I and II. Since samples grown with pressure at 0.25 and 0.5 Torr resulted in the highest quality selective CdTe growth from experiments performed in Sets I and II, it was decided to complete the rest of the experiments in this study for Si(211) substrates with the same system pressures.

Table 4.4. Summary of experiments performed on Si(211) substrates with 1  $\mu\text{m}$  pattern (Set III).

Sample	Pattern Size	$T_{\text{sub}}$ (°C)	$T_{\text{sou}}$ (°C)	Pressure (Torr)	Dep. Time	Uniformity (Poor, Fair, Good)	Grain Size
S211-6	1 $\mu\text{m}$	450	550	0.5	5 min.	Fair	4.9 $\mu\text{m}$
S211-8	1 $\mu\text{m}$	450	560	0.5	5 min.	Fair	5 $\mu\text{m}$
S211-11	1 $\mu\text{m}$	450	550	0.25	5 min.	Good	4.6 $\mu\text{m}$
S211-12	1 $\mu\text{m}$	450	560	0.25	5 min.	Good	4.8 $\mu\text{m}$

SEM images for the samples listed in Table 4.4 are shown in Figures 4.13 through 4.16. These images include a surface view of the substrate before and after CdTe deposition. Multiple micrographs are provided for the CdTe growth at low and high magnification. For this set of experiments, all samples were patterned at the micro-scale, resulting in Si pillars of  $\sim 1 \mu\text{m}$  in diameter and  $2 \mu\text{m}$  pitch. The CdTe deposition for Sample S211-8 and S211-12 was performed for 5 minutes at  $T_{\text{sou}}=560^\circ\text{C}$  and  $T_{\text{sub}}=450^\circ\text{C}$  in order to study the effect of higher source temperature on the quality and size of the CdTe

grains. The system pressure was set to 0.50 Torr for sample S211-8 and 0.25 Torr for sample S211-12. The average grain size was 5  $\mu\text{m}$  in diameter for sample S211-8 (Fig. 4.14) and 4.6  $\mu\text{m}$  in diameter for sample S211-12 (Fig. 4.16). For samples S211-6 and S211-11, selective CdTe deposition was performed for 5 minutes at  $T_{\text{sou}}=550^\circ\text{C}$  and  $T_{\text{sub}}=450^\circ\text{C}$ , and system pressures of 0.50 Torr and 0.25 Torr, respectively. The average grain size for sample S211-6 (Figure 4.13) and S211-11 (Figure 4.15) was 4.9  $\mu\text{m}$  and was 4.8  $\mu\text{m}$  in diameter, respectively. Samples S211-6 and S211-11 in this set of experiments resulted with the best quality selective CdTe growth according to the results obtained from the morphology study of the samples using SEM characterization. Figures 4.13 and 4.16 show SEM images for these two samples for pressures of 0.50 and 0.25 Torr, respectively. According to this set of experiments, it was observed once again that the CdTe grain size decreased as the pressure was decreased. The next set of experiments were performed with the same CSS parameters, but on Si(211) substrates patterned at the nano-scale (500 nm -700 nm).

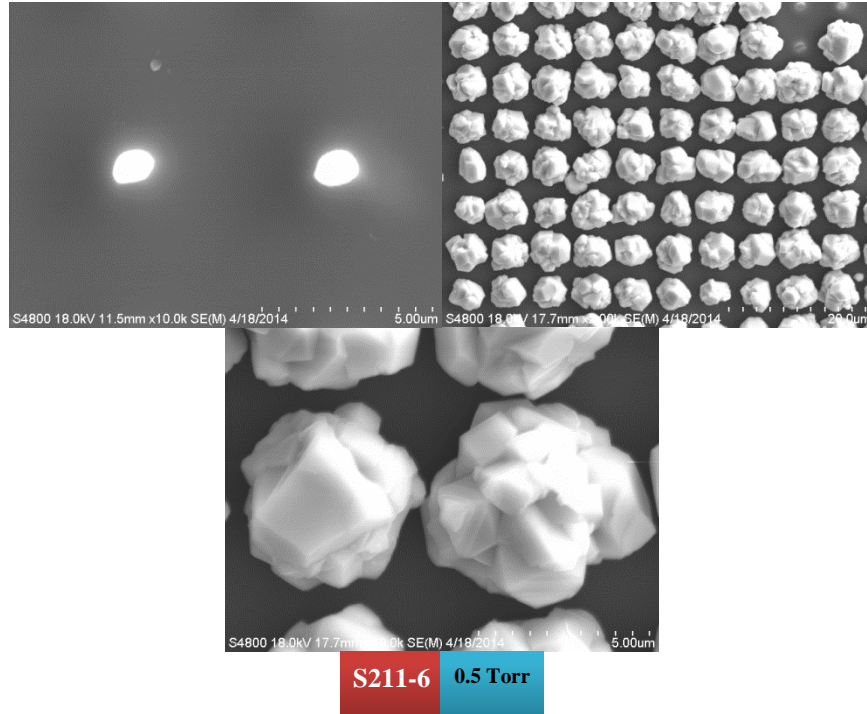


Figure 4.13. Selective CdTe Deposition on patterned Si(211) at  $T_{\text{sou}} = 550^\circ\text{C}$ ,  $T_{\text{sub}} = 450^\circ\text{C}$ , and pressure system of 0.5 Torr.



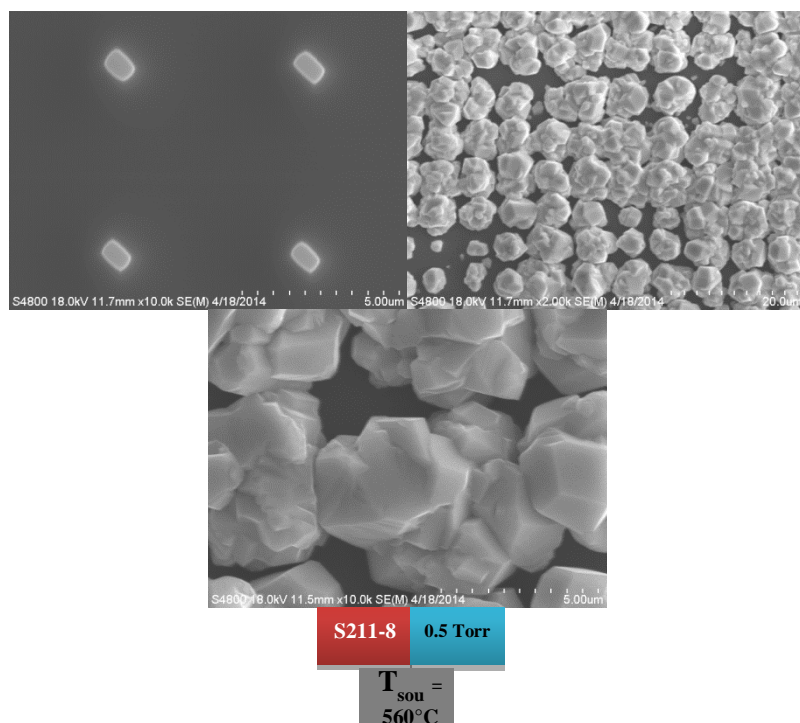


Figure 4.14. Selective CdTe Deposition on patterned Si(211) at  $T_{\text{sou}} = 560^{\circ}\text{C}$ ,  $T_{\text{sub}} = 450^{\circ}\text{C}$ , and pressure system of 0.5 Torr.

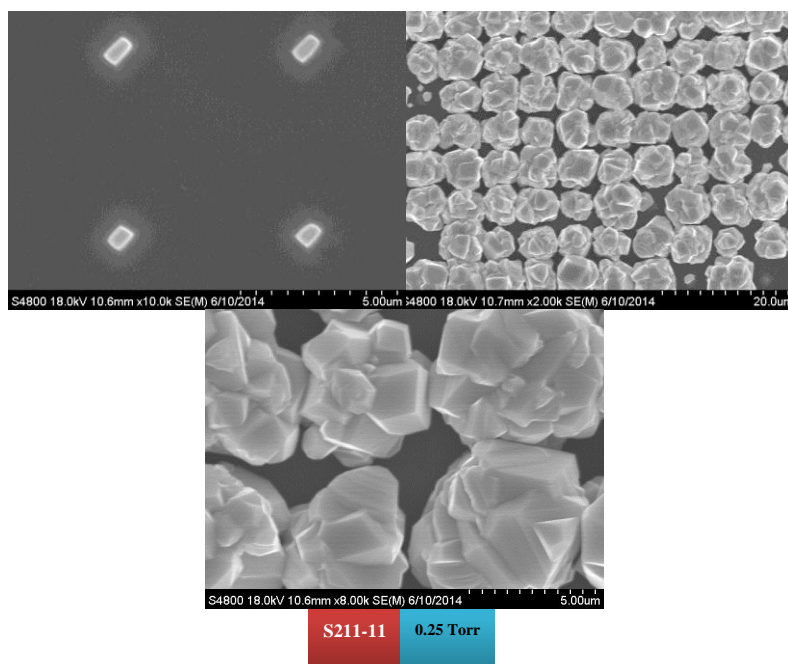


Figure 4.15. Selective CdTe Deposition on patterned Si(211) at  $T_{\text{sou}} = 550^{\circ}\text{C}$ ,  $T_{\text{sub}} = 450^{\circ}\text{C}$ , and pressure system of 0.25 Torr.

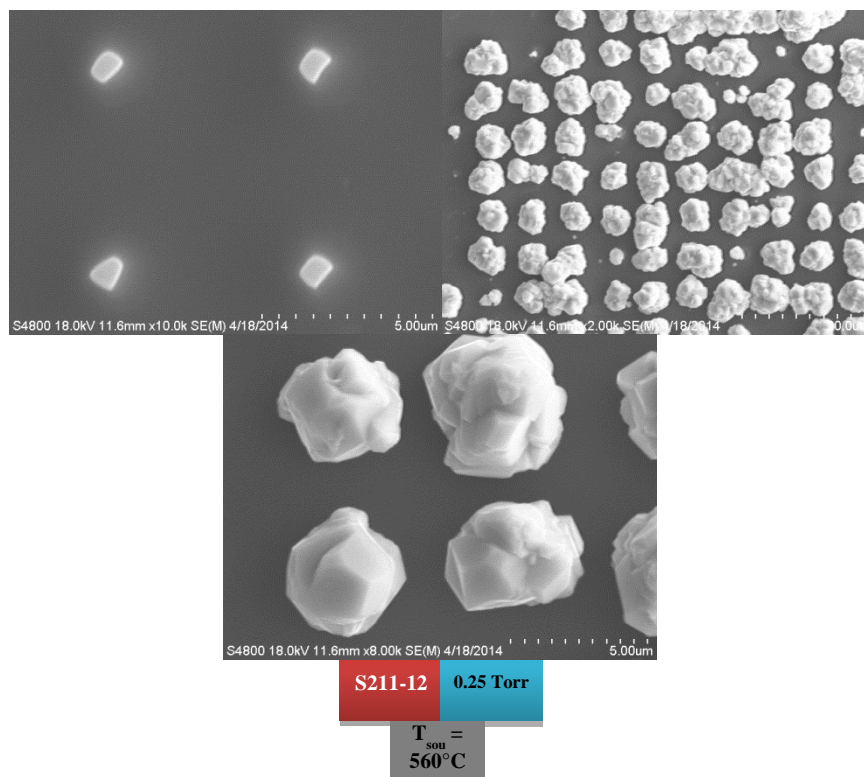


Figure 4.16. Selective CdTe Deposition on patterned Si(211) at  $T_{\text{sou}} = 560^{\circ}\text{C}$ ,  $T_{\text{sub}} = 450^{\circ}\text{C}$ , and pressure system of 0.25 Torr.

#### 4.3.4. Selective CdTe growth on Si(211) with 500-700 nm pattern (Set IV)

The fourth set of experiments consisted of selective CdTe growth on Si(211) substrates patterned at the nano-scale in order to analyze the effect of the system pressure on the quality of the selective CdTe growth and the CdTe grain size. Reactor warm-up steps were included and the CdTe source was annealed prior to each deposition. Table 4.5 includes, pattern size, source and substrate temperatures, pressure of the system, deposition time, uniformity selective CdTe growth, and grain size for each sample. Moreover, each deposition was carried out for 5 minutes for a substrate temperature of  $450^{\circ}\text{C}$  and source temperature of  $550^{\circ}\text{C}$ . The pressure system was vary between 0.50 - 0.25 Torr for this set of experiments.

Table 4.5. Summary of experiments performed on Si(211) substrates with 500-700 nm pattern (Set IV).

Sample	Pattern Size	$T_{\text{sub}}$ (°C)	$T_{\text{sou}}$ (°C)	Pressure (Torr)	Dep. Time	Uniformity (Poor, Fair, Good)	Grain Size
<b>S211-5</b>	~500 nm	450	550	<b>0.5</b>	5 min.	Good	4.2 $\mu\text{m}$
<b>S211-9</b>	~700 nm	450	550	<b>0.25</b>	5 min.	Good	4.6 $\mu\text{m}$
<b>S211-10</b>	~700 nm	450	550	<b>0.5</b>	5 min.	Good	4.7 $\mu\text{m}$

SEM images for the samples listed in Table 4.5 are shown in Figures 4.17 through 4.19. These images include a surface view of the substrate before and after CdTe deposition. Multiple micrographs are provided for the CdTe growth at low and high magnification. For this set of experiments, all samples were patterned at the nano-scale, resulting on Si pillars of ~500 - 700 nm in diameter and 2  $\mu\text{m}$  pitch. The CdTe deposition for these samples was performed for 5 minutes at  $T_{\text{sou}}=550^\circ\text{C}$  and  $T_{\text{sub}}=450^\circ\text{C}$ . The system pressure was varied between 0.25 - 0.50 Torr in order to study the effect of the system pressure on the quality and size of the CdTe grains. The average grain size was 4.2  $\mu\text{m}$  in diameter for sample S211-5 (Fig. 4.17), 4.6  $\mu\text{m}$  in diameter for sample S211-9 (Fig. 4.18) and 4.7  $\mu\text{m}$  in diameter for sample S211-10 (Fig. 4.19). Samples S211-5 and S211-10, grown at 0.5 Torr, resulted in the best quality selective CdTe growth. Figures 4.17 and 4.19 show SEM images for these two samples. According to this set of experiments, it was observed that the CdTe grain size decreased as the pressure was decreased, and the grain size increased for larger patterned samples grown at the same pressure.

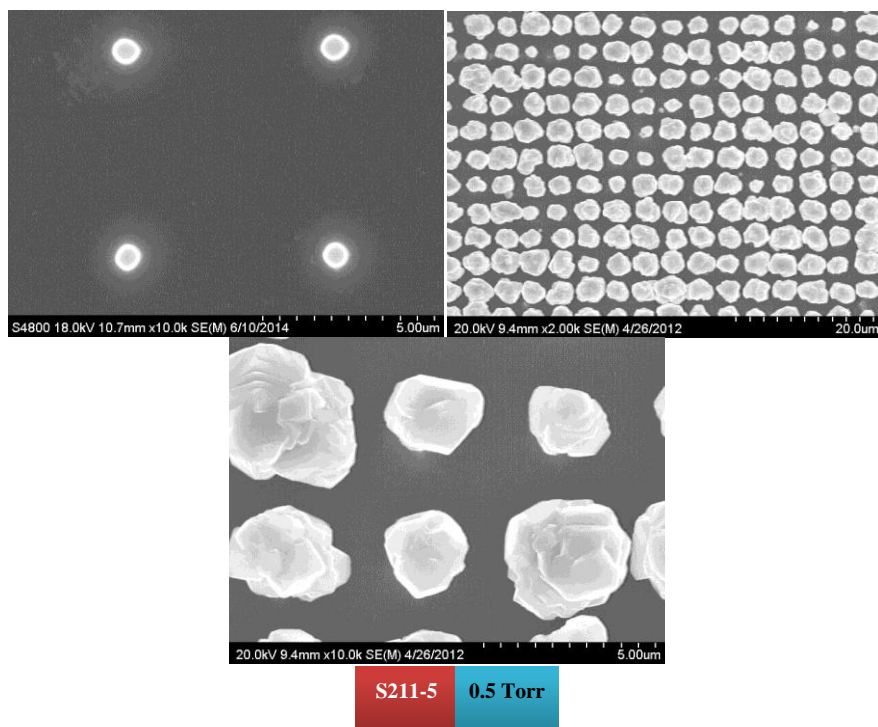


Figure 4.17. Selective CdTe Deposition on patterned Si(211) at  $T_{\text{sou}} = 550^{\circ}\text{C}$ ,  $T_{\text{sub}} = 450^{\circ}\text{C}$ , and pressure system of 0.25 Torr.

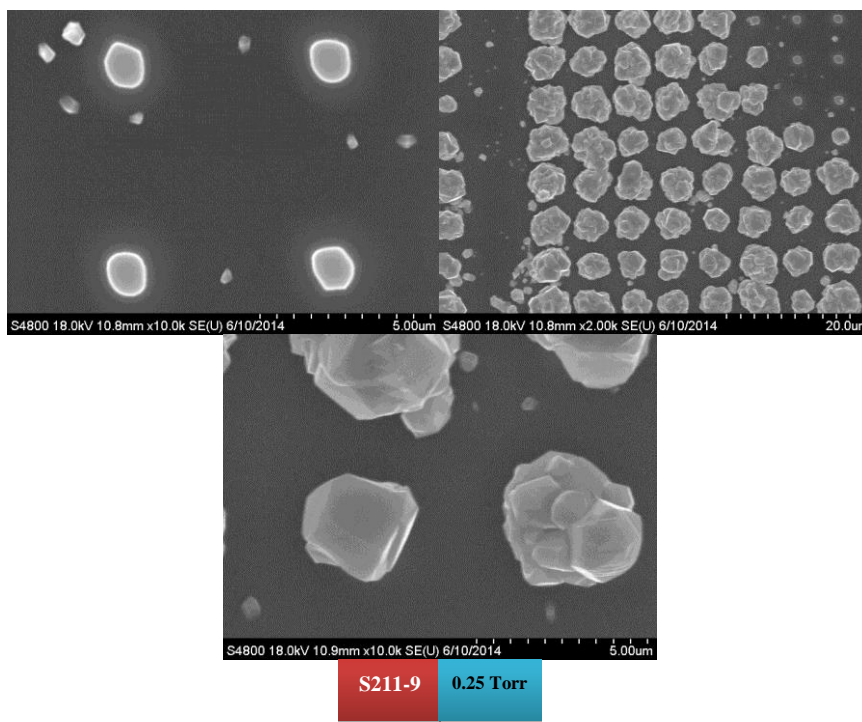


Figure 4.18. Selective CdTe Deposition on patterned Si(211) at  $T_{\text{sou}} = 550^{\circ}\text{C}$ ,  $T_{\text{sub}} = 450^{\circ}\text{C}$ , and pressure system of 0.5 Torr.

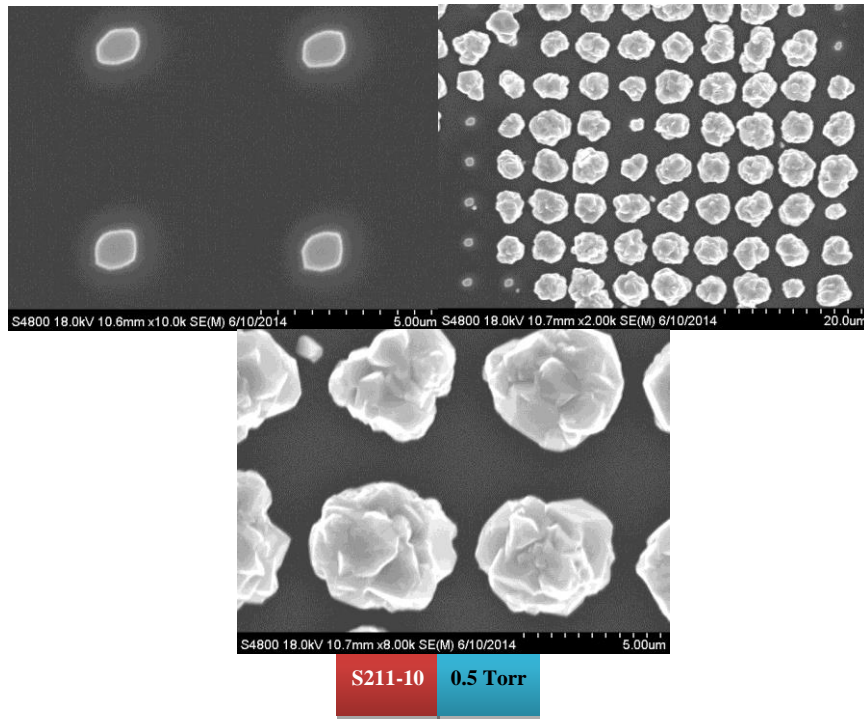


Figure 4.19. Selective CdTe Deposition on patterned Si(211) at  $T_{\text{sou}} = 550^{\circ}\text{C}$ ,  $T_{\text{sub}} = 450^{\circ}\text{C}$ , and pressure system of 0.25 Torr.

#### 4.4 QUALITY OF SELECTIVE CDTE GROWTH VIA TEM

Transmission electron microscopy (TEM) was performed for high quality CdTe/Si samples identified from the SEM morphology results of the CdTe growth on the Si(111) and Si(211) substrates. The analysis was performed in order to characterize the CdTe grain structure and orientation, along with the defects and strain at the CdTe/Si interface. TEM analysis was conducted using two modes of operation, HRTEM and diffraction mode, and these were used to identify the following structural features:

- (1) Indexing of planes on the diffraction patterns
- (2) Identification of planes on the HRTEM images
- (3) Calculation of d-spacings using the diffraction patterns and comparing these values to the theoretical values



- (4) Measurement of the misorientation angle at the CdTe/Si interface from the planes identified on the HRTEM images
- (5) Characterization of defects at the CdTe/Si interface.

#### 4.4.1. Indexing of Diffraction Patterns

Identification of the orientation of the CdTe growth and Si substrate is determined based on indexing of the CdTe and Si diffraction patterns (Refer to section 3.3.4). However, for the CdTe/Si(111) sample the Si pillar was etched away as a result of the FIB process. Figure 4.20(a) is a TEM micrograph of the CdTe grain and an indication of where the etched Si pillar should have been located. Fig. 4.20(b) is a HRTEM image of Fig. 4.20(a) rotated 50°, and Fig. 4.20(c) is the corresponding diffraction pattern of CdTe 1 grain identified in Fig. 4.20(b). The diffraction patterns for the CdTe/Si(211) growth are shown in Fig. 4.21(a) for Si and Fig. 4.21(b) for CdTe. These diffraction patterns are indexed based on the crystallographic structure of Si (diamond cubic) and CdTe (zinc blende).

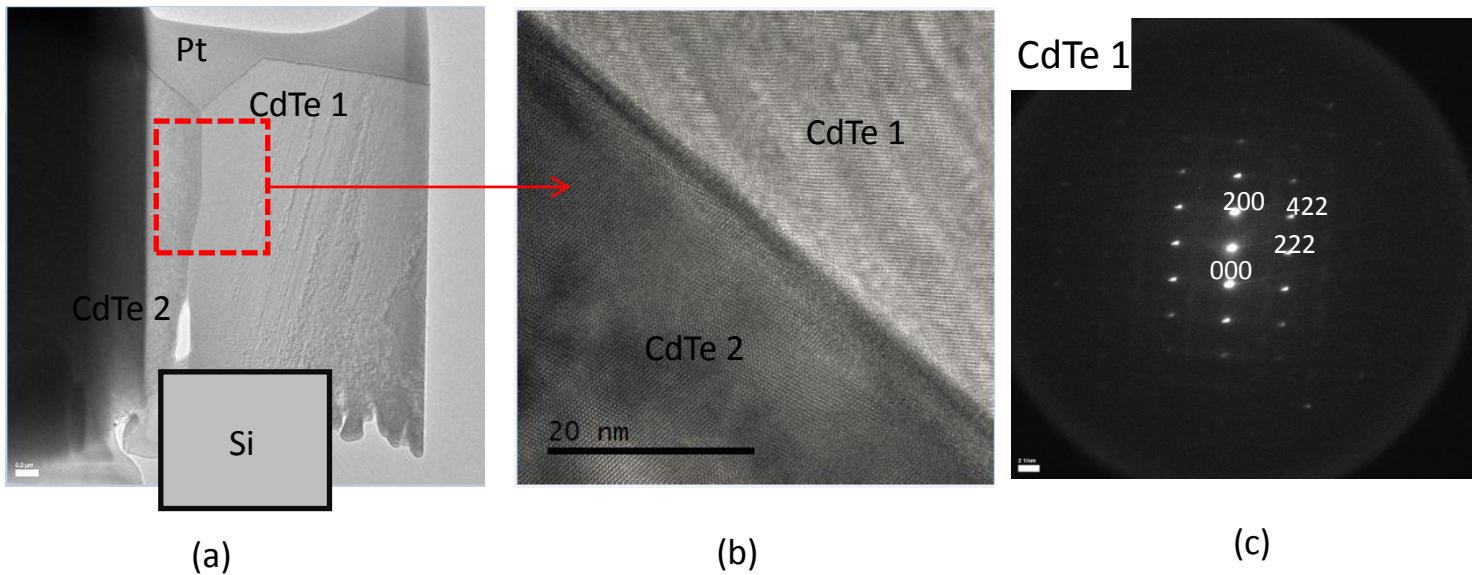


Figure 4.20. (a) Cross-sectional TEM image of CdTe grain grown on Si(111) (etched away during FIB process), (b) HRTEM image of CdTe grain rotated 50°, and (c) diffraction pattern of CdTe 1 grain.

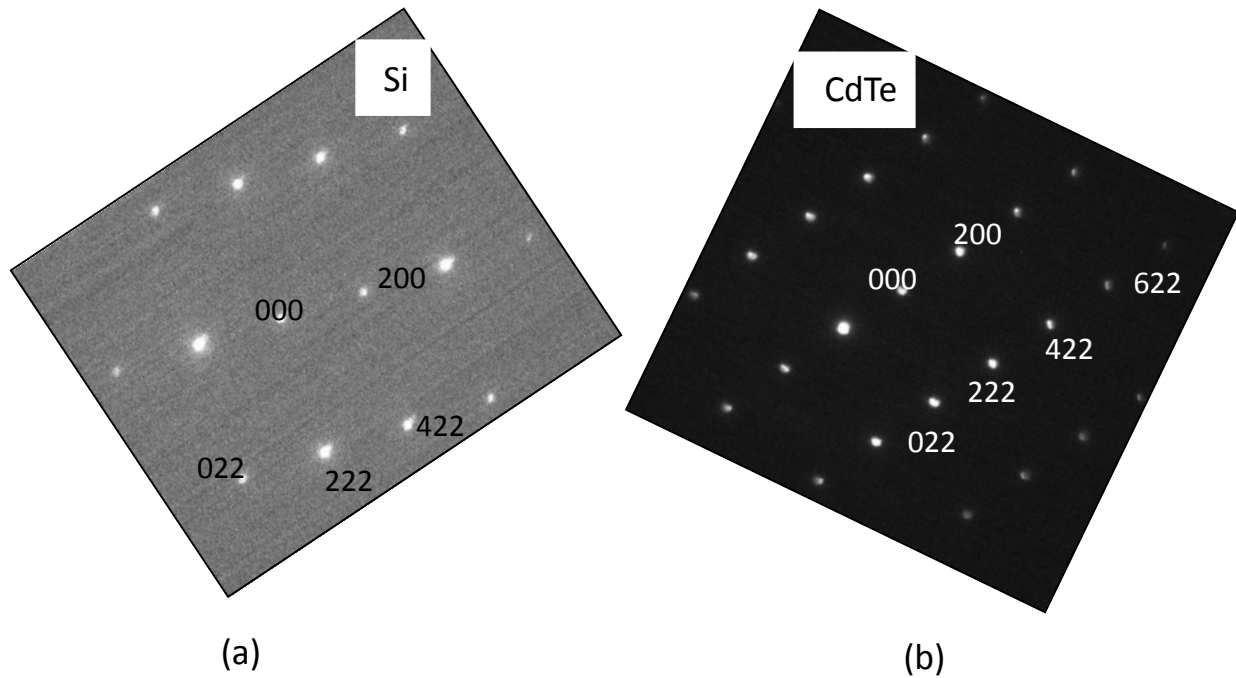


Figure 4.21. Diffraction patterns for (a) Si (211) substrate and (b) CdTe grain grown on this substrate.

#### 4.4.2. Identification of Planes on HRTEM Images

The identification of the lattice planes on the HRTEM images is determined by comparing the HRTEM image with its corresponding diffraction patterns. For example, vector drawn between a transmitted beam and a given (xyz) spot on the diffraction pattern corresponds to the [xyz] direction on the HRTEM image, and the (xyz) planes on the HRTEM image lie perpendicular or normal to this direction. The normal is transposed onto the HRTEM to identify the corresponding planes. Figure 4.22(a) is a HRTEM image illustrating only the boundary of two CdTe grains grown on top of a Si(111) pillar, since the Si pillar was etched away(Fig. 4.20(a)). Figure 4.22(b) is the HRTEM image of the CdTe/Si(211) interface. The (200), (222), and (422) planes are indexed for each material.

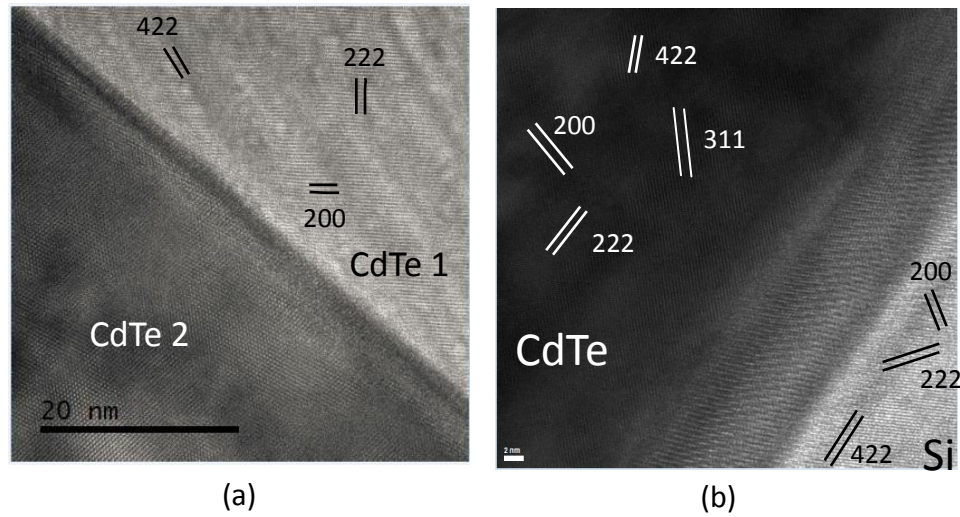


Figure 4.22. HRTEM images of (a) CdTe grains from Si(111) substrate and (b) CdTe/Si(211) interface.

#### 4.4.3. Lattice Spacings Analysis

The lattice spacings (d-spacings) are calculated directly from the diffraction patterns corresponding to Si and CdTe growth using Eqs. 3.1 and 3.2 from the diffraction pattern and bulk material, respectively. If the measured d-spacing from the diffraction pattern does not agree with the bulk (theoretical) d-spacing then the material is under strain. The most common reason is due to the film being tetragonally distorted to accommodate strain [87]. Table 4.6 and includes the d-spacings of the planes identified from the diffraction pattern for CdTe grains grown on the Si(111) pillar and Table 4.7 includes the d-spacings for both the CdTe grain and the Si(211) pillar.



Table 4.6 Comparison of d-spacings from diffraction pattern and bulk material (theoretical) for Si(111) pillar.

<b>d-spacings (111)</b>				
Planes	Si	CdTe	Diffraction $d_{hkl} = \lambda L/R$	Theoretical $d_{hkl} = a/\sqrt{h^2 + k^2 + l^2}$
(200)		X	2.89 Å	3.24 Å
(222)		X	1.37 Å	1.87 Å
(422)		X	1.14 Å	1.32 Å

Table 4.7 Comparison of d-spacings from diffraction pattern and bulk material (theoretical) for CdTe grain and Si(211) substrate.

<b>d-spacings (211)</b>				
Planes	Si	CdTe	Diffraction $d_{hkl} = \lambda L/R$	Theoretical $d_{hkl} = a/\sqrt{h^2 + k^2 + l^2}$
(200)	X		1.76 Å	2.71 Å
(222)	X		1.14 Å	1.56 Å
(422)	X		0.95 Å	1.10 Å
(200)		X	3.75 Å	3.24 Å
(222)		X	2.3 Å	1.87 Å
(422)		X	1.79 Å	1.32 Å

#### 4.4.4. Misorientation at CdTe/Si Interface

The misorientation angle at the CdTe/Si interface was measured based on the misorientation of the planes between CdTe and Si on the HRTEM images. Based on the orientation of the planes in Fig. 4.23, the (222) plane is oriented approximately 55° from the surface of the pillar, which is a (111) surface. Since the (222) plane is parallel to the (111), then the CdTe grain has a misorientation of 55° with respect to the Si pillar. For the CdTe grain grown on the Si(111) pillar, the misorientation angle at

the interface was determined by assuming that the Si pillar sketched in Figs. 4.20(a) and 4.23, has a (111) surface orientation. Figure 4.24 is the HRTEM image of the CdTe grain on Si(211) with the associated indexed diffraction patterns and planes. From Fig. 4.24, a misorientation of  $35^\circ$  is observed at the interface between CdTe and Si(211).

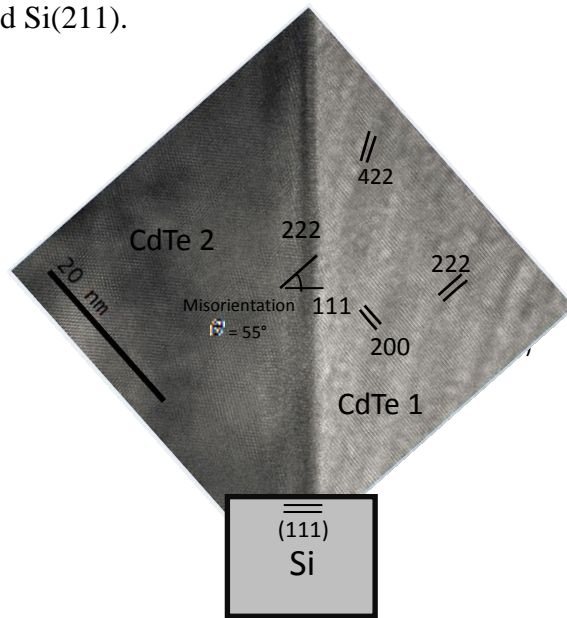


Figure 4.23. Estimated misorientation of CdTe grain grown on Si(111) based on approximation of where Si pillar was located.

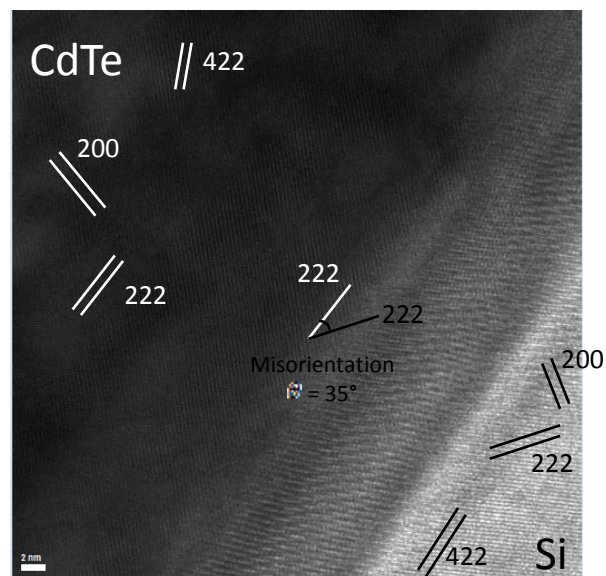


Figure 4.24. HRTEM image of CdTe grain on Si(211) pillar, with corresponding indexed diffraction pattern and planes.

#### 4.4.5. Structural Defects at CdTe/Si Interface

The HRTEM images were used to analyze the growth and structure of the CdTe/Si interface, which is an important factor that impacts the final material quality for the subsequent growth of HgCdTe. Samples S211-11 was characterized using this technique in order to analyze more closely the crystallography structure of the Si substrate, the CdTe grain and the CdTe/Si interface at the atomic scale. The HRTEM image obtained of this sample reveals the presence of misorientation growth in the CdTe layers and CdTe/Si interface in reference to the substrate. Figure 4.25 shows a HRTEM image at low and high magnification at the interface for sample S211-11, where the misorientation observed at the CdTe/Si interface is approximately  $35^\circ$ . From the high magnification image, stacking faults are present within the CdTe/Si interface in order to accommodate the lattice mismatch.

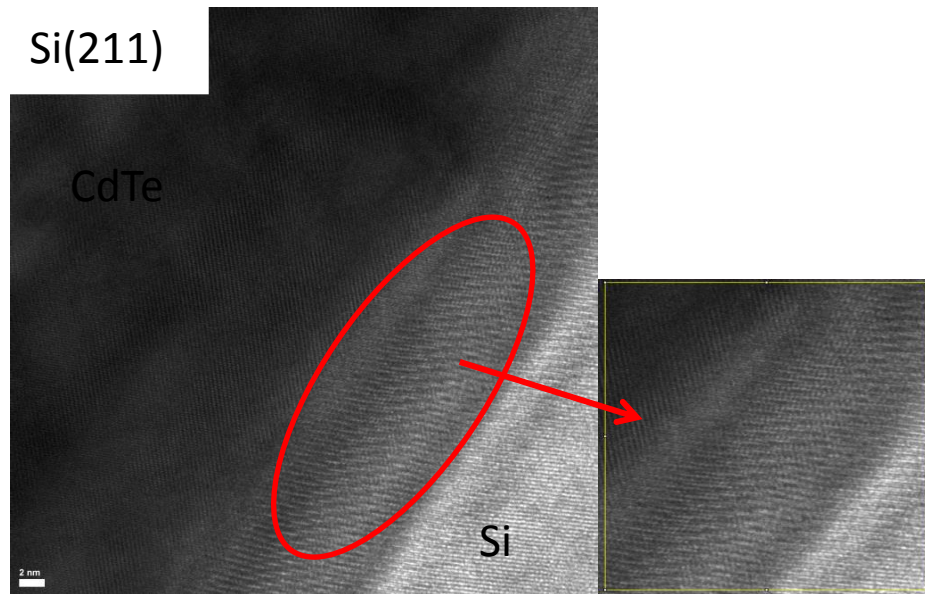


Figure 4.25. HRTEM images of CdTe/Si(211) interface at low and high magnification.

#### 4.4.6. Comparison to Similar Work

The best selective CdTe growth obtained in this study was for sample SS211-11, where selective CdTe growth was on a 1  $\mu\text{m}$  patterned Si(211) sample at 550°C source temperature, 450°C substrate temperature, 5 minute CdTe deposition time, and 0.5 Torr pressure. This sample was compared to two studies performed by Diaz [3] and Escobedo [30], where selective CdTe growth was achieved on a Si(100) substrate and a Si(211) substrate, respectively. Diaz achieved selective CdTe growth at 550°C source temperature, 450°C substrate temperature, 5 minute CdTe growth and pressure system of 5 Torr. Escobedo achieved selective CdTe growth for a deposition time of 15 minutes at similar growth temperatures. In Escobedo's work CdTe is grown on CdTe windows, where the CdTe was grown on Si(211) on top of a thin ZnTe buffer layer, where both the CdTe windows and ZnTe were grown using MBE, and the selective growth was by CSS. In Diaz's earlier work, CdTe was deposited on Si(100) using the CSS ;also without a mask layer [3,30].

Figure 4.26(a-f) includes a comparison of the selective growth resulting from the three studies. Fig. 4.26(a) and (b) are low and high magnification SEM and TEM images of Escobedo's work, respectively, showing single CdTe grains deposited on patterned CdTe/Si(211) substrates. The CdTe growth resulted in 1 $\mu\text{m}$  in diameter high faceted CdTe grains. TEM analysis confirmed that these were single crystal CdTe grains with twins. Figure 4.26(c) and (d) are high magnification SEM and HRTEM images of Diaz' work, respectively, showing CdTe grains deposited on patterned CdTe/Si(100) substrates. TEM analysis confirmed the evolving misorientation between the substrate and the film. Nevertheless, defects such as facets and stacking faults can be clearly seen in CdTe grains (Figure 4.26 (c)). Figure 4.26 (e) and (f) are high magnification SEM and TEM images, respectively, of selective growth achieved on Si(211) substrates in this study. The SEM results obtained for selective CdTe grown on Si(100), Si(111), and Si(211) prove that selective CdTe growth can be achieve without the use of a mask via the CSS technique. The TEM results obtained for the four studies demonstrate that structural defects such as twins and stacking faults are present in the CdTe grains and at the interface. In

addition, TEM results obtained for studies done by Diaz' and this dissertation show the evolving misorientation at the CdTe/Si interface.

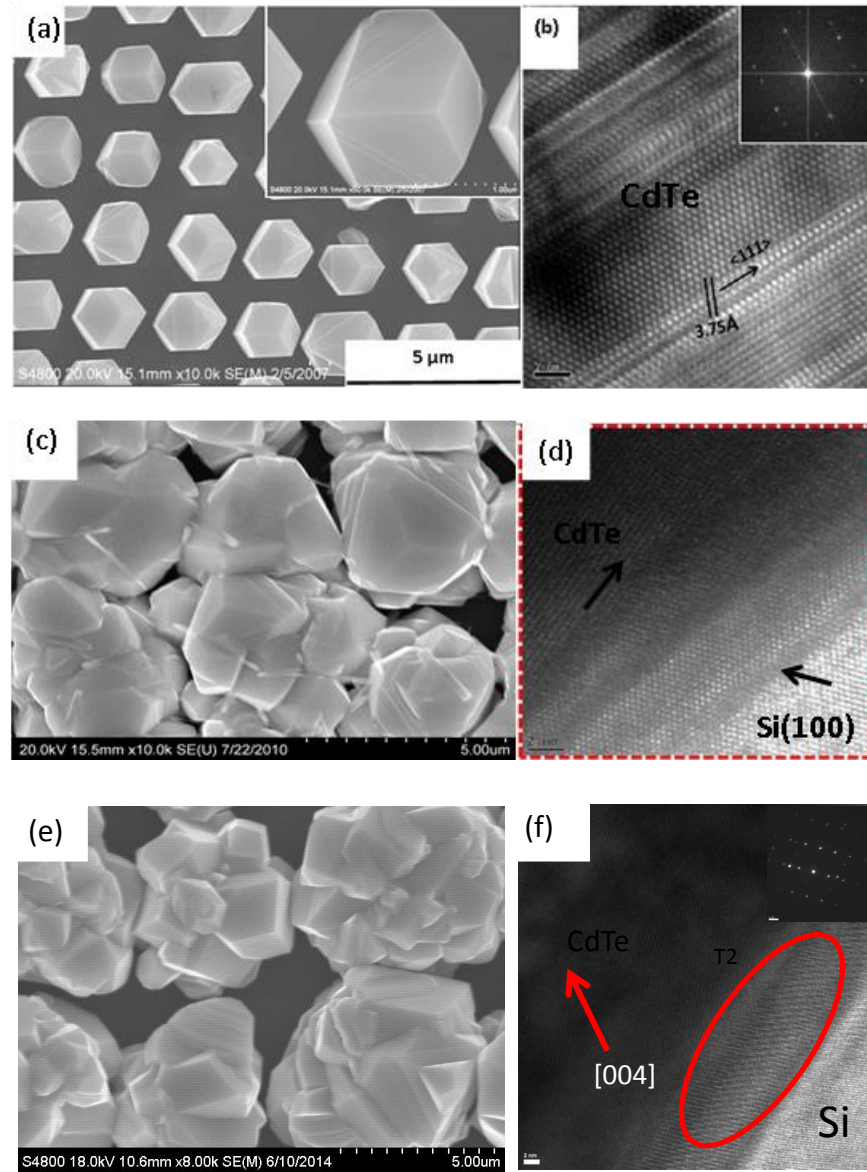


Figure 4.26. SEM and TEM images of Selective CdTe Growth (a-b) on CdTe/Si(211) substrate (Escobedo's work) (c-d) on Si(100) substrate (Diaz' work), and (e-f) on Si(211) substrate [3,30].

## **Chapter 5: Conclusions**

The set of experiments performed in this study consisted of the selective CdTe growth on patterned Si(111) and Si(211) substrates, where selectivity was achieved for all source and substrate temperatures, and pressures. Selective CdTe grains were observed for source temperatures of 550°C and substrate temperatures of 450°C. The CdTe grain size was observed to be proportional to the pressure. A summary of the results obtained in this study will be explained.

### **5.1 SELECTIVE GROWTH OF CdTe ON Si(111) AND Si(211) SUBSTRATES VIA CSS**

Several set of experiments were performed to achieve a high quality CdTe/Si(111) film via CSS technique. These set of experiments consisted of varying the source and substrate temperature, as well as the pressure. The following can be concluded from the results obtained:

- 1) CdTe selectivity was achieved for all substrate and source temperatures used in this study.
- 2) Selective growth of CdTe on Si(111) and Si(211) substrates was achieved without the use of a mask.
- 3) The growth rate is proportional to the source temperature.
- 4) As the source temperature is increased, the film morphology improved.
- 5) CdTe grains with smooth surface were achieved for source temperature of 550°C, substrate temperature of 450°C, 0.25Torr pressure, and 5 minute growth.
- 6) Annealing the source improves the quality and repeatability of the CdTe films grown on Si(111) and Si(211) substrates.
- 7) Increasing the source temperature increases the grain size.
- 8) The CdTe grain size increases and uniformity of selective CdTe growth improves as the deposition time increased.

9) Decreasing the pattern size decreases the grain size.

### **5.3 TEM ANALYSIS OF CdTe GRAINS AND CdTe/Si INTERFACE FOR Si(111) AND Si(211) SUBSTRATES**

TEM analysis was performed for two high quality samples obtained from the set of experiments completed in this study. Sample Si(111) and Si(211) were analyzed using diffraction patterns of the Si substrate and CdTe film in order to identify the planes on the material and calculate the lattice spacings on the substrate and film corresponding to the HRTEM image. In addition, the misorientation angle at the CdTe/Si interface was determined. The following can be concluded from the results obtained for both samples:

- 1) Most of the d-spacing values obtained from both, Si(111) and Si(211) substrates, are in line with the d-spacings calculated from the theoretical equation.
- 2) The misorientation angle at the CdTe/Si(111) interface ( $55^\circ$ ) is greater than the misorientation of the CdTe/Si(211) interface ( $35^\circ$ ).
- 3) The HRTEM images for the CdTe/Si(211) film show structural defects such as misorientation at the CdTe/Si interface, which are due to the lattice mismatch (19%) between CdTe and Si.

Overall, the results presented in this dissertation demonstrate that CdTe can be selectively deposited on patterned Si(111) and Si(211) substrates resulting in high quality films for the subsequent growth of HgCdTe films. Especially important, is that this was accomplished without the use of a mask. In order to improve the quality of CdTe growth even further, it is recommended that the size of the pillars be reduced further, to less than 200 nm.

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## **Curriculum Vita**

Aryzbe Najera was born on November 7, 1984 in Cd. Juarez, Chihuahua, the oldest daughter of Silvia Vences and Venancio Diaz. She moved to El Paso, Texas when she was 11 years old, without knowing a word of English. In May 2003 she graduated from Montwood High School in the ten top percent of her class out of 650 students, and with the National Honor Society honors. She started her professional career as an Electrical and Computer Engineer at the University of Texas at El Paso (UTEP) on August 2003. In May 2008, she earned her Bachelor's of Science in Electrical and Computer Engineering, and enrolled in the UTEP graduate school in Fall 2008. As a graduate student, she became a member of the NanoMIL group at UTEP and obtained a position as a research assistant. Being a research assistant gave her a great experience in her field, semiconductor devices, and the opportunity to expose her work in national conferences as wells as working with other research assistants from other fields. Also, she had the opportunity to work as a tutor with the GEAR UP organization at Jefferson High school, helping freshman students with their mathematic courses. In January 2010, she was awarded the National Science Foundation (NSF) Bridge to the Doctorate Fellowship, which supported her financially to finish her Master's career and continue with her Ph.D. In August 2013, she was awarded the UTEP Graduate School Scholarship, which supported her financially to complete her Ph.D. degree. In October 2013, she had the opportunity to start working as an Instructor of Electronics Engineering at Western Technical College, where she obtained a permanent Faculty position on January 2014.

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