2016-01-01

CdTe Doped With Zn Grown On Si(111) And Si(211) Using The Closed Space Sublimation Method

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Dedication

I dedicate this paper to my friends and family

Who have supported me through this process

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by

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DISSERTATION

Presented to the Faculty of the Graduate School of

The University of Texas at El Paso

in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

Department of Electrical and Computer Engineering

THE UNIVERSITY OF TEXAS AT EL PASO

August 2016

Acknowledgements

I would like to thank Dr. Quinones for her support and guidance through obtaining my PhD. I would like to thank Tony James for is help with the E-Beam tool at CINT. I would like to thank John Nogan for is help with the Plasma Lab and other tools at CINT. I would like to thank Dr. Bernal for the help with the Cryo-TEM in the Chemistry department at UTEP. Dr. Palard for the help with the TEM at UT Austin. Dr. Cooke for letting me use the SEM at NMSU.

Abstract

Cadmium telluride (CdTe) doped with zinc (Zn) has been used for the fabrication of X-ray imaging devices. CdTe allows the device to have the same image quality at a lower X-ray dose. When silicon is used as a substrate for CdTe growth, this reduces the cost and allows the readout circuitry to be fabricated on the same substrate. However, material quality and device performance needs to be addressed since the lattice parameters of CdTe (6.482 Å) and Si (5.431 Å) result in a 19% lattice mismatch.

In this work, CdTe doped with Zn is deposited on Si (211) and Si (111) substrates by the closed-space sublimation (CSS) technique. The CSS method has an advantage over other techniques in terms of cost and growth rate, but represents a challenge when growing high quality films. The nanoheteroepitaxy (NHE) technique makes it possible to grow CdTe on Si substrates with fewer defects at the CdTe/Si interface and in the resulting epilayer. Electron beam lithography is used to pattern three different pillar diameters (200 nm, 100 nm, and 50 nm) on Si substrates (Si(211) and Si(111)), and two different pitch to diameter ratios (p/d=3 and p/d=2) to examine the growth of CdTe doped with 5 and 10 percent Zn.

Scanning electron microscopy (SEM) is used to examine the morphology of the CdTe growth and X-ray diffraction (XRD) is used to identify the orientation of the film and the quality of the structure of the CdTe film doped with 5% Zn. TEM characterization is used to examine the planar structure at the interface, the misorientation at interface and the type of defects in the CdTe film growth. SEM results indicate when the pitch/diameter pattern ratio is decreased from 3 to 2, the morphology of the CdTe growth is improved. As expected and confirmed with XRD data, the quality improves as the pattern diameter is reduced, especially when Zn doping is increased from 5% to 10%. Transmission electron microscopy (TEM) is used to study the

CdTe/Si interface and the resulting misorientation of the CdTe/Si interface, ranges from 0.2˚ to 1.2˚.

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Chapter 1: Introduction

Cadmium telluride (CdTe) has been a promising semiconductor material for X-ray detector applications since the early 1970's [1]. The high Z value of CdTe results in a high quantum efficiency, which allows the detector to operate from 10 keV to 500 keV [1]. CdTe X-ray devices have emerged as a top material that outperform conventional scintillators, as a result of a high bandgap of 1.44eV, high resistivity, and its ability to operate at room temperature [1]. This allows the device to have high count rates, high-energy resolution, and linear energy response during operation [2]. However, the trapping of charge carriers caused by defects in CdTe causes incomplete charge collection that jeopardizes detector operation [3].

High spatial resolution is needed for medical and security industries and CdTe detectors have the required spatial resolution [4, 5, 6]. CdTe detectors can be used in industrial non-destructive evaluations and homeland security where X-ray detectors detect concealed material [7]. CdTe detectors have a wide dynamic range and high contrast resolution that can be used for real-time high quality images, and require less dosing than other X-ray detectors [6]. CdTe doped with Zn would have a border impact on x-ray imaging detectors. A higher stopping power for photons, which makes the device more sensitive to X-rays. CdTe doped with Zn would be ideal for medical applications, as a result of its high spectral and spatial resolution, which results in a higher image quality. The lower intensity X-rays would be ideal for medical use.

The properties of the CdTe are changed when it is doped with Zn. The concentration of Zn can vary from 5 to 25 percent. This is ideal for X-ray detector applications, because it results in an even larger bandgap, which increases its resistivity, and improves its performance at room temperature (compared to undoped CdTe) [2, 1, 3]. The presence of Zn in CdTe changes the energy

required to form intrinsic defects in the surrounding atoms [3]. The addition of Zn results in Zn-Te bonds that are shorter and stronger than Cd-Te bonds. This strengthens the lattice and raises the energy that is necessary to create defects in the structure of the material [3]. In addition, as the concentration of Zn increases defects present in the material are less mobile through the structure. Currently the need for large CdTe wafers is needed for X-ray devices. The wafers need to be single crystal and can cost $500 or more. Defects such as tellurium antisite and cadmium vacancies are prevalent in larger wafers. The use of silicon (Si) as a substrate can reduce these drawbacks, and lower the cost, since Si wafers are available in larger sizes.

The lattice mismatch between CdTe and Si ranges from 12% to 19%, depending on the percent of Zn doping [8]. Zn in CdTe will help reduce the lattice mismatch and the amount of defects created at the interface between the two materials [2, 8, 35, 41].

The nanoheteroepitaxy method is another way to help reduce the defects that form at the interface as a result of the lattice mismatch between CdTe and Si. Nanoheteroepitaxy often employs the use of a patterned oxide mask layer to help with selective growth [9]. The CSS method is implemented for deposition of CdTe on Si substrates, for its high growth rate of 1μm/hr or higher. The CSS is versatile in terms of materials that can be used and the cost of operating the equipment is much lower than other methods. The nanoheteroepitaxy method and Zn doping of CdTe will be used to reduce the misorientation between the CdTe and Si interface.

Chapter 2: CdTe X-Ray Detector

2.1 CdTe X-ray Imaging Applications

Semiconductor X-ray imaging devices are used in military, national security, and in biomedical applications. Important properties of semiconductor detectors are fast image collection, operation at room temperature, and high spectral and spatial resolution [10].

CdTe has become a popular material for X-ray imaging applications since the 1980's when it replaced scintillators [13]. Silicon (Si), germanium (Ge), and CdTe are the top materials used for direct semiconductor detectors. CdTe has an advantage over Si and Ge detectors, since it is more sensitive and requires less dosing. The most common configurations for CdTe X-ray imaging detectors are pixelated and segmented crystal array detectors [5]. The pixel detectors have better spatial resolution and energy resolution over segmented crystal array detectors [5].

The performance of CdTe detectors can be improved by reducing the amount of defects, such as cadmium vacancies [2]. In addition, doping with Zn helps reduce cadmium vacancies in CdTe and improve the performance, compared to undoped CdTe. This allows for better detection of the incident X-rays and improves the spectral and spatial resolution. Doping with Zn increases the bandgap and resistivity, and this allows the X-ray detector to operate at room temperature, requiring no cooling system. The ideal resistivity for CdTe doped with Zn is between 10^9 to 10^{11} Ωcm, with a bandgap between 1.5 eV and 2.26 eV (depending on the percent of Zn). The increase of both resistivity and the bandgap reduces the dark current [19]. These detectors operate within the 60°-150°C range, but can still be sensitive at higher temperatures [16].

The key performance requirements for an X-ray imaging devices are:

(1) High quality material (low number of defects in CdTe, around 3 x 10^{-3} cm^{-2}) and a uniform charge transport throughout the device [17].

(2) Low device noise.

(3) Large breakdown voltage [16].

2.2 Device Physics

CdTe doped with zinc (Zn) is a very promising material for X-ray imaging applications. The most common concentration of Zn used for X-ray imaging detectors is 10% [20]. Cadmium zinc telluride (CZT) is an alloy of cadmium telluride (CdTe) and zinc telluride (ZnTe), while CdTe doped with Zn has Zn atoms introduced into the CdTe lattice. The Horizontal Bridgeman (HB) method is used to grow CdTe doped with Zn, and this method produces a material with defects, such as cadmium vacancies and tellurium antisites. This method is the most common way to grow CdTe, and results in low yield, with more defects in larger wafers [1]. Improving the growth method by reducing the defects at the interface, will reduce the device noise and breakdown voltage.

The material properties of CdTe doped with Zn change the properties of an X-ray imaging detector. Doping CdTe with 10% Zn results in a bandgap of 1.57eV along with a high resistivity of $8x10^{10}$ Ω cm. The larger bandgap also results in a decrease in leakage current to less than $1x10^{-9}$ A/cm^2 at room temperature of 21°C [21, 10]. In order to transport a large amount of carriers, a high dopant concentration and a high lifetime is required. CdTe with 10% Zn has an electron and hole carrier range of $\mu_e\tau_e \approx 1x10^{-3}$ to $1x10^{-2}cm^2/V$ and $\mu_h\tau_h \approx 1x10^{-5}$ cm^2/V, respectively, along with a resistivity of $1x10^{10}$ Ω cm [1, 10, 21, 23]. When the concentration of Zn is dropped to 4%, the resistivity drops to $5x10^9$ Ωcm [24]. The carrier range is important and affects the charge collection of these carriers and the higher this value, the better the device is

able to operate. When the Zn concentration is dropped to 5%, the electron and hole carrier range decreases to $\mu_e\tau_e \approx 2x10^{-4}cm^2/V$ and $\mu_h\tau_h \approx 3x10^{-6}cm^2/V$, respectively [19].

When 1% Zn is added to CdTe, there is about a 0.5% shift in the position of the photo peak [14]. CdTe doped with Zn has a good stopping power for incoming photons as a result of its high density of 5.8 g/cm^3. A high density signifies that the photon is more likely to interact with an atom and create charge carriers. This high density implies high quantum efficiency (number of charge carriers collected by the detector) for photons with energy less than 180 keV [18]. An array of detectors gives a wider range of photon energies that can be detected by the material. A 3 mm thick layer of CdTe doped with Zn has a stopping efficiency of 90% at 120 keV.

Defects in the material reduce the charge-carrier trapping since these traps reduce carrier mobility and this affects device performance. Charge carrier trapping is when defects cause charge carriers to recombine and thus decrease mobility. Instead of the charge-carriers being detected by the readout chip, they are trapped in defects in the material. The effects of charge-carrier trapping can also be reduced by applying reverse bias on the CdTe doped with Zn detector. Carrier trapping can also be reduced by changing the structure of the device, and by reducing the pixel size below the thickness of the pixel [22]. This reduces the chances of recombination, since the charge carriers travel a shorter distance through the material.

High amount of defects can also result in high noise and low device performance as a result of carriers being trapped. Dark current is the direct result of defects in the semiconductor material that interact with charge carriers. The dark current must be reduced to less than 10 pA per mm^2 for X-ray imaging detectors [19]. For a CZT detector, the leakage current is about 4 nA at room temperature, but can increase to 30 nA [27, 1]. The surface of polycrystalline CdTe doped with Zn is passivated to help reduce the dark current [19].

2.3 Detector Structure and Operation

There are a number of important device physics processes that occur during the operation of X-Ray imaging devices. X-ray imaging detectors operate in photocurrent mode. CdTe detectors can detect X-ray intensity and incident x-ray photon energy for imaging [4]. Each pixel of the detector converts a photon into an electron-hole pair that has an energy that is proportional to the incident photon. This charge is stored in a capacitor associated with each pixel and is readout by the Application-Specific Integrated Circuit (ASIC) chip. The ASIC circuitry interprets the signals of the electron-hole pairs into a digital image [19].

The readout chip consists of a signal-integrated transistor that operates in the electron collection mode or negative signal [26]. The MOSFETs are used in the readout circuit as amplifiers and can have multiple number of channels for image recreation. [15, 14, 22]. The use of ASIC circuity for the readout chip can be manufactured on the same Si wafer as the detector, allowing for a more compact design. CdTe doped with Zn detectors have an operating range of 10 KeV to 1 MeV [14]. The percent of zinc in CdTe determines the required energy needed to create electron-hole pairs in the material.

A Schottky barrier, a blocking electrode, and p-n junctions are common contacts used to connect the readout chip to the CdTe doped with Zn pixel [16]. A readout duration of 1.28 μs is required in order for the CdTe doped with Zn detector to acquire a good image, with a photon counting readout cycle of approximately 1.25 μs. The device is divided into a number of binary groups of pixels, so that high-speed electronics are not required [25]. A uniform spatial response is needed in order to reduce the fixed-pattern noise that is present in other detectors [25]. Charge trapping caused by defects in CdTe doped with Zn grains can result in decreased electric field in the detector [25]. The electric field helps move electron and hole carriers. This causes a low

carrier life time and results in noise at the readout chip. It is important to have a high electric field to help carriers travel to the electrodes and then to be detected by the readout chip.

X-ray imaging devices are characterized by pixel size, pitch, and electrode material. The most common structure for a CdTe doped with Zn X-ray imaging detector is a pixelated detector, which is composed of many small pixels, that capture incoming X-ray photons. The amount of pixels varies depending on the application. Each pixel can range from 2.5 cm^2 to 100 mm^2 [22, 25, 14, 16, 1]. The pitch between pixels can vary from 0.6 mm to 1.25 mm [14, 15]. The thickness of the detector can vary from 2 mm to 15 mm [16, 25]. CdTe X-ray imaging devices have a pixel structure that has 0.2 mm spacing between each pixel [11, 12].

X-ray detectors have a full area electrode on the top and bottom, to connect the detector material to the readout chip, much like solar cells. The common materials that are used for the electrodes are platinum (Pt), gold (Au), titanium (Ti), and indium (In) [25, 22]. These materials help form a Schottky barrier at the interface between the detector material and the electrodes [10].

There are three factors that contribute to the sensitivity of a detector:

(1) The amount of radiation that is absorbed into the material from the incident radiation that generates electron-hole pairs, or the quantum efficiency of the material;

(2) The amount of charge that is created by the electron-hole pairs; and

(3) The amount of charge carriers that are collected/read by the readout chip, characterized by the carrier drift mobility and lifetime [19].

A CdTe doped with Zn X-ray imaging detector is characterized by (1) a high speed that minimizes errors, (2) a high count rate of 50-100 million counts/s/mm^2, (3) good uniform response, and (4) long term stability [16].

These ensure an X-ray imaging detector with good spectral and special resolution, which results in the detector requiring less X-rays from the source to form the same quality image. These performance requirements above can be met by the material properties of CdTe doped with Zn.

The way X-ray imaging detectors are rated is by their energy resolution. The detector energy resolution can be obtained from this Fig. 2.1 by measuring the FWHM at a peak. The energy resolution can be improved by changing the detector structure and the readout chip structure.

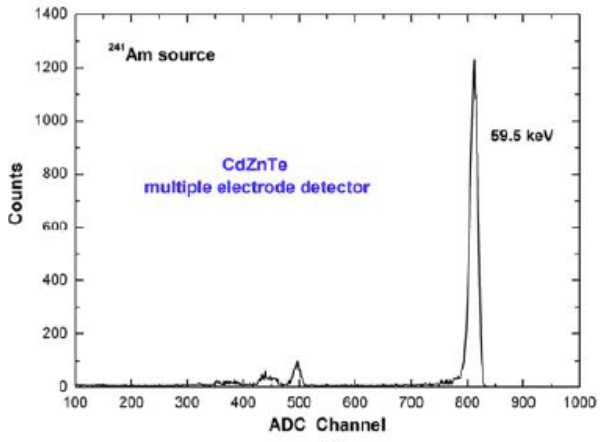


FIGURE 2.1: GRAPH SHOWING COUNTS VS CHANNELS TO FIND ENERGY RESOLUTION OF THE DETECTOR [21].

Cesium (^{137}Cs) and Americium (^{241} Am) are two common elements used to find the energy resolution of X-ray imaging detectors. Energy resolution for a device is important because it validates how well a device will perform. The smaller the energy resolution, the better the quality of the image, and the less the detector is needed to be exposed to the X-ray source to obtain an image. Table 2.1 includes a summary of the energy resolution of the fabricated devices

and the source used for verification. The higher the energy resolution the better quality of imaging the device is able to obtain.

TABLE 2.1: ENERGY RESOLUTION OF A FABRICATED DETECTOR AND THE SOURCE USED FOR CALIBRATION.

Energy Resolution FWHM	Energy in keV	Spectrum Material	Source
13.9keV	662	^{137}Cs	[5]
2.7%	59.5	^{241}Am	[21]
3.42keV	60	^{137}Cs	[1]
5.6keV	662	^{137}Cs	[1]

2.4 CdTe Growth on Si Substrates

Cadmium telluride (CdTe) planar growth on silicon (Si) is grown for X-ray detector applications. Common methods used to grow these materials are closed space sublimation (CSS), molecular beam epitaxy (MBE), and metalorganic chemical vapor deposition (MOCVD). High quality growth has been achieved using these methods, which results in fewer defects, such as cadmium vacancies, tellurium antisite and twins at the interface, leading to improved device performance. These methods can also be used for growth of high quality CdTe growth doped with Zn. The following examples illustrate the type of CdTe growth that has been achieved on a variety of Si substrates.

In a study by Escobedo et al., CdTe is deposited on Si (211) using the CSS method, where the source temperature is 530˚C, and the substrate temperature is 350˚C [28]. A mask of Si_3N_4 is used to successfully achieve growth in the windows of the mask. The CdTe grains grow selectively in the open widows using Si_3N_4 (Fig. 2.2). The CdTe grains grown in the window have excellent vertical growth compared to the grains grown on the mask. The quality of the epitaxial growth on the windows has a rough surface.

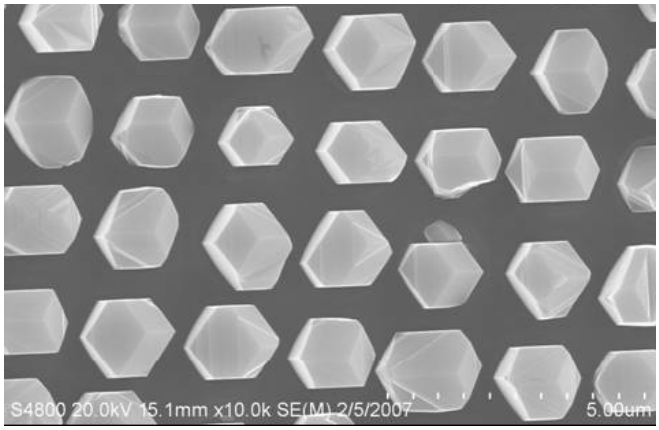


FIGURE 2.2: IMAGE OF CDTE GROWN SELECTIVELY ON SI(211) WITH A SI_3N_4 MASK AT A SOURCE TEMPERATURE OF 530˚C [28].

Diaz et al. achieved selective CdTe growth on Si(100) substrates patterned with 1 μm to 500 nm pillars by using the CSS method [29]. This growth is achieved for source temperatures 530˚ between 560˚C and substrate temperatures between 440˚ and 450˚C. The resulting average grain size for CdTe is 3.37 μm for a Si pillar diameter of 500 nm and 3.46 μm for a Si pillar diameter of 1μm. There is a small difference in grain size between the CdTe growth on pillar diameters of 500 nm and 1 μm. The highest quality growth is shown in Fig. 2.3 for a source temperature of 550˚C and a substrate temperature of 450˚C. This study demonstrates that it is possible to obtain selective growth on Si without a mask layer. The growth quality is similar for

the 500 nm and 1 μm pillar diameters, with some grains having a smooth flat surface. Transmission electron microscopy (TEM) analysis is used to view the orientation and quality of the growth at the CdTe/Si(100) interface for work done by Diaz. The grain that is imaged in Fig. 2.4 has two sub-grains misoriented at 35˚ and 32˚. Twins are also visible in both sub-grains and at the interface between CdTe and Si, along with stacking faults.

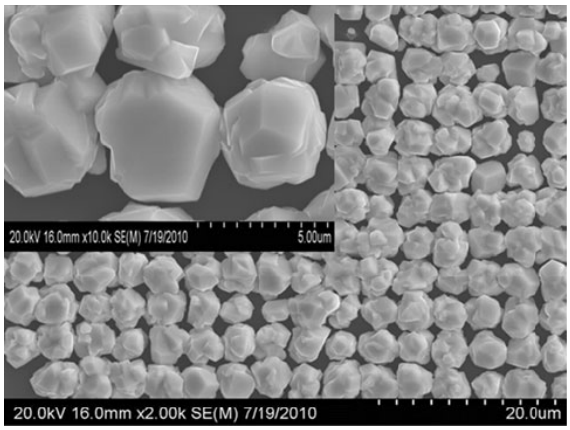


FIGURE 2.3: CDTE GROWTH ON SI (100) AT A SOURCE TEMPERATURE OF 550˚C AND A SUBSTRATE TEMPERATURE OF 450˚C [29].

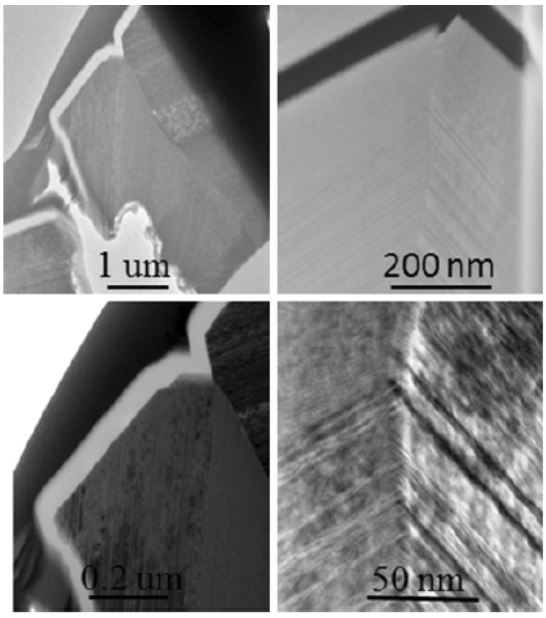


FIGURE: 2.4: CDTE GRWON SELECTIVLY ON SI(211) SUBSSTRATE WITH FACETS AND STACKING FAULTS ORIENTATION [31].

CdTe is grown on Si (211) by Wang et al. using the MBE method for a temperature range between 280˚ and 295˚C [30]. In this study, the Si(211) orientation is used to help reduce the misorientation at the interface. In addition, a thin 2.5 nm ZnTe (a=0.61 nm) buffer layer is used to help reduce the lattice mismatch of 19% between Si (a=0.543 nm) and CdTe (a=0.648). Misorientation is observed in the growth of CdTe toward the (111) orientation and ranged from 0˚ to 10˚. This study shows that the misorientation decreases between CdTe and Si with the use of a ZnTe buffer layer on Si (211). The FWHM for this growth is 83 arcsec.

Zhao et al. also used the MBE method to deposit CdTe on Si(211) with a ZnTe buffer layer [31]. Stacking faults and twins, are identified by the TEM at the interface and propagate 50 nm into the CdTe layer (Fig. 2.5). The draw back is using ZnTe as a buffer layer is that Zn atoms diffuse into the CdTe layer, and affects the growth quality.

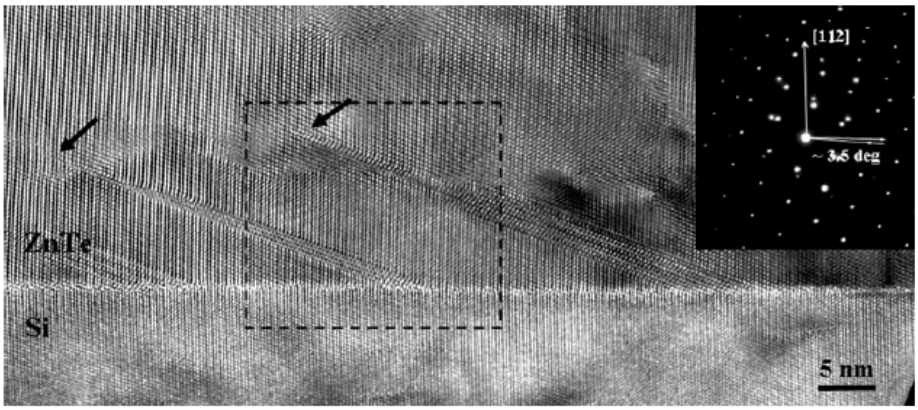


FIGURE 2.5: TWINS ARE BE OBSERVED NEAR THE INTERFACE FOR CDTE GROWTH ON SI (111) ORIENTATION [31].

CdTe is grown on Si(001), Si(211) and Si(111) substrates by Smith et al. using the MBE method [32]. The growth temperature in this study is 300˚C and a 2 nm ZnTe buffer layer is used. CdTe growth on Si(001) results in {111} lamellar twins which grow from the interface to the surface. It is observed that if the misorientation angle is between 4˚ and 10˚, the twin defects propagate through the entire epilayer to the surface. If the misorientation angle is larger the twins only propagate 1 μm to 2 μm in the epilayer. Twins can be seen propagating 100 nm away from the interface in the CdTe film shown in Fig. 2.6. The defect density at the surface of the CdTe film is $3x10^5$ cm^{-2}. When the growth temperature of the ZnTe buffer layer is increased, the twins propagate to the surface of the epitaxial layer. The twins propagate a short distance for CdTe grown on Si (211), while the twins propagate to the surface for CdTe grown on Si (001). CdTe grown on Si (001) results in a FWHM of 230 arcsec for the CdTe (422) peak. CdTe grown on Si (111) results in a FWHM of 56 arcsec from the CdTe (333) peak.

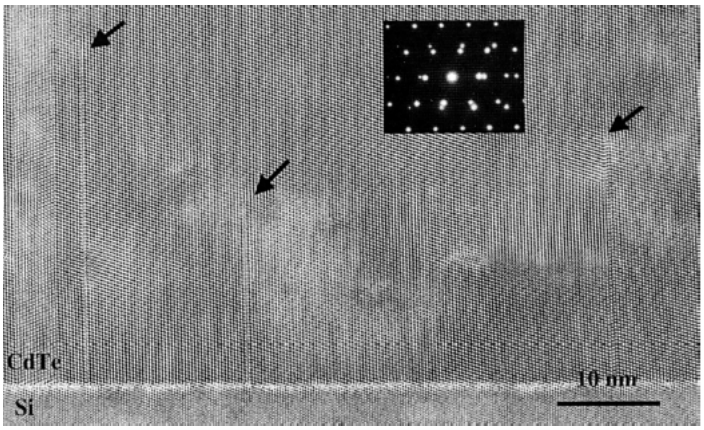


FIGURE 2.6: CDTE GROWTH ON SI(211) SUBSTRATE, WITH TWINS PROPAGATING FROM THE INTERFACE [32].

The MOCVD method is used by Kim et al. to deposit CdTe on Si (211) [33]. When the growth temperature is less than 450˚C, the CdTe growth is observed to be polycrystalline. As the temperature is increased to 500˚C, the CdTe layer quality is observed to be single crystal. Twins are present in the 500˚C grown layer, and have an orientation of (111). The surface of the CdTe layer includes (111) terrace planes and (100) step planes. The CdTe growth has a CdTe(331) dominant orientation and the intensity of this peak increases as the temperature is increased.

The MBE method is used by Rujirawat et al. to deposit CdTe on Si (211) [34]. The deposition occurs at 300˚C for CdTe. When the ZnTe buffer layer temperature is increased higher than 220˚C, the XRD data shows a single peak for CdTe(133). At temperatures lower than 300˚C, the CdTe (211) and CdTe (133) peaks are dominant, and the CdTe (211) peak has a FWHM of 74 arcsec. CdTe has a 2˚ to 3˚ misorientation at lower temperatures and a FWHM greater than 300 arcsec [34]. Etch pit density analysis shows a defect density at the surface of the epitaxial layer of 1.5×10^5 cm^{-2}. TEM analysis at the interface shows vertical twins present, which only propagate 100 nm into the epitaxial layer.

In summary, the best method for CdTe growth on Si substrates has been the MBE method. In order to be characterized as high quality growth, CdTe needs to have a FWHM of less than 100 arcsecs and one clear dominant peak. CdTe growth using the CSS method needs to be improved in order to act as a seeding layer. A FWHM of less than 100 arcsec needs to be achieved for this method to be widely used in industrial applications. Both CSS and MBE growth methods for planar growth have twins at the interface, but the twins in the MBE method propagate a shorter distance. The quality of growth for the CSS can be improved by using the Si(211) orientation the substrate.

2.5 CdTe Doped with Zn Growth

2.5.1 Effect of Zn on CdTe Structure

The addition of Zn to CdTe has an effect on the properties, structure, and defects in CdTe. Zn is an ideal dopant for CdTe, since it is an isoelectronic element and has a low segregation coefficient of 1.3 to 1.4. A low segregation coefficient means that it can easily be distributed through the CdTe material during the growth. This allows the Zn atoms to be more evenly distributed in the CdTe substrate.

Zn atoms help to reduce the etch pit density in CdTe substrates [35]. CdTe doped with Zn forms a zinc blend structure, with two face centered cubic lattices that are offset by one quarter diagonally from each other. Cd or Zn atoms occupy one sub-lattice and Te atoms occupy the other sub-lattice, as shown in Fig. 2.7 [36]. This is referred to as a FCC Bravais lattice [36]. When CdTe is doped with Zn, Cd atoms are randomly substituted by Zn atoms. Adding Zn to CdTe stiffens the lattice, increases the resistivity, and increases the bandgap [37], all of which improves the performance of X-ray detectors.

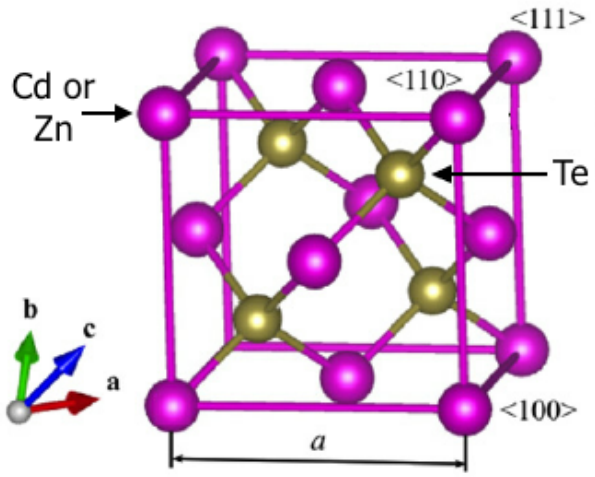


FIGURE 2.7: CDTE DOPED WITH ZN LATTICE [38]

It can be difficult to obtain high quality CdZnTe and CdTe with low defect density. In the CdZnTe material, intrinsic defects and residual impurities are electrically active. Defects present a problem for detectors, since they result in incomplete charging, as a result of trapping of charge carriers [39].

Defects commonly found in CdTe doped with Zn are cadmium vacancies (V_{Cd}), Te vacancies (V_{Te}), and Zn as an interstitial (Zn_i). The two dominate defects are cadmium vacancies (V_{Cd}) and tellurium antisites (Te_{Cd}), with cadmium vacancies being the dominant of the two [30]. A telluride antisite is when a Te atom occupies the space in the lattice where a Cd atom should be. A Cd vacancy defect is a double acceptor, since it leaves the neighboring Te atom with a dangling bond, which needs two electrons for the atom to be neutral. Consequently, a Cd vacancy in CdTe induces a tensile stress field on the nearby Te atoms in the lattice [39]. This type of force pulls the Te atoms closer to each other. This leads to repulsive forces between the Te atoms leading to stress and deformation by nearby atom bonds.

The formation energy of the Cd vacancy decreases as the concentration of Zn increases and the formation energy of Te antisite increases as the concentration of Zn increases as illustrated in Fig. 2.8. This indicates that Cd vacancies are more likely to form after the doping of Zn is 20% or higher, as a result of an even higher reduction in the Cd vacancy formation energy. At the same time, the tellurium antisite formation energy increases, making it more difficult to form.

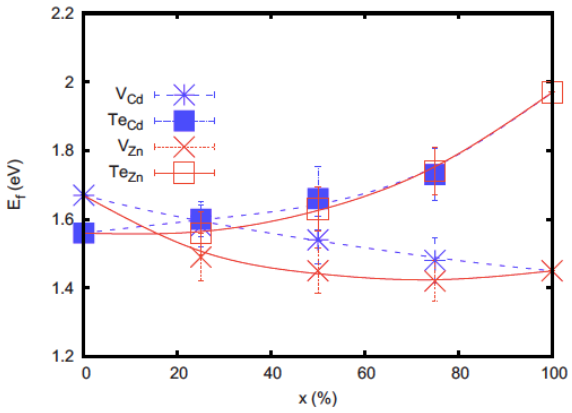


FIGURE 2.8: SIMULATION OF MINIMUM FORMATION ENERGIES OF CATION VACANCY V_X AND TELLURIUM ANTISITE TE_X DEFECTS IN $CD_{1-X}ZN_XTE$, WITH VARYING CONCENTRATION OF ZN [39].

The bond length between Zn and Te is 12% longer in CdZnTe than its ideal, strain free length in ZnTe. Since the Zn atom is smaller than the Cd atom, this causes the Te bonds to stretch toward the Zn atom. This creates a strain field around the substitution of a Zn atom for a Cd atom. This favors the formation of tensile defects, cadmium vacancies, but disfavors the formation of compressive defects such as the tellurium antisite.

The ZnTe bond is less ionic than the CdTe bond and has a higher cohesive energy, since the ZnTe bonds are shorter and stronger than the CdTe bonds [39, 40]. Because of this, the

defects migration path avoids the ZnTe bond. The Cd-Te bonds are longer and require less energy to break. As a result, Zn atoms in CdTe stiffen the lattice and increase the energy needed to displace defects in the material. Both Te_{Cd} and V_{Cd} defects migrate following the Cd rich paths, and both of these types of defects will be less mobile as the concentration of Zn increases. A stronger lattice and fewer tellurium antisites reduces the etch pit density for bulk material [41].

CdTe doped with Zn undergoes several structural changes. XRD analysis shows that the dominant orientation for CdTe doped with a low percentage of Zn is the (220) orientation and as the Zn concentration is increased, the (220) peak shifts from 39.511˚ to 40.962˚ [42]. Twins are the most common defect found in CdTe film growth on Si substrates, with a growth orientation in the (111) direction [43]. Twins are characterized as crystal planes, which are symmetrical, on either side of an interface or grain boundary, but are misorientated at an angle with respect to each other. Twins result during epitaxial growth when an error in the staking of the unit cells of the grown material occur. Lamellar and double positioning twins are two types of twins found in the crystal illustrated in Fig. 2.9. They are referred to as polysynthetic twins, since multiple twins are aligned in parallel. The lamellar twin forms a coherent twin boundary parallel to the (111) plane. The double-positioning twins form an incoherent boundary perpendicular to the (111) plane. Both types of twins have 180˚ rotational symmetry. When CdTe is grown on Si(111), twins occur at a higher density, and propagate further away from the CdTe/Si interface [44]. This is the preferred growth direction for twins and is a way to relieve the stress induced by the lattice mismatch at the interface. Si (211) has been known to reduce the amount of twin formation at the interface.

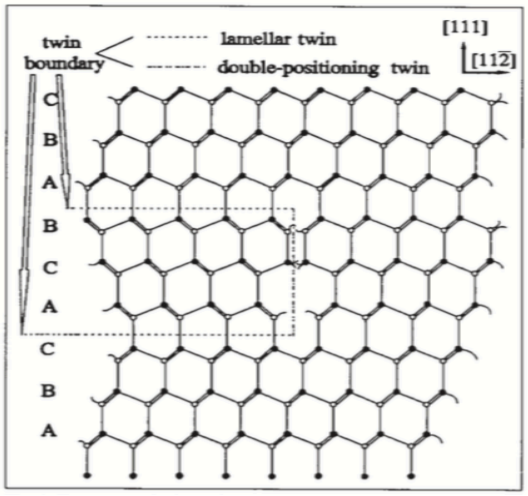


FIGURE 2.9: ILLUSTRATION OF LAMELLAR AND DOUBLE POSITION TWINS IN A CDTE CRYSTAL [45].

The TEM helps to provide information about the types of defects that result from the strain caused by the lattice mismatch of 12% to 19% between CdTe and Si. Depending on the orientation, defects can travel to the surface of the film or only a short distance from the interface [31]. Zhao et. al (2011) reports that stacking faults are the most common defect and also form when CdTe is grown on Si(111) substrates, and are reposted to extend 50 nm from the film interface [31].

2.5.2 GROWTH OF CDTE DOPED WITH ZN

The lattice constant for silicon is 5.43 Å, while the lattice constant for CdTe is 6.482 Å. As mentioned above, the difference in lattice constant, results in a lattice mismatch of 19%. The large lattice mismatch results in defects forming at the interface of the two materials. A ZnTe buffer layer is often used to reduce the defects at the interface, since it has a lattice constant of 6.101 Å, which is closer to that of Si. This results in a lattice mismatch of 12% between ZnTe and Si and a more gradual accommodation of strain between each material. Therefore, doping CdTe with Zn further reduces the lattice mismatch between CdTe and Si. Adding Zn to CdTe

reduces its lattice constant to, 6.463 Å for 5% Zn and 6.444 Å for 10% Zn. This results in a smaller change in the lattice mismatch between the CdTe and Si. Several methods have been used to grow CdTe doped with Zn on different types of substrates. The most common doping concentration of Zn for CdTe in X-ray detector applications used in industry is 10% [10, 46, 47]. The range of Zn doping varies between 10% and 20% [21, 36].

The Electrochemical bath method is used to deposit CdZnTe on SnO_2 with the solution consisting of $CdCl_2$, $ZnCl_2$, and Te [49]. The XRD data shows that the CdZnTe film is polycrystalline with (111) and (200) being the dominant peaks. As the growth potential is increased in the negative direction, there is a decrease in grain size. The grain size ranged from micrometers to nanometers. CdZnTe prefers to grow in the (111) and (200) direction on SnO_2.

The closed space sublimation (CSS) and metalorganic chemical vapor deposition (MOCVD) methods are used to grow CdZnTe on GaAs and GaAs/Si substrates [50, 51]. The CdZnTe source material is in powered form and is doped with 10% Zn. CdZnTe is grown on GaAs (001) substrates using the CSS method. The growth parameters for growing CdZnTe doped with 10% Zn are source temperatures, 788k and 873k, and substrate temperatures are 763K and 848K. The atomic force microscopy (AFM) root mean square roughness is 5nm for a smooth and high quality surface. The XRD data is used to characterize the CdZnTe growth and shows (002) and (004) orientations as the dominant peaks. The (004) orientation has a wide base that is caused by defects in the film, but as the temperature is increased the quality is improved. The full width at half max (FWHM) for the (004) peak is 306 arcsec for a source temperature of 873K. Based on TEM analysis, the CdZnTe film did not show any twins present and the defects are confined near the interface (Fig. 2.10).

The MOCVD method is used to grow CdTe with 4% Zn on GaAs/Si(100) substrates at a temperature range between 390˚C and 450˚C. The XRD shows that the CdZnTe film is misoriented towards the [111] orientation. TEM analysis revels twins present in the CdZnTe growth. The MOCVD method is also used to grow CdZnTe on GaAs/Si(001) substrates. Doping with 4% Zn resulted in a CdZnTe layer grown on GaAs/Si(001) with a FWHM of 83 arcsec. The FWHM of the MOCVD method resulted in an excellent value versus the CSS method.

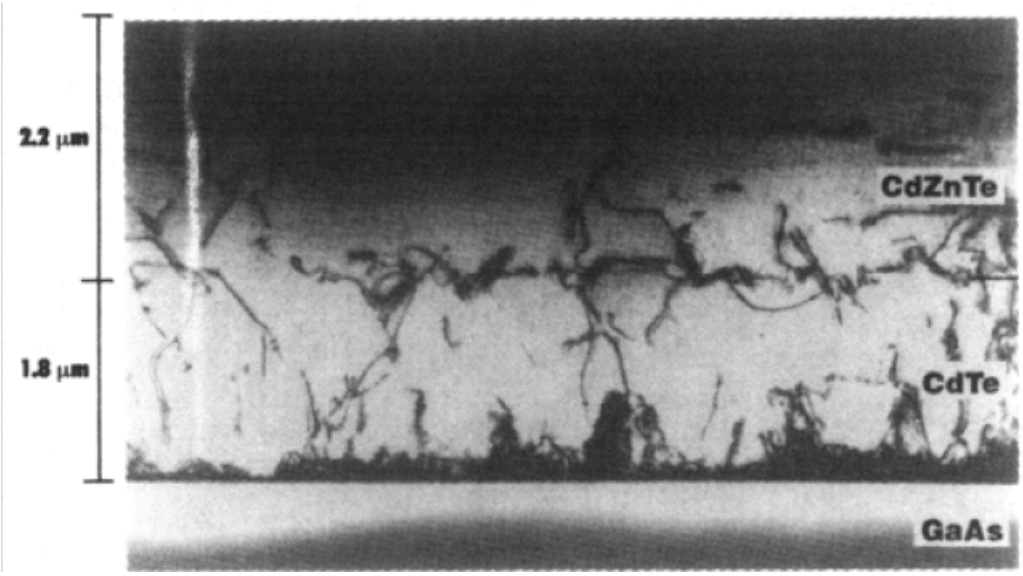


FIGURE 2.10: TEM CROSS-SECTION OF CDZNTE/CDTE/GAAS INTERFACE WITH NO TWINS [51]

The MBE method is used to grow CdZnTe on Si substrates using a ZnTe buffer layer [8, 52, 53, 54, 55]. The first study uses a Si(211) substrate and the ZnTe buffer layer ranges from 15 nm to 25 nm. The Zn doping in CdTe ranges from 2% to 4%, and is controlled by varying the flux of CdTe and ZnTe sources. The FWHM of the CdTe with Zn doping is approximately 150 arcsec [55]. This value is higher than the value reported from a previous study of CdTe without doping of 71, arcsec. CdTe doped with 2% to 6% Zn, with a buffer layer on Si (112) has a high density of twins at the interface, shown by the TEM [8]. For a Si(100) substrate with a 1μm

ZnTe buffer layer, and 4% Zn doping results in a FWHM of 160 to 200 arcsec for the (400) orientation [53]. When CdZnTe is grown on Si (001) with a ZnTe buffer layer, FWHM is 78 arcsec for the (004) orientation as shown in Fig. 2.11 [55]. These studies show that as the ZnTe buffer layer thickness is decreased the FWHM also decreases.

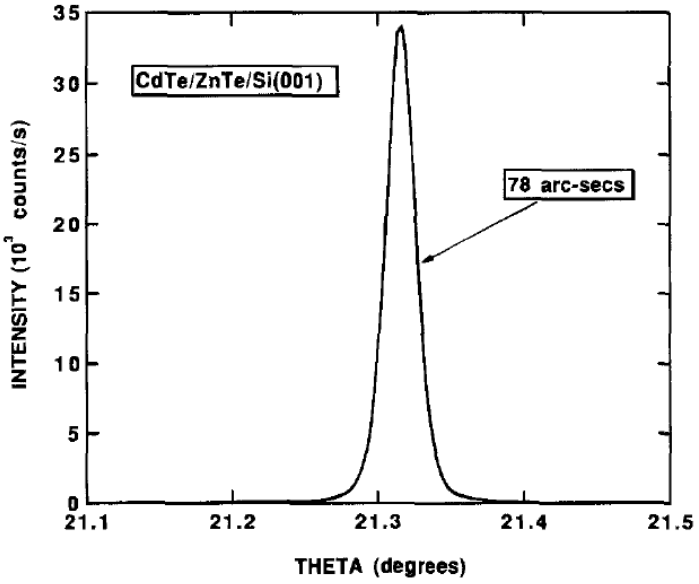


FIGURE 2.11: X-RAY ROCKING CURVE FOR CDTE/ZNTE/SI(001) IN THE (004) ORIENTATION [55]

Thermal vacuum evaporation, hot wall epitaxy (HWE), and low-pressure chemical vapor deposition (LPCVD) is used to grow CdZnTe directly on Si [43, 56, 57, 58]. CdZnTe grown by LPCVD has 20% and 8% Zn doping on Si (111) and Si (100), respectively. The XRD data shows a 2θ peak at 27.8˚, which corresponded to the (111) orientation for CdZnTe (Fig. 2.12). The CdZnTe peak of (111) orientation is present for CdZnTe growth on both Si(111) and Si(100) substrates (Fig. 2.13 (a)). SEM images show that the surface is rough and the XRD data proves the film is epitaxial for Si(111) (Fig. 2.13 (b)).

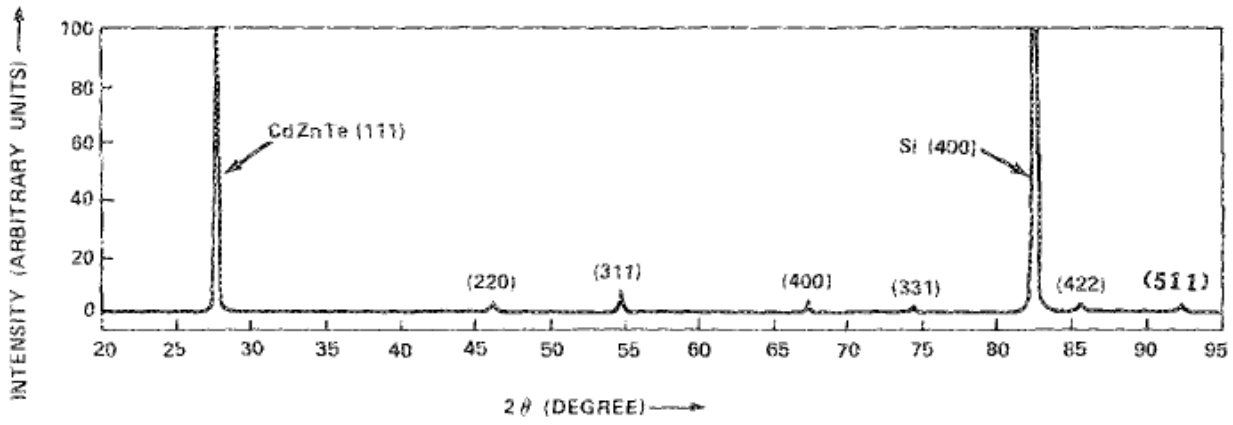


FIGURE 2.12: X-RAY DIFFRACTION OF CDTE WITH 8% ZN GROWN ON SI(100) [56]

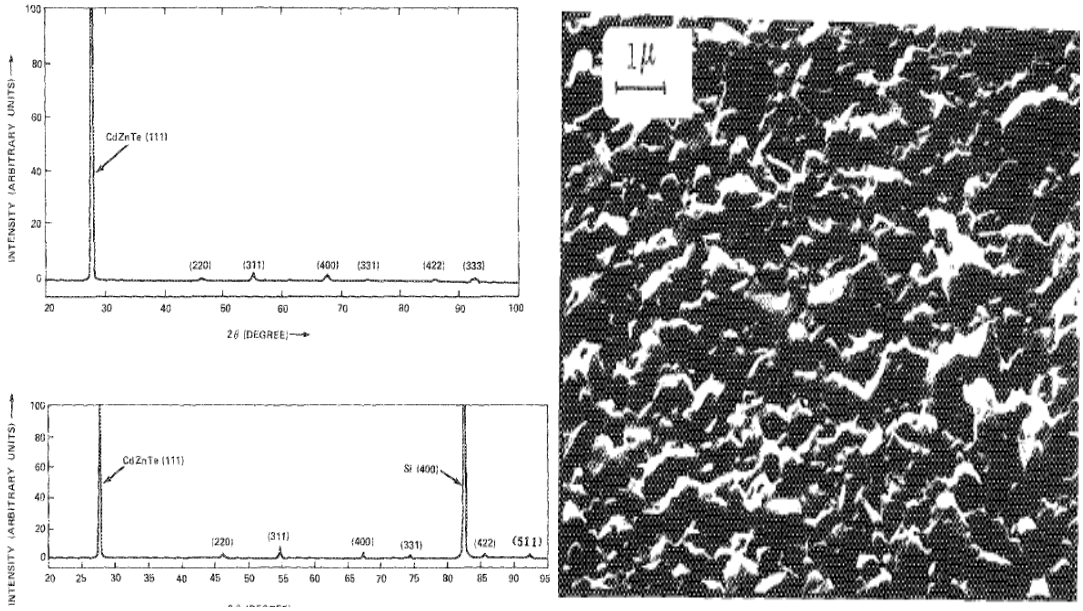


FIGURE 2.13: CDZNTE GROWTH BY LOW-PRESSURE CHEMICAL VAPOR DEPOSITION (A) XRD OF CDZNTE FILM (B) SEM OF CDZNTE FILM [56]

CdZnTe growth by HWE on Si (100) substrates 4% Zn results in a main orientation of (400), with a mirror like film surface [43]. CdZnTe grown by HWE on Si (111) with 4% Zn, and

a substrate temperature of 350˚C results in a FWHM 119 arcsec for (111) orientation, and poor growth quality [43].

The thermal vacuum evaporation method is used to grow CdZnTe with 6% Zn on Si(111) substrates. The TEM analysis shows a 3 nm CdZnTe layer is amorphous and the composition is mainly Te atoms. The CdZnTe deposited layer has an orientation of (111) and has an average grain size of 15 nm (Fig. 2.14) [58]. The XRD data shows that the (111) orientation is dominant with smaller (110) and (331) orientations. These CdZnTe films are grown on Si directly without a ZnTe buffer layer and the FWHM value that is reported is 266 arcsec for the (444) orientation, which is higher than the values with a ZnTe buffer layer 78 arcsec [55, 58]. When CdZnTe is grown on Si without a buffer layer, CdZnTe growth prefers the (111) orientation [34]. Twins are observed at the Si interface, which reduces the quality of the film [58].

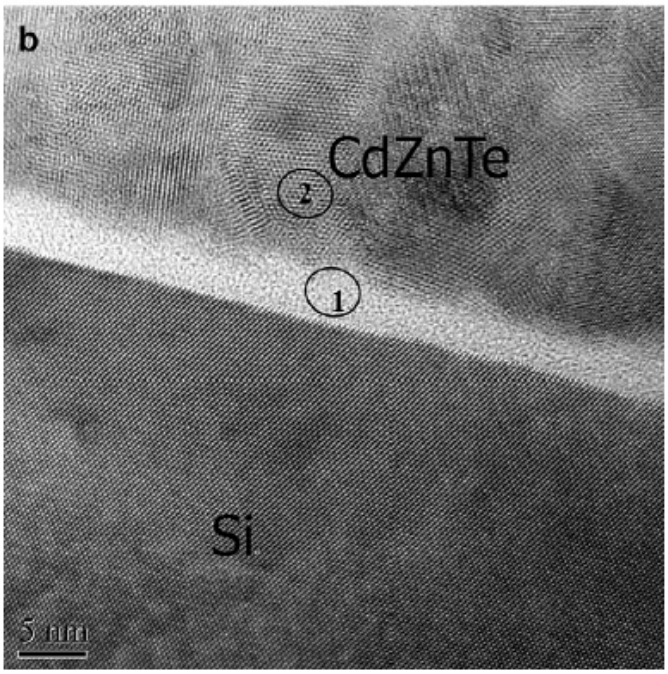
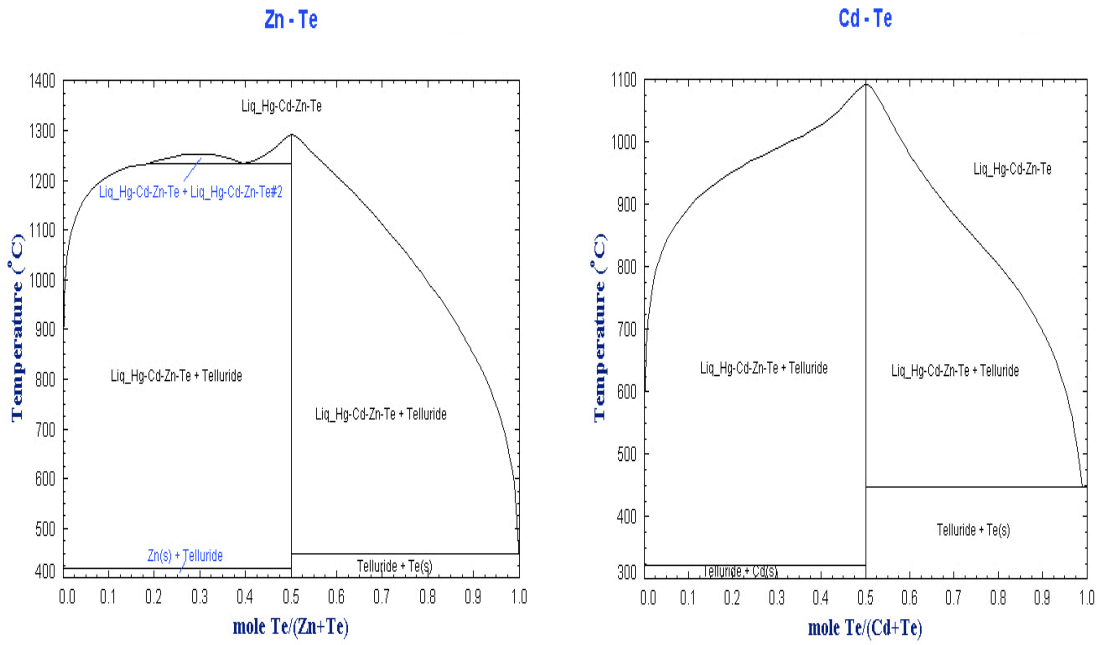


FIGURE 2.14: HRTEM OF CDZNTE/SI INTERFACE [58]

2.6 CdTe Growth with Zn Doping using the CSS Method

Growing CdTe doped with Zn on Si is challenging due to low thermal conductivity for Si, CdTe twin formation, CdTe film stoichiometry control, and Zn segregation. These problems play a role in the quality of growth of CdTe. The most common methods for epitaxial growth for CdTe are Molecular Beam Epitaxy (MBE) and Metalorganic Vapor Phase Epitaxy (MOVPE) [29]. These methods are both costly and have slow growth rates relative to the CSS method. This makes epitaxial growth difficult when thick layers are required, such as those required for X-ray imaging that range from 1 mm to 10 mm or thicker [16]. The use of the close spaced sublimation (CSS) technique has several advantages over MBE and MOVPE. The CSS advantages are easily scaled for industry use. The main draw back for the CSS is the quality of film planar growth. Thee have been many efforts to improve the CdTe growth quality using the CSS technique [28, 29, 61].

The CSS can control the structure properties of the CdTe doped with Zn by varying the following during deposition: (1) source temperature, (2) substrate temperature, (3) distance between source and substrate, (4) pressure, and (5) gas flow rate. Fig. 2.15 shows the phase diagram as a function of Te for ZnTe and CdTe materials. The stoichiometric CdTe, which is 50% Cd and 50% Te, is the most stable phase for CdTe. This stable phase is near 1100˚C. The stoichiometric ZnTe is most stable around 1300˚C. Cd and Te have similar atomic masses which results in stoichiometric growth. But Zn has a smaller mass compared to Te and Cd. Since Zn-Te bond is stronger than the Cd-Te bond, a higher temperature is necessary to break the bond. An even distribution of Zn in CdTe can be obtained at a lower temperature using the CSS method than what is stated in the phase diagram [59].



(a) (b)

FIGURE 2.15: PHASE DIAGRAM OF ZNTE AND CDTE AS A FUNCTION OF TE [60].

The mean free path for Cd, Zn, and Te is calculated using the following equation:

$$\lambda = \frac{RT}{\sqrt{2}\pi d^2 N_a P} \quad (1)$$

Where P is the pressure, T is the temperature, d is the diameter of the molecule, and Na is Avagadro's Number. The mean free path for Cd is 0.7 mm, 1.3 for Te, and 0.98 mm for Zn. Zn is able to sublimate based on the distance used for the spacers.

The source and substrate temperatures can be varied to determine the best quality growth and the condition for selectivity. The distance between the source and substrate will be at approximately 1 mm, which is the optimal distance for selective growth [28, 29, 61]. Single crystal growth has been observed between 0.25 Torr and 2 Torr [61].

The gas flow rate is measured as standard liters per minute (SLPM). Hydrogen (H_2) is similar to Helium (He) in its physical properties, except that it is reactive. It has been shown that H_2 is a good carrier for many materials, but it is not a good carrier for CdTe depositions [62]. He results in a higher growth rate and a good transport for CdTe growth. He also helps to promote selective growth [28, 29, 61].

Tokuda et al. (2004) uses the CSS method to grow 200 μm of CdZnTe on glass and alumina (Al_2O_3) at a source temperature of 600˚C [63]. The substrate is 100 mm x 70 mm for both glass and alumina. Alumina is selected to reduce of micro-cracks at the interface, caused by the thermal expansion coefficient of 24 10^{-6} C. A sinter mix of CdTe and ZnTe is used as the source material to deposit a CdZnTe layer on the alumina substrate at 600˚C. XRD analysis of the CdZnTe film and results in a (111) orientation at 24.20˚. A 9" x 9" film is grown in this study and the zinc concentration is about 4 mol%. An SEM analysis shows that the CdZnTe film is made of 100 μm grains. This study demonstrates that a temperature of 600˚C is required to grow CdZnTe on alumina using the CSS method. The high growth temperatures result in large CdTe grains.

Dzhafarov et al. 2005 examined the use of the CSS method to grow CdTe doped with Zn by diffusing Zn into the CdTe grown layer [64]. The deposition of CdTe on CdTe, using the CSS method produces a 1-5μm thick layer. A 40 nm – 100 nm thick layer of Zn is deposited on the CdTe surface by using electron beam evaporation. The sample is annealed at 500˚C and 1.3 Pa for 10 minutes to diffuse Zn into the CdTe layer. After annealing, the remaining Zn is removed using HCl. XRD analysis of the sample resulted in a single (111) peak at $2\theta = 24.22°$. This indicates a lattice parameter of $d_0 = 0.6360$ nm, and a Zn concentration of 21%. CdTe without Zn results in a smaller diffraction angle of $2\theta = 24.02°$ and a lattice constant of a = 0.6412 nm. This shows one possible way to grow CdTe doped with Zn.

Gao et al. (2012) examined the use of the CSS method for the growth of CdZnTe on GaAs (001) substrates, using $Cd_{0.9}Zn_{0.1}Te$ powder as a source material, a source temperature of 788K to 873K, substrates temperature of 763K to 848K, for 10 minutes and 120 minutes [65].

A 9.8 μm thick CdZnTe film is deposited by CSS on the (001) GaAs substrate. A 7 nm amorphous layer is observed at the interface of GaAs and CdZnTe. When the deposition time is increased by 20 minutes, the amorphous layer disappears. It is noted that Te atoms are less volatile than Cd and Zn atoms. This results in higher dissociation energy of Te–Te bonds. The best deposition resulted in a FWHM of 306 arcsec. The growth resulted in a (400) orientation being the dominant peak with a small second peak at (200) orientation. TEM analysis shows that the growth is epitaxial and there are defects at the interface that travel 570 nm away from the interface. This show that epitaxial growth can be obtain form the CSS method and the defects are localized to the interface.

Huang et al. 2012 examined the use of CSS method to grow $Cd_{0.9}Zn_{0.1}Te$ with source temperatures between 570˚C and 650˚C a fluorine doped tin oxide (FTO) glass substrate [66]. A source to substrate distance of 3 mm and 5 mm is used. As the substrate temperature is increased above 450˚C, a drop in the growth rate is observed. This can be explained by increased re-evaporation of CZT from the substrate, along with the atoms being more mobile on the substrate surface. There is a single peak in the XRD at the (111) orientation which indicates single crystal.

Tobenas et al. (2001) examined the use of isothermal close space sublimation (ICSS) method to grow CdZnTe on GaAs substrates [67]. Zinc, cadmium and tellurium are evaporation in individual source compartments. The deposited films have mirror-like surfaces, and XRD showed that a (200) plane diffraction peak and for CdZnTe. It is noted that the Zn–Te bond is more

stable than the Cd–Te bond. This can produce a higher concentration of Zn in the sample. Cd atoms from the inner deposited layers can diffuse to the surface and be substituted by Zn atoms.

Tokuda et al. (2002) examined the use of CSS method to grow CdZnTe on glass and alumina (Al_2O_3) substrates [68]. The resulting film surface is rough with large grains with an average 100 μm in size. Polycrystalline grains are observed in the sample and the orientation could not be determined. The concentration of the Zn in the sample is from 3.6% to 4.6% molar mass.

2.7 CdTe Growth Models

Modeling of CdTe growth is accomplished using molecular dynamics, Molte Carlo, and atomistic simulations. These methods help to better understand the quality and growth of CdTe. Molecular dynamics and Molte Carlo have been used to simulate both molecular beam epitaxy (MBE) and close spaced sublimation CdTe growth.

Oh et al. (1998) uses a combination of molecular dynamics and Molte Carlo methods to simulate the growth of CdTe(111) on Si(001) [69]. These two methods are used to examine the effect of temperature on growth quality and to find a model for dynamical growth. The results of the simulation of CdTe(111) on Si(001) indicates a similar growth of CdTe epilayer observed in experiments previously preformed.
produce the highest-quality epilayers.

Zang et al. (2011) uses molecular dynamics to simulate the growth of CdTe/ZnTe on Si (211) substrates [70]. Atomic interactions are simulated using the Stillinger–Weber potentials and focuses on the growth of the ZnTe buffer layer. The simulation shows that the best quality growth for ZnTe occurs at 300˚C and 350˚C, and the surface roughness of the CdTe layer is smoother when the there is less Te atoms in the flux.

Ward et al. (2012) simulates vapor deposition of CdZnTe on CdTe using molecular dynamics with bond-order potential [71]. During the simulations zero pressure is assumed for the growth of $Cd_{0.5}Zn_{0.5}Te$ on CdTe, with Cd atoms terminating on the surface. A substrate temperature of 1000 K, a deposition rate of 2.6 nm/ns, and a vapor flux ratio of Cd:Zn:Te= 1:1:2 is applied. The method is apple to correctly predict defects in CdZnTe, such as cadmium vacancies and tellurium antsites.

Simulation of CdTe growth has been shown by Cruz-Camp et. al 2009 using the CSS method [72], by focusing on the source and substrate temperature, pressure, distance between the source and substrate, and interaction of gas molecules with the CdTe atoms. The model shows that CSS can be modeled accurately by either the diffusion limited or sublimation limited models. This can help to better find the optimal parameters for growth.

Based on the diffusion limited model the CdTe growth is controlled by the pressure, the distance between the source and substrate, and the ΔT of the source temperature and substrate temperature. The diffusion, in this case He, is controlled by the source temperature, substrate temperature, and the flow rate of the gas. The deposition rate is given by the following relationship:

$$Depostion\ rate\ \left(\frac{m}{s}\right) = \frac{P_{sou}^{i}(T)N_a}{\sqrt{\pi m_i RT}}\left(\frac{m_i}{\rho_i}\right) \quad (2)$$

Where P_{sou}^{i} is vapor pressure is in for the substance i to be evaporated at the source (Pa), m_i is the molar mass of the source material in (kg/mol), R is the universal gas constant in (J/(mol K)), T is the temperature of the source in (K), N_A is Avogadro's number, and ρ_i density of the substance evaporated in (kg/m^3). If the pressure is higher than 1 Torr and the distance between source and substrate is greater than the mean free path, then the growth is said to be diffusion-limited [72].

In the sublimation limited model, there is no collision between the source atoms as they move towards the substrate. This model is based on a study done by Hertz et al (2001) and where the sublimation rate is controlled by the temperature [72]. The growth rate is given by the following relationship:

$$GR\ \left(\frac{m}{s}\right) = \frac{\alpha\beta\left[p^i_{sou}T_{sou} - p^i_{sub}T_{sub}\right]N_A}{\sqrt{\pi m_i R T_{av}}}\left(\frac{m_i}{\rho_i}\right) \qquad (3)$$

Where α and β are coefficients with values between 0 and 1, $p^i_{sou}$and p^i_{sub} are the vapor pressure of the materials evaporated for the source and substrate (Pa), m_i is the molar mass of the source material in (kg/mol), R is the universal gas constant in (J/(mol K)), T_{sou} and T_{sub} are the source and substrate temperatures in (K), T_{av} is the average temperature of the system, N_A is Avogadro's number, and ρ_i is the density of the substance evaporated in (kg/m^3) [72]. This model only applies to temperatures between 400˚C and 600˚C, pressures between 10^{-2} and 760 Torr, and a distance between the source and substrate between 0.8 mm and 1 mm.

Molecular dynamics growth simulations for CdZnTe growth on CdS study the dislocations at the interface that resulted from the lattice mismatch [48]. As the percent Zn is increased from 0% to 20%, the dislocation density and dislocation length decreases, with 20% Zn having the fewest and the shortest dislocation lengths (Fig. 2.16). As the percent Zn is increased beyond 20%, the dislocation density and dislocation length begin to increase [48].

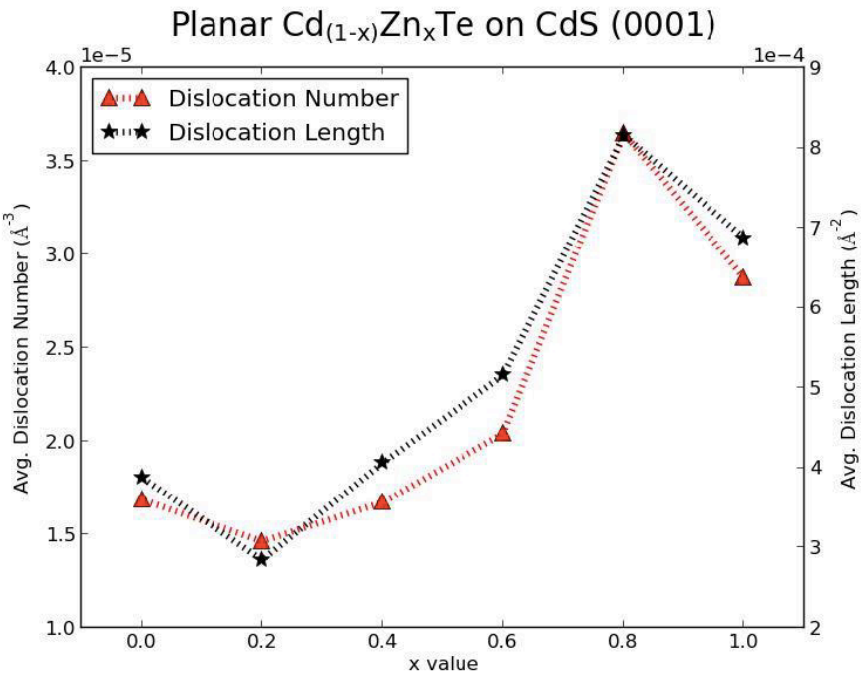


FIGURE 2.16: DISLOCATION NUMBER VS PERCENT OF ZN IN $CD_{(1-X)}ZN_XTE$ GROWTH ON CDS [48]

2.8 Role of Nanoheteroepitaxy

2.8.1 EFFECT ON INTERFACIAL STRAIN

CdTe doped with Zn has a large lattice mismatch with Si. The mismatch can range from 12% to 19%, with x=0 and x=1 respectively for $Cd_{x-1}Zn_xTe$ [8]. The large lattice mismatch results in an increase in energy at the interface, which leads to an increase in defects such as twins forming at the interface between the two materials and propagate through the CdZnTe thin film.

The use of heteroepitaxy method has been commonly applied on to Si to the growth of germanium (Ge). This material system has a lattice mismatch of 4%. This method incorporates the use of islands or pillar pattern to help relieve the strain at the interface. Heteroepitaxy results in a for three-dimensional stress relief on the deposited material resulting in less defects to form

at the interface [73]. Zubia et al. (2000) suggests that if the lattice mismatch is greater than 8% a diameter of the pillars needs to be less than 10 nm-100 nm.

The Heteroepitaxy method often incorporates a mask such as SiO_2 to promote the selective growth of the deposited material. The deposition of the material on the top of the pillars allows the defects that form at the interface to propagate a short distance. In planer growth, the defects propagate through the thin film to the surface.

Crystal growth is limited in the lateral direction by a mechanism results in strain relief at the edge of the nanoheteroepitaxy pattern from the free surfaces at the edges [74]. Hersee observed the growth of GaN on Si (111) using TEM, where stacking defects are observed at the basal [75]. Although there is a high dislocation density at the interface, but they did not propagate through the epilayer. The dislocations associated with the mismatch between the two materials decay exponentially away from the interface (Fig. 2.17).

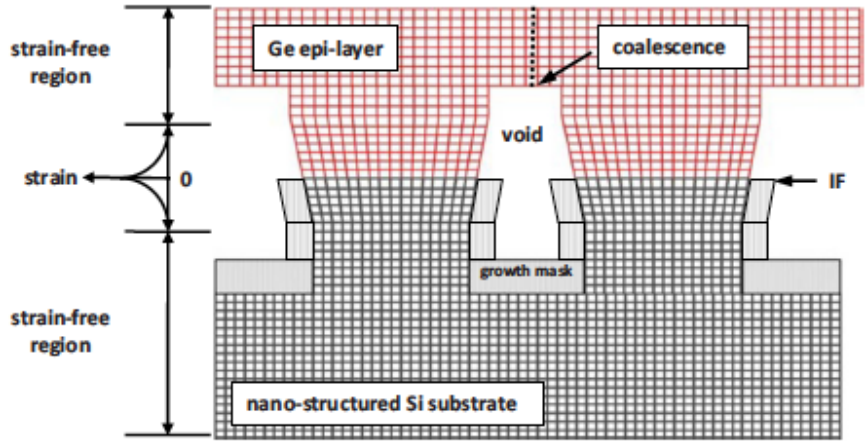


FIGURE 2.17: MODEL OF NANOHETEROEPITAXY PROPOSED BY [73]

The nanoheteroepitaxy method has an advantage compared to planar growth (Fig. 2.18). With planar growth, the growth of the material can only deform vertically in order to relieve the stress caused by the lattice mismatch. With nanoheteroepitaxy the deformation occurs vertically and laterally, to reduce the strain in three dimensions (Fig. 2.18) [75, 76]. With planer growth, the strain energy increases linearly with increasing growth of the epilayer. This results in an increase in defects in the deposited material, and at the interface [73]. This in not the case with nanoheteroepitaxy where the epilayer can deform vertically and laterally to reduce the generation of dislocations. The stain that is present at the interface decreases exponentially with distance from the interface. This results in higher quality growth of with increase thickness.

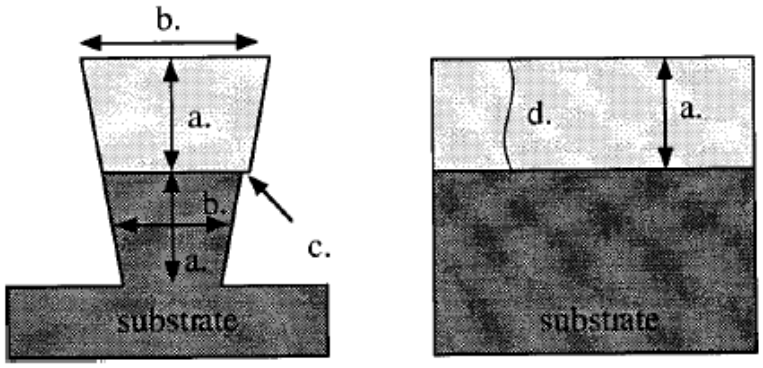


FIGURE 2.18: MODEL OF NANOHETEROEPITAXY PROPOSED BY [77]

2.8.2 FACTORS AFFECTING SELECTIVE GROWTH

Selective epitaxial growth is the high nucleation of material on the exposed substrate material with low nucleation on the mask material [78, 79, 75]. Selective growth can be improved by changing the growth temperatures, reactor pressure, and pattern parameters on the substrate surface. The pattern parameters that are known to affect selective growth are the pillar diameter, the pitch, and the height of the pillars. The pitch has more of an impact on the growth rate; as the pitch gets smaller the growth rate of the deposited material increases [80, 73]. Higher substrate temperatures, lower pressures, selection of mask material, and substrate orientation improve the selective growth process [78, 79].

Nucleation of the deposited material happens instantly over the exposed surface of the substrate. Ideally, more time is required for the deposited material to nucleate on the surface of the mask material, than that of the substrate [81]. Selective growth of CdTe has been shown using MOVPE and MBE on Si and GaAs substrates [81]. The growth of single crystalline and selective growth depends on the flux value of CdTe and the growth temperature. When in a hydrogen atmosphere, the hydrogen seems to have an effect on the selective growth process [78]. For instance, for the selective growth of SiGe on Si, the selective growth is enhanced in the presence of GeH_4.

Several types of materials have been used as masks for selective growth. A mask is used to prevent a specific material from growing on a specified area. A mask is used to prevent a material from growing on the sides of the pillars or areas where growth is not desired. The mask materials that have a low nucleation rate compared to Si for CdTe, InP, GaAs, GaN, and SiGe on Si substrates include SiO_2, Si_3N_4, and CaF_2 [75, 78, 81, 82].

CaF_2 and Si_3N_4 and material has been used as a mask to grow CdTe on a Si and GaAs substrate [44, 81]. Si_3N_4 is used to grow CdTe at 320˚C for the substrate temperature. It is theorized that if the temperature is higher than 350˚C for the substrate, the growth would not be single-crystalline for molecular beam epitaxy (MBE) method [44].

SiO_2 is the most common material used for selective growth on Si substrates. SiO_2 is used to passivate the sides of the pillars. This results in Te atoms having a higher bond energy with silicon, then that of SiO_2 and allows the Te atoms on SiO_2 to desorb during the deposition [84] SiO_2 has been used as a mask to prevent the depositing material from growing on the sides of the pillars. The growth rate is greater when the pitch of the nanopillars is smaller [80].

In Fig. 2.19, SiO_2 is grown on the sidewalls and the bottom of the nanopillars and only the top surface of the pillar is exposed for Ge grown [83]. The selective growth is a result of the Te atoms having higher bond energy with silicon, then with SiO_2. The Te atoms on SiO_2 to desorb during the deposition [84].

Kozlowski et al. (2011) uses SiO_2 as a mask, with a thickness of 15 nm to 25 nm, to grow Ge on Si(001) substrates [85]. Reduced pressure chemical vapor deposition (RP-CVD) is used to selectively grow Ge on Si substrates. It is observed that the strain energy decreased at the interface with a thinner oxide layer. The strain energy in the Ge film, reduces away from the interface. Misfit dislocations result from the energy strain and has a spacing of approximately 10.6 nm at the interface.

Sporken et al. (2000) uses the MBE method and SiO_2 mask to selectively grow CdTe on Si(111) [86]. Strips with a pitch of 10 μm and 50μm are created. Selectivity of CdTe is achieved at 300˚C.

Diaz et al. (2013) uses the CSS method to selectively grow CdTe on Si pillars without the incorporation of a mask [29]. The best growth is found at a source temperature of 550˚C and a substrate temperature of 450˚C. Defects such as facets and stacking faults are reported at the CdTe/Si(211) interface (Fig. 2.4).

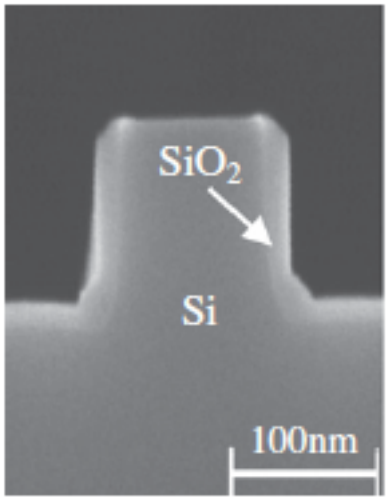


FIGURE 2.19: SILICON PILLAR HAS A SiO_2 MASK NO THE SIDES TO PROMOTE SELECTIVE GROWTH [86].

CdTe is selectively gown on Si with Si_3N_4 and SiO_2 as masks to create the windows for selective growth [44, 84]. Selective growth is achieved for both masks. Fahey et al. (2012) uses MBE to deposit CdTe on CdTe windows 250 nm wide and separated by 250 nm [84]. XRD is used to analyze the resulting CdTe growth and FWHM of 84 arcsec in the (422) orientation.

Metalorganic vapor phase epitaxy (MOVPE) is used to selectively grow several materials. CdTe is selectively gown on Si and GaAs substrates with Si_3N_4, SiO_2, and CaF_2 as a mask to create the windows on CdTe [79, 81]. Bhat el al. (2006) reports a (FWHM) of approximately 1,195 arcsec for CdTe using the XRD. Zhang et al. 2009 reports that the surface

of CdTe contains many defects. For the SiO_2 mask, CdTe grew selectively when temperatures are higher than 450˚C and pressures is lower than 50 Torr. For Si_3N_4 mask shows perfect selective growth on GaAs at temperatures higher than 525˚C.The comparison of SiO_2 and Si_3N_4 showed that Si_3N_4 is a better mask for selective growth on Si substrates. Si_3N_4 has also been used as a mask for the growth of GaN on Si(111) substrates [87]. One study showed the use of MOVPE method to grow GaN on Si without a mask and selective growth is achieved [73].

Table 2.2 summarizes the pervious studies used to selectively grow CdTe and Ge on Si using several different mask materials and patterns.

TABLE 2.2: SUMMARY OF METHODS AND MATERIALS.

Reference	Deposition material/Substrate	Deposition Method	Mask	Pattern
44	CdTe/Si CdTe/ZnTe/Si	MBE	Si_3N_4	Islands
29	CdTe/Si	CSS	None	Pillars
84	CdTe/Si	MBE	SiO_2	Pillars
81	CdTe/Si	MOVPE	Si_3N_4, SiO_2, and CaF_2	Strips and Squares
70	CdTe/Si	MOVPE	Si_3N_4 and SiO_2	Strips
85	Ge/Si	(RP-CVD)	SiO_2	Strips
86	CdTe/Si	MBE	SiO_2	Strips

The CVD method is used to selectively grow Ge on Si nanopillars [83, 88]. Pillar pattern has a diameter of 100nm, with corresponding pitch spacing of 360nm is used and results in a diameter/pitch ratio of 0.277. In one study a transmission electron microscopy (TEM) image is taken of the Si nanopillar and the Ge growth (Fig. 2.20) [83]. The TEM image shows Ge has grown on the top of the pillar. The TEM image shows the presence of misfit dislocations at the Ge/Si interface. No threading dislocations are observed as a result of the small lateral dimensions of the Ge/Si interface. The presence of threading dislocations is known to reduce the device performance [84]. A low amount of misfit dislocations at the Ge/Si interface is observed in [110] and [-110] direction (Fig. 2.21) [88]. Microtwins and a small amount defects in the structure are found throughout the sample in Ge film. It is suggested that further reduction of the pillar parameters would result in reduced defects at the interface.

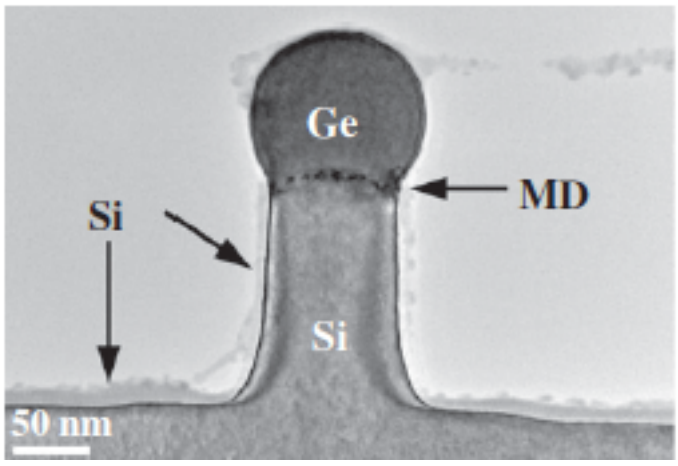


FIGURE 2.20: TEM ANALYSIS OF GE/SI INTERFACE [83]

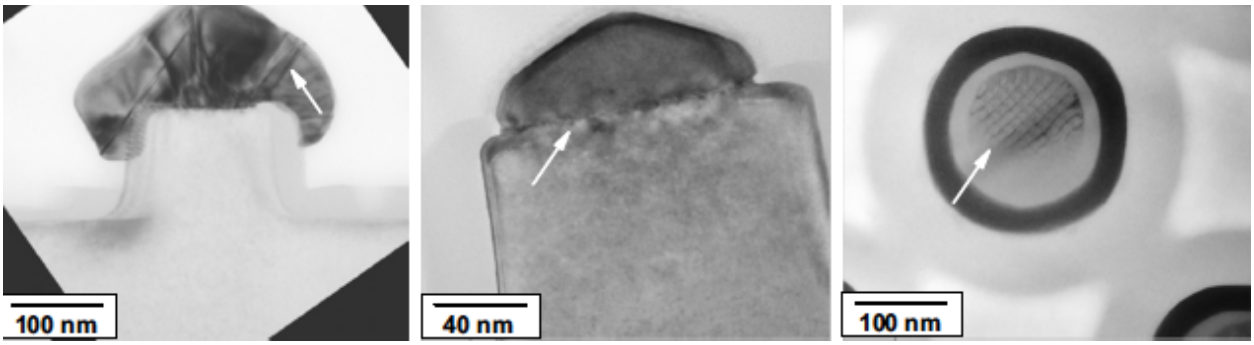


FIGURE 2.21: TEM ANALYSIS OF GE/SI INTERFACE WITH THREADING DISLOCATIONS [88].

Table 2.3 shows a summary of pillar diameter, pillar pitch, height, and the diameter/pitch ratio. These studies helped to determine the best pillar and pitch to use for this study.

TABLE 2.3: THE PITCH, HEIGHT, AND THE RATIO OF THE TWO

Diameter	Pitch	Height	Ratio (diameter/pitch)	Author
100nm	360nm	130nm	0.277	83
150nm	360nm		0.417	84
200nm	500nm		0.4	84
250nm	1000nm		0.25	84
40nm-120nm		120nm		87
	430nm -704nm		0.3	80
100nm		100nm		88
80 nm – 280 nm	360 nm	0.22-0.77	80 nm – 280 nm	73

Chapter 3: Experimental Procedures

This chapter will describe the experimental processes for the selective growth of CdTe on nanopatterned Si(211) and Si(111) substrates along with the material characterization of the interface and CdTe film quality. The aim of this study is to reduce the misorientation and the number of defects at the CdTe/Si interface by (1) using the nanoheteroepitaxial selective growth process and (2) doping CdTe with zinc (Zn) [73, 84].

The main factors influencing the quality of the CdTe growth in this study are summarized below.

- Si wafer orientation – CdTe growth on Si wafers with (211) surface orientation will be analyzed, since low etch pit density and high device performance have been reported for CdTe on the (211) surface [32, 34]. CdTe growth on the Si(111) orientation will also be examined, since it is the preferred orientation for CdTe polycrystalline growth using the CSS method [89].
- Substrate pattern – Several nanoscale pillar patterns created by the electron beam (E-beam) lithography method will be examined in order to determine the optimum pillar size, and pitch to diameter ratio.
- Growth technique – The closed space sublimation (CSS) technique will be used for the selective CdTe growth. The use of the CSS for planar growth results in an increase in defects at the interface. [63, 65, 66]. The use of the CSS method allows for lower cost of operations and higher deposition rates compared to other methods. The CSS can be easily implemented into industrial applications.
- Zn doping – Doping CdTe with Zn results in a stronger lattice, since the ZnTe bonds are stronger and results in a reduction in the defect density for Zn 5% [35, 39, 40, 41].

It is hypothesized that the pattern (pitch/diameter ratio), pattern size, substrate orientation, and the amount of Zn doping will have an effect on the CdTe structure and each will be examined in a systematic manner.

The critical steps used to grow CdTe on nano-patterned Si substrates include the following:

- Substrate Selection and Acquisition
- Substrate Pattern Processes
    - Surface Preparation
    - Photoresist Application
    - Electron Beam Lithography (E-Beam) and Development
    - Dry Etching Process
    - Photoresist Removal Process
    - Summary of Substrate Pattern Methology
    - Pattern Characterization
- CdTe growth on patterned Si(211) and Si(111) substrates using the CSS method
    - Surface Preparation
    - Annealing of CdTe source doped with Zn
    - Close Spaced Sublimation (CSS)
    - CdTe Growth Process
- Materials characterization
    - Scanning Electron Microscopy (SEM)
    - Energy Dispersive X-ray spectroscopy (EDX)
    - X-Ray Diffraction (XRD).

- Focused Ion Beam Process (FIB) TEM Sample Preparation
- Transmission Electron Microscopy (TEM)

3.1 Order of Experiments

A summary of the experiments preformed in this study (Set I - Set V) is shown in Table 3.1. Set I experiments establish the optimum growth temperatures for CdTe doped with 5% Zn growth on Si(211) patterned with 200 nm pillars and a 600 nm pitch. Set I will focus on varying the source temperature from 550˚C to 585˚C and varying the substrate temperature from 450˚C to 505˚C to identify the highest quality growth for this type of substrate.

Set II experiments repeat the best growth parameters of CdTe growth on Si(211) that resulted from Set I. The source temperature of 575˚C and substrate temperature 485˚C is used for all of Set II experiments. The pattern is changed in Set II to 200 nm diameter pillars with a 400 nm pitch. The pitch to diameter ratio is changed from 3 to 2 for Set II, and the time of deposition is varied from 3 minutes to 5 minutes.

Set III examines the effect of decreasing the pitch and the pillar diameter while keeping the same pitch/diameter ratio (p/d=2) from Set II. CdTe is grown on a 200 nm x 100 nm Si(211) patterned substrate using a CdTe source doped with 5% and 10% Zn. Since a change in the pattern surface area for Set III, the source temperature is varied from 565˚C to 600˚C and the substrate temperature is varied from 445˚C to 495˚C.

Set IV experiments involve a further decrease in the pitch to 100 nm and the pillar diameter to 50 nm, while keeping the same p/d ratio from Set II and Set III. The source temperature is varied from 580˚C to 565˚C and the substrate temperature is varied from 455˚C to 485˚C, as a result of the reduction in pattern size. CdTe growth is doped with 5% and 10% Zn.

Set V includes CdTe growth on Si(111) substrates for CdTe doping of 5% and 10% Zn. The pattern dimensions are the same as Set IV, with a pillar diameter of 100 nm and a pitch of 50 nm.

TABLE 3.1: GROWTH PARAMETERS FOR SETS I – V.

Study	Source	Substrate	Pattern (PxD) (nm)	(p/d) ratio	Zn Doping %
Set I	CdTe (111) with twins	Si(211)	600x200	3	5
Set II	CdTe (111) with twins	Si(211)	400x200	2	5
Set III	CdTe (111) with twins	Si(211)	200x100	2	5 10
Set IV	CdTe (111) with twins	Si(211)	100x50	2	5 10
Set V	CdTe (111) with twins	Si(111)	100x50	2	5 10

3.1.1 SET I

The selective growth of CdTe doped with 5% Zn on nanopatterned Si(211) substrate is examined in Set I. The goal for Set I is to identify the optimum source (T_{sor}) and substrate (T_{sub})

temperatures required for high quality selective growth when a CdTe source doped with 5% Zn is used. The source used for Set I is a single crystal CdTe(111) wafer with twins and doped with 5% Zn. The Si(211) substrates for Set I consist of 200 nm pillars, a pitch of 600 nm, and a p/d ratio of 3.

Selective growth of CdTe on Si by the CSS method has been reported by Escobedo, Hoong, Najera, and others [28, 29, 61, 63, 65, 66]. Deposition temperatures for CdTe doped with Zn have been reported around 600˚C [63, 65, 66, 67]. The pressure and the time of deposition are based on previous studies at UTEP [28, 29, 61]. The pattern dimensions are selected based on the average value of p/d ratio found in the literature [73, 80, 83, 84, 87, 88]. The most common concentration of Zn used for X-ray imaging detectors is 10% [1, 10, 20, 21]. As the Zn concentration increases past 20%, the dislocation density increases in the CdTe film [48]. As a result of these studies, the doping concentration selected for Set I is 5% Zn. The growth parameters for Set I are also based on these studies, and are summarized in Table 3.2. Fig. 3.1 summarizes the source and substrate temperatures tested. A decision to increase the source temperature for the rest of the experiments in Set I, is based on the observations of the film for sample S1_1. As noted here, three source temperatures are examined (550 ˚C, 575 ˚C, and 585˚C) and the substrate temperatures is varied between 450 ˚C and 505 ˚C.

TABLE 3.2: SET I-GROWTH OF CDTE WITH 5% ZN ON SI (211) 200 NM PILLARS WITH A 600 NM PITCH.

Fabrication Parameters	Sample name	Tsor (˚C)	Tsub (˚C)	Reactor Pressure (Torr)	Substrate	Pitch/Diameter (nm)	Zinc Doping (%)	Deposition time (min)
Optimization of Deposition Temperatures	S1_1	550	450	1.5	Si (211)	600/200	5	5
	S1_2	575	460	1.5	Si (211)	600/200	5	5
	S1_3	575	475	1.5	Si (211)	600/200	5	3
	S1_4	575	465	1.5	Si (211)	600/200	5	3
	S1_5	575	455	1.5	Si (211)	600/200	5	3
	S1_6	575	485	1.5	Si (211)	600/200	5	3
	S1_7	585	505	1.5	Si (211)	600/200	5	3
	S1_8	585	485	1.5	Si (211)	600/200	5	3
	S1_9	585	495	1.5	Si (211)	600/200	5	3
	S1_10	575	485	1.5	Si (211)	600/200	5	3

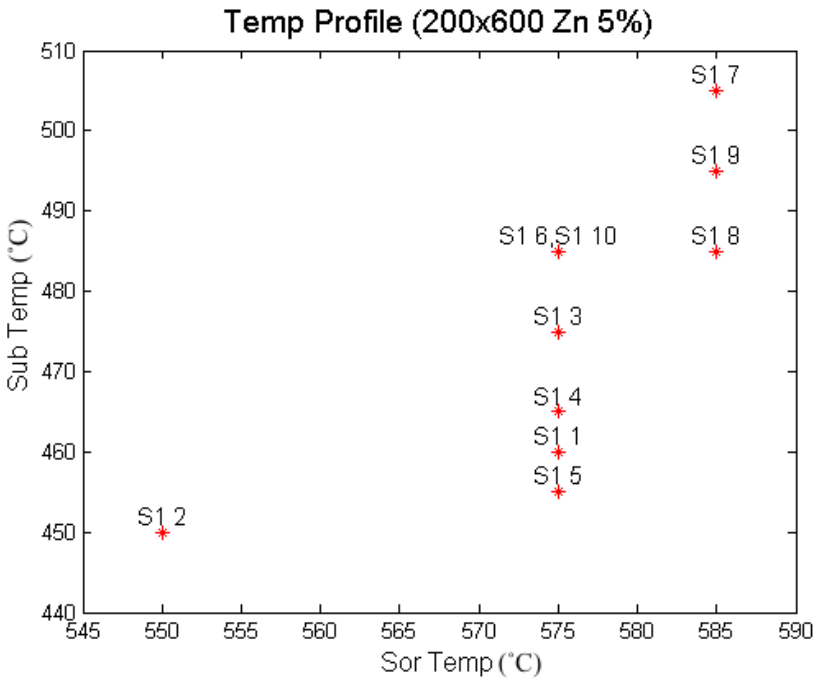


FIGURE 3.1: SOURCE AND SUBSTRATE TEMPERATURE PROFILES FOR SET I

3.1.2 SET II

A pillar diameter of 200 nm is maintained, and the pitch is decreased from 600 nm to 400 nm for the growth of CdTe with 5% Zn on Si(211) substrates for Set II. This results in a p/d ratio of 2. The goal for Set II is to identify the optimum p/d ratio by comparing the p/d of Set II (p/d=2) to that of Set I (p/d=3).

The p/d ratio of 2 is based on research conducted by Bommena et al. (2006) and Bhat et al. (2008) and is the smallest value used in the literature [81, 84]. Bhat and Bommena report selective growth of CdTe on GaAs and Si substrates, with Bhat reporting better growth quality on the smaller pattern of 200 nm to 300 nm pillars, with less than $1x10^5$ cm^{-2} defects at the interface. Table 3.3 includes the growth parameters for Set II. A substrate temperature of 485˚C

and a substrate temperature of 575˚C are used for Set II and are based on the results from Set I. Fig. 3.2 summarizes the source and the substrate temperatures examined for Set I and Set II.

TABLE 3.3: SET II-GROWTH OF CDTE WITH 5% ON SI(211) 200 NM PILLARS WITH A 600 NM PITCH

Fabrication Parameters	Sample name	Tsor (˚C)	Tsub (˚C)	Reactor Pressure (Torr)	Substrate	Pitch/Diameter (nm)	Zinc Doping (%)	Deposition time (min)
Testing of Diameter and Pitch Ratio	S2_1	575	485	1.5	Si (211)	400/200	5	3
	S2_2	575	485	1.5	Si (211)	400/200	5	3
	S2_3	575	485	1.5	Si (211)	400/200	5	5

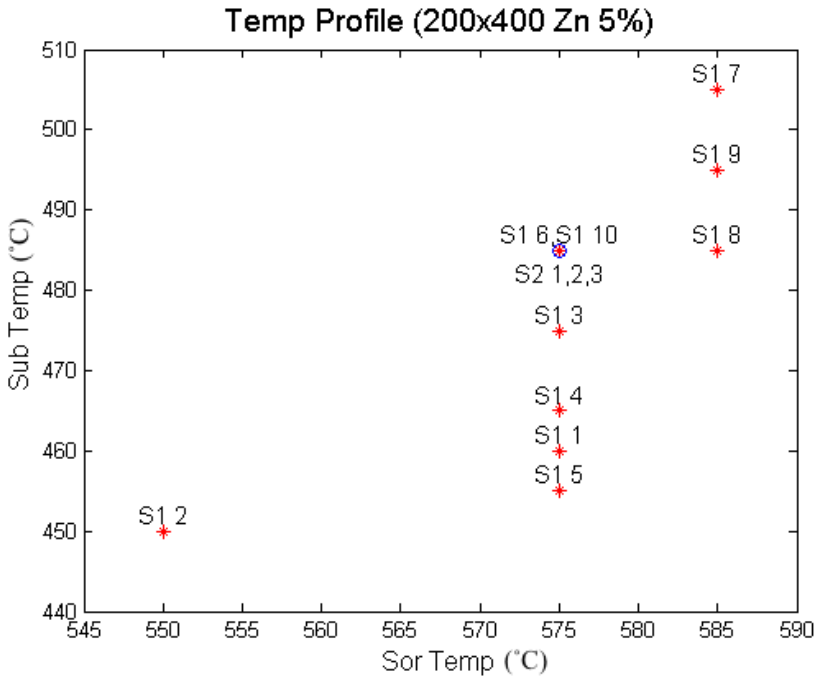


FIGURE 3.2: SOURCE AND SUBSTRATE TEMPERATURES FOR SET II (⊗)AND SET I(*).

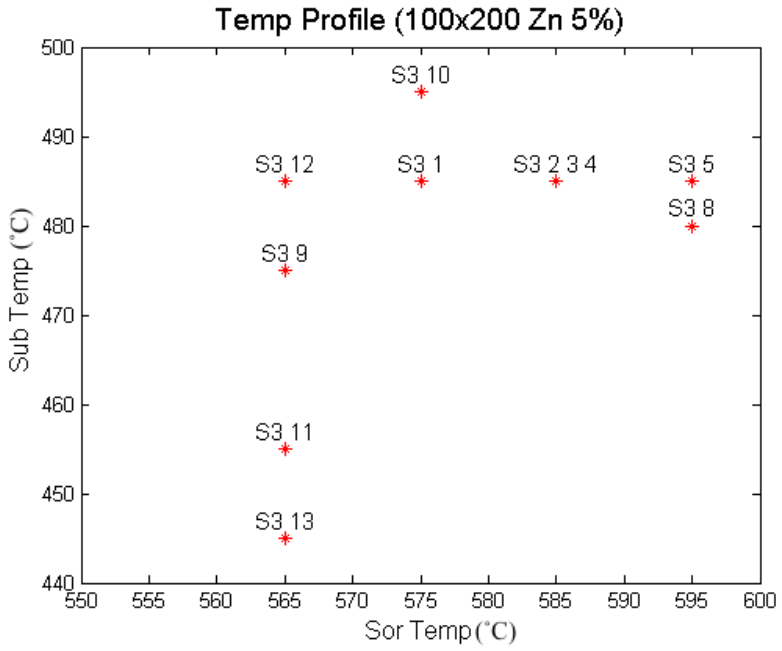
3.1.3 SET III

Set I is compared to Set II and the p/d ratio resulting in the best quality growth of CdTe is identified. A p/d ratio of 2 yielded superior results and this ratio is used for Sets III-V. The diameter of the pillars for Set III is reduced from 200 nm (Set II) to 100 nm and the pitch is reduced to 200 nm to maintain a p/d of 2. The goal for Set III is to identify the optimum source (T_{sor}) and substrate (T_{sub}) temperatures for CdTe growth on 100 nm Si(211) pillars for Zn doping values of 5% and 10%.

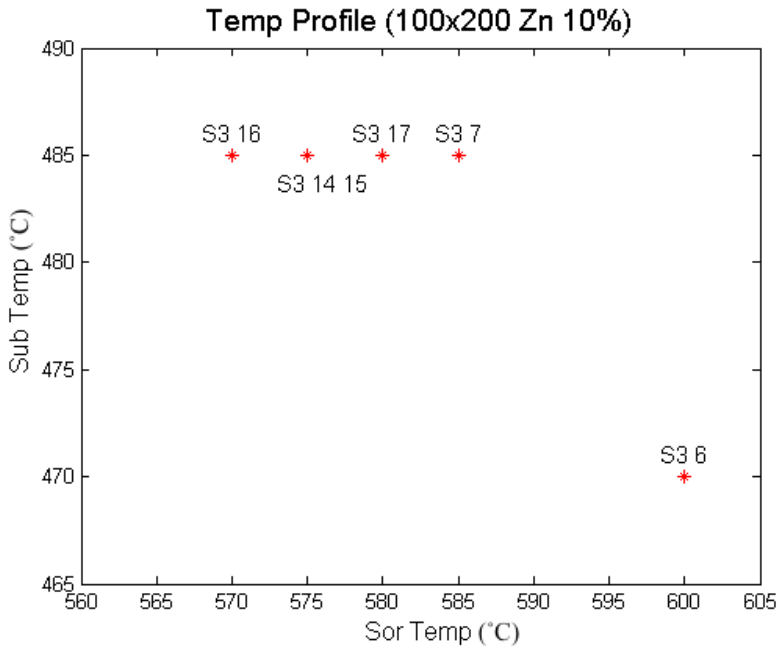
A Zn doping of 10% is included in this study since it is a common value used in X-ray imaging applications [1, 10, 20, 21]. The values of substrate and source temperatures are varied (as shown in Table 3.4), since a change in the pattern, etch method, and the use of a CdTe source with 10% Zn. Based on the literature, a high source temperature is required to sublimate the source, since there are Zn-Te bonds in the material which have a melting point of 1,295˚C compared to a CdTe melting point of 1,041˚C [63, 66]. Fig. 3.3 includes a comparison of the source and the substrate temperatures examined in Set III for 5%, Fig. 3.3(a) and 10% Zn, Fig. 3.3(b).

TABLE 3.4: SET III-GROWTH OF CDTE WITH 5% AND 10% ZN ON SI(211) 100 NM PILLARS WITH A 200 NM PITCH

Fabrication Parameters	Sample name	Tsor (˚C)	Tsub (˚C)	Reactor Pressure (Torr)	Substrate	Pitch/Diameter (nm)	Zinc Doping (%)	Deposition time (min)
Optimization of Deposition Temperatures	S3_1	575	485	1.5	Si (211)	200/100	5	3
	S3_2	585	485	1.5	Si (211)	200/100	5	3
	S3_3	585	485	1.5	Si (211)	200/100	5	1:30
	S3_4	585	485	1.5	Si (211)	200/100	5	2
	S3_5	595	485	1.5	Si (211)	200/100	5	2
	S3_6	600	470	1.5	Si (211)	200/100	10	5
	S3_7	585	485	1.5	Si (211)	200/100	10	2
	S3_8	595	480	1.5	Si (211)	200/100	5	2
	S3_9	565	475	1.5	Si (211)	200/100	5	3
	S3_10	575	495	1.5	Si (211)	200/100	5	1:45
	S3_11	565	455	1.5	Si (211)	200/100	5	3
	S3_12	565	485	1.5	Si (211)	200/100	5	3
	S3_13	565	445	1.5	Si (211)	200/100	5	3
	S3_14	575	485	1.5	Si (211)	200/100	10	5
	S3_15	575	485	1.5	Si (211)	200/100	10	8:30
	S3_16	570	485	1.5	Si (211)	200/100	10	3
	S3_17	580	485	1.5	Si (211)	200/100	10	5



(a)



(b)

FIGURE 3.3: SOURCE AND SUBSTRATE TEMPERATURE PROFILES FOR SET III FOR (A) 5% ZN DOPING AND (B) 10% ZN DOPING

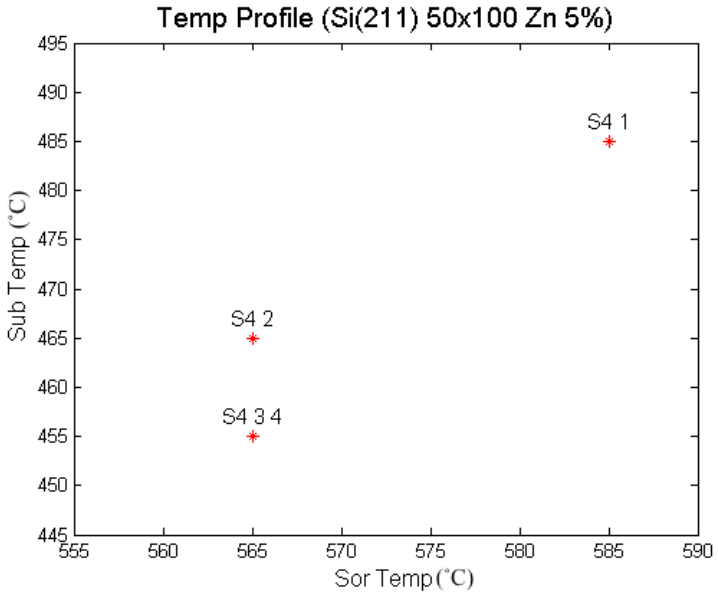
3.1.4 SET IV

A p/d ratio of 2 is the ratio used for Set IV. The diameter of the pillars for Set IV is reduced from 100 nm (Set III) to 50 nm and the pitch is reduced from 200 nm (Set III) to 100 nm to maintain a p/d ratio of 2. The pillar diameter is reduced in order to help reduce the strain that occurs as a result of the lattice mismatch. The goal for Set IV is to identify the optimum source (T_{sor}) and substrate (T_{sub}) temperatures for selective CdTe growth on the 50 nm by 100 nm pattern. The 50 nm by 100 nm pattern is the smallest pattern in this study. Set IV again examines the growth of CdTe with Zn doping values of 5% and 10% Zn.

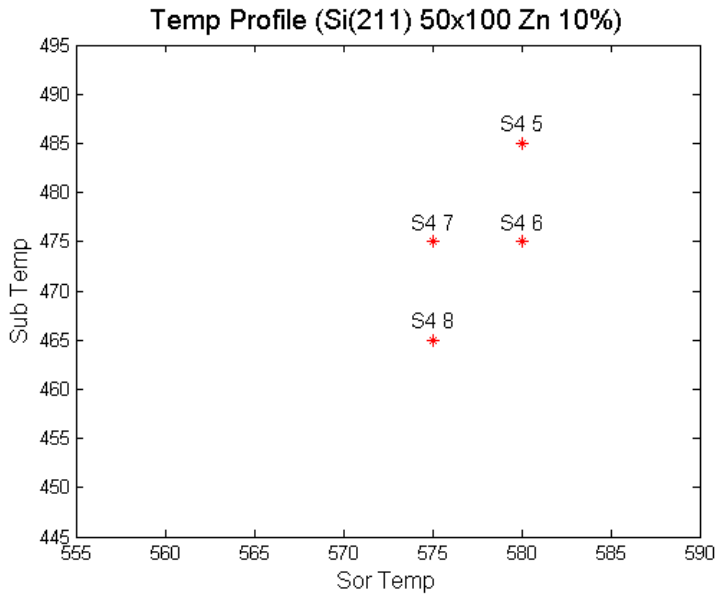
The values of the substrate and source temperature are varied (as shown in Table 3.5), to adjust for the reduction in pattern size, and for the CdTe growth with 10% Zn. Fig. 3.4 includes the source and the substrate temperatures examined in Set IV for 5% and 10% Zn. The temperatures are adjusted in this manner in order to observe the quality of the growth on individual Si pillars. This resulted in the source and substrate temperatures being reduce from the previous Set III. The CdTe with 5% Zn growth temperatures for sample S4_1, in Set IV, are the same as the growth temperatures in Set III, sample S3_2. The growth for S4_5, with 10% Zn, in Set IV, has the same temperature as the best growth in Set III, sample S3_17. When the best temperatures from Set III are used, for Set IV, the CdTe film is thicker and the pillars are difficult is see. In order to reduce the thickness for both the 5% and 10% Zn samples, both source and substrate temperatures are reduced.

TABLE 3.5: SET IV-GROWTH OF CDTE WITH 5% AND 10% ZN ON SI(211) 50 NM PILLARS WITH A 100 NM PITCH

Fabrication Parameters	Sample name	Tsor (˚C)	Tsub (˚C)	Reactor Pressure (Torr)	Substrate	Pitch/Diameter (nm)	Zinc Doping (%)	Deposition time (min)
Optimization of Deposition Temperatures	S4_1	585	485	1.5	Si (211)	100/50	5	2
	S4_2	565	465	1.5	Si (211)	100/50	5	2
	S4_3	565	455	1.5	Si (211)	100/50	5	2
	S4_4	565	455	1.5	Si (211)	100/50	5	2
	S4_5	580	485	1.5	Si (211)	100/50	10	3
	S4_6	580	475	1.5	Si (211)	100/50	10	3
	S4_7	575	475	1.5	Si (211)	100/50	10	3
	S4_8	575	465	1.5	Si (211)	100/50	10	5



(a)



(b)

FIGURE 3.4: SOURCE AND SUBSTRATE TEMPERATURE PROFILES FOR SET IV FOR (A) 5% ZN DOPING AND (B) 10% ZN DOPING

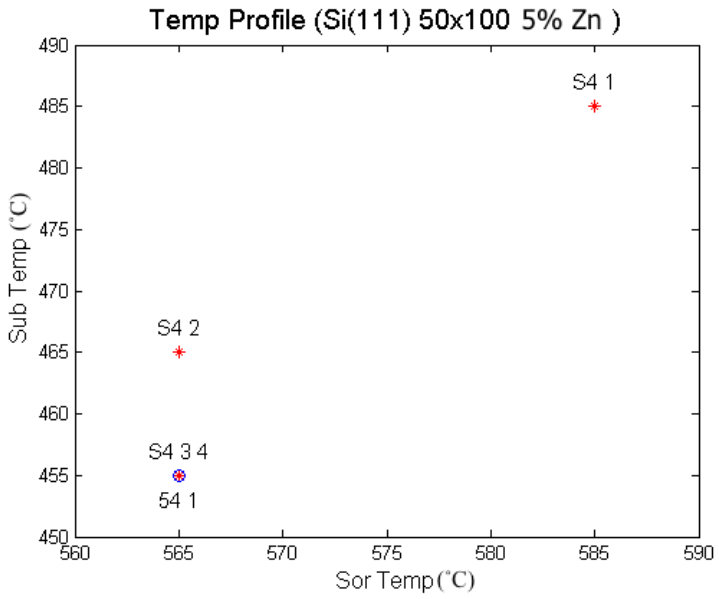
3.1.5 SET V

Set V examines the growth of CdTe on Si(111) 50 nm diameter pillars with a pitch of 100 nm (p/d=2). The CdTe growth is examined on Si(111) substrates for 5% and 10% Zn doping values. The (111) orientation is examined in this study, since it is the preferred growth orientation of CdTe films [32]. CdTe growth in the (111) orientation favors the formation of twins at the interface [32, 34, 89]. CdTe twins are prevalent in the (111) growth direction. The source and substrate temperatures are 565˚C and 455˚C, respectively for the 5% Zn sample, and 575˚C and 465˚C, respectively for 10% Zn sample. These are the source and substrate temperatures identified from the 50 nm by 100 nm pattern growth that produced the highest quality growth. The use of the same temperatures from Set IV and Set V, allows the growth on

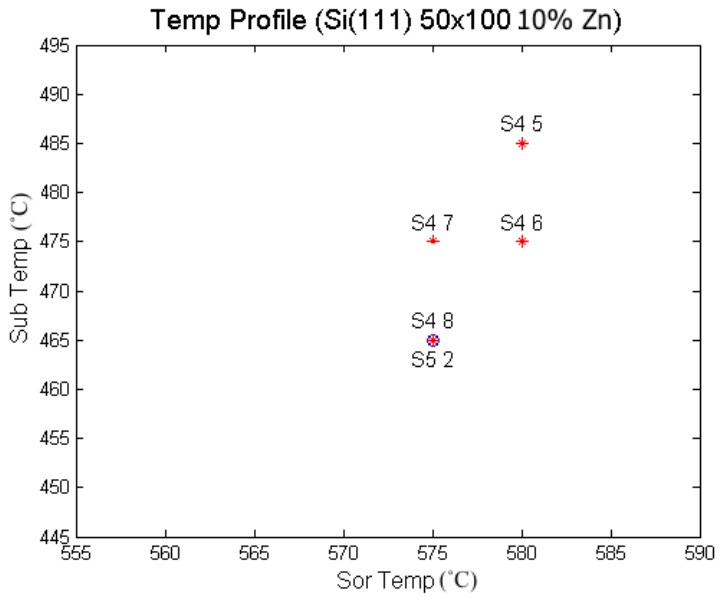
two different substrates to be compared. Table 3.6 includes the growth parameters used for Set V. Fig. 3.5 includes a comparison of the source and the substrate temperatures examined in Set V for 5% and 10% Zn.

TABLE 3.6: SET V-GROWTH OF CDTE WITH 5% AND 10% ZN ON SI(111) 50 NM PILLARS WITH A 100 NM PITCH.

Fabrication Parameters	Sample name	Tsor (˚C)	Tsub (˚C)	Reactor Pressure (Torr)	Substrate	Pitch/Diameter (nm)	Zinc Doping (%)	Deposition time (min)
Change of Substrate Si (111)	S5_1	565	455	1.5	Si (111)	100/50	5	2
	S5_2	575	465	1.5	Si (111)	100/50	10	5



(a)



(b)

FIGURE 3.5: SOURCE AND SUBSTRATE TEMPERATURE PROFILES FOR SET V FOR (A) 5% ZN DOPING AND (B) 10% ZN DOPING. PARAMETERS FOR SET IV (*) COMPARED TO THOSE FORM SET V(⊗)

3.2 Substrate Selection and Acquisition

A Si wafer for CdTe growth with a (211) surface orientation is used for Sets I-IV. The (211) orientation is used since low etch pit density and high device performance have been reported for CdTe on the (211) surface [32, 34]. The device noise and breakdown voltage are both related to the amount of defects in the material. CdTe grown on Si (211) results in higher quality growth compared to other orientations [34]. The Si nanopattern and use of Si(211) substrate will further reduce the formation of twins at the interface. Twins and defects that form at the interface only propagate a short distance and decay exponentially at the interface. This is confirmed when analyzing the defect density at the surface of CdTe film, which is $3x10^5$ cm^{-2}

[32]. Si (211) has been known to reduce the amount of twin formation at the interface. Twins have been reported by Smith for CdTe growth on Si(211) [32]. The twins are present at the interface and did not propagate to the surface of the grown CdTe layer. Si(111) will also be examined for Set V, since it is the preferred orientation for CdTe growth, and will be compared to CdTe growth on Si(211). The growth of CdTe on Si will be used to grow an initial seed layer of CdTe and other methods like MBE will be used to grow a thicker high quality layer.

The Si (111) and Si (211) wafers used are from University Wafer. The Si(211) wafer is a 3-inch wafer, n-type, and polished on both sides. The Si(111) wafer is a 3-inch wafer, n-type, and polished on one side.

3.3 Substrate Pattern Process

3.3.1 Sample Preparation

A dicing saw is used to cut the 3" Si(211) and Si(111) wafers into 1 cm by 1 cm squares. The wafer surface is cleaned prior to the photoresist application. Sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) are used in combination to create a Piranha solution, which strips the wafer surface of organic materials.

The following steps are followed to make the Piranha solution:

Step 1: A quantity of 10 ml H_2O_2 is poured into a beaker containing 50 ml of H_2SO_4.

Step 2: The Piranha solution is poured into a Teflon dish that contains the Si samples.

Step 3: The Piranha solution and the samples are heated to 110˚C on a hot plate for 8 minutes.

Step 4: The samples are removed from the Piranha solution, rinsed in a beaker containing deionized water for 10 min, and then dried with nitrogen (N_2) gas.

3.3.2 PHOTORESIST APPLICATION

Photoresist (PR) is applied to the wafer surface to begin the patterning process. Prior to the application of the PR, hexamethyldisilazane (HMDS), an adhesion promoter, is used to help the PR stick to the substrate. The PR used in this study is NEB-31, a negative PR, which when exposed to an electron beam, changes chemically and becomes more difficult to dissolve, thus creating the negative pattern on the substrate wafer. NEB-31 is also used in this study since it results in exceptional resolution at the nanoscale.

The following steps are followed during PR application:

Step 1: The substrate is placed on a spinner and coated with 0.2 mL of HMDS from a pipette. The spinner speed is ramped up to 3000 rpm and spun for 30 seconds. This creates a thin layer of HMDS on the wafer surface.

Step 2: After the spinner comes to a stop, NEB-31 is applied to the substrate surface and the speed is ramped up to 3000 rpm and spun for 30 seconds.

Step 3: The substrate is then removed and placed on a hot plate at 110°C for 2 minutes. This results in a 300 nm thick layer of NEB-31, Fig. 3.6.

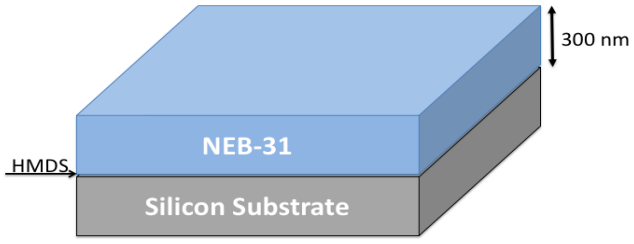


FIGURE 3.6: APPLICATION OF HMDS AND 300 NM OF NEB-31ON THE SI WAFER SURFACE.

3.3.3 Electron Beam Lithography and Development

An electron beam (E-beam) lithography tool (JEOL JBX-6300fs) is used to pattern Si(211) and Si(111) substrates with the pillar diameter, pitch values, and E-beam parameters shown in Table 3.7. The accelerating voltage is 100 kV, the apertures are 60 µm or 130 µm, and electron beam current ranges from 2 nA to 400 pA. The 60 µm aperture corresponds to Aperture 6, and the 130 µm aperture corresponds to Aperture 7 on the tool. The use of two different apertures is required, since aperture 6 has a current range between 50 pA and 2 nA, and aperture 6 has a current range between 2 nA and 7 nA.

Table 3.7: Pillar diameter, pitch and E-beam parameters for Set I-V experiments.

Set	Pitch	Pillar Diameter	Pitch/Diameter Ratio	E-Beam conditions
1	600 nm	200 nm	3	Aperture 7, 6 nA
2	400 nm	200 nm	2	Aperture 6, 2 nA
3	200 nm	100 nm	2	Aperture 6, 400 pA
4	100 nm	50 nm	2	Aperture 6, 400 pA
5	100 nm	50 nm	2	Aperture 6, 400 pA

The E-Beam software converts a computer aided design (CAD) file to graphic data system (GDS) format so that the tool software can read the pattern. The files that are used to execute the pattern are in job definition format (JDF) and standard data file (SDF) format. The JDF file contains the GDS file, the pattern array, the beam spacing, and the charge density settings. The SDF file specifies the position of the holder, position offset of each pattern, and the

beam conditions (accelerating voltage, beam current, and charge density). The maximum size of each CAD file pattern is 500 µm x 500 µm. Fig. 3.7 illustrates a 5 by 5 array of the 500 µm x 500 µm pattern, which results in a final write area of 6.25 mm^2. The area to be scanned by the electron beam will result in circular pillars once the patterning process is complete. During the E-beam process, the scanned area is divided into these small 500 µm x 500 µm rectangles, and the pillars are initially shaped as hexagons in the pattern file, as illustrated in Fig. 3.7. The electron beam scans through each hexagon, with a pre-defined E-beam spacing. The E-beam condition is specified by the beam current, which depends on the resist sensitivity. These parameters ensure that the pattern does not result in larger dimensions than those specified in the CAD and GDS files. The cassette holder has dimensions of 2 cm by 1 cm, which allows for two Si (1 cm by 1 cm) samples to be placed in the holder during each write process.

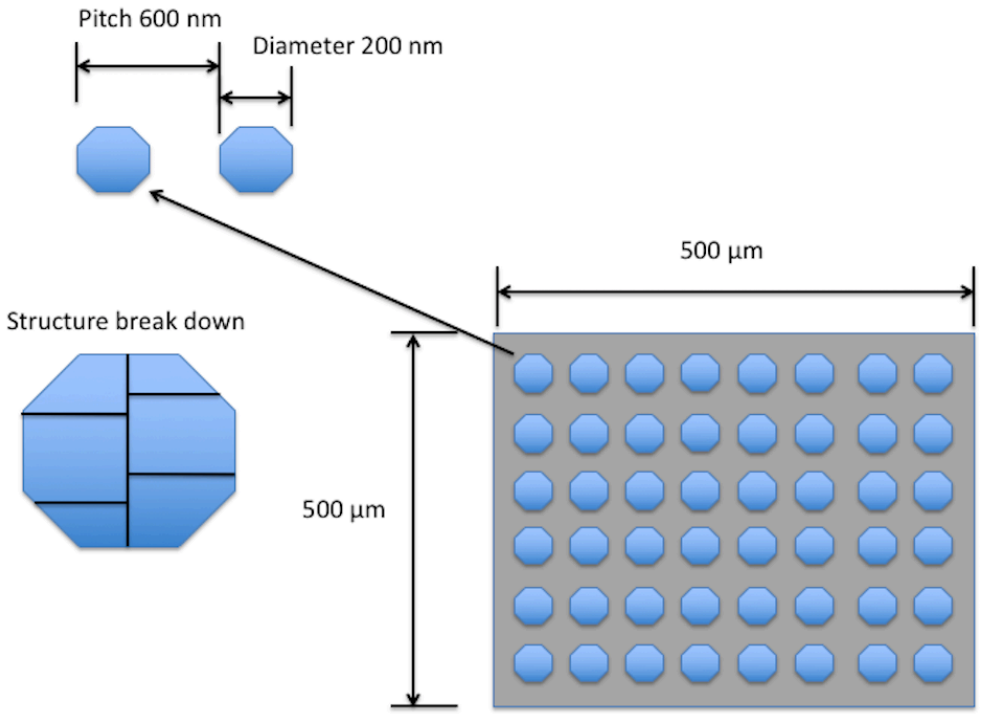


FIGURE 3.7: CAD IMAGE USED TO WRITE THE PATTERN ON THE SUBSTRATE. IMAGE SHOWS A 500µM X 500µM WRITE AREA.

The following steps are followed during the E-beam process:

Step 1: The substrates are placed on a cassette holder, which is then placed in the vacuum chamber of the E-beam tool and pumped down to $1x10^{-4}$ Pascal.

Step 2: A series of adjustments are made to align the beam.

Step 3: A nod on the outside of the E-Beam tool is used to select the desired aperture. Using the software, the beam condition file is loaded and the current condition is verified.

Step 4: The E-beam tool scans the electron beam across the sample to create the desired pattern specified by the GDS file as illustrated in Fig. 3.8. The electrons have the same effect on the PR as photons coming from light. The key difference is that the photon energy is absorbed in one step, while electrons release their energy gradually as they scatter throughout the PR. In the case of the electrons, the electron interactions with the PR change the chemistry of the PR molecules, and the PR becomes less soluble.

Step 5: When the E-beam write is finished, the cassette is taken out and the substrate is removed.

Step 6: The substrate is baked for 2 minutes at 90°C to change the chemistry of the exposed PR. This further strengthens the bonds of the exposed PR, and it becomes more resistant to the developer.

Step 7: The substrate is developed in a MF-321 solution for 40 seconds in order to remove the non-exposed PR. The exposed area is non-soluble to the developer, and the non-exposed area is soluble to the developer. A schematic of the patterned substrate after this step is illustrated in Fig. 3.9.

Step 8: The substrate is rinsed in DI water for 10 minutes, and dried with nitrogen (N_2) gas.

Fig. 3.9 illustrates the resulting pattern, where the PR pillars (exposed area) are formed by removal of the unexposed area.

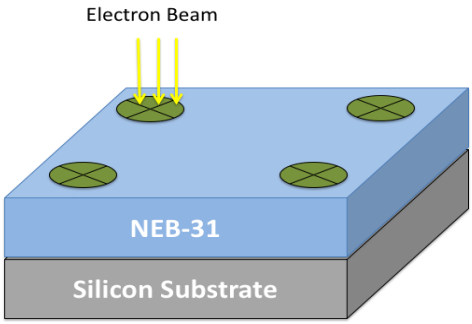


FIGURE 3.8: EXPOSURE OF THE PHOTORESIST PATTERNED AREAS TO THE ELECTRON BEAM.

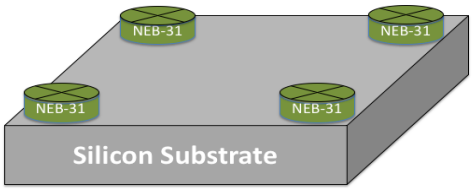


FIGURE 3.9: PATTERNED PHOTORESIST AFTER DEVELOPER STEP.

3.3.4 DRY ETCHING PROCESS

The substrate is etched in an Oxford Plasma Lab and the method used is an anisotropic reactive ion etch (RIE). This process combines both plasma and sputtering (ion milling), through an electrochemical process that results in chemical reactions which create ionized reactive atoms. A schematic of the etch processes is illustrated in Fig. 3.10. The gases employed for the etch process for Sets I and II are sulfur hexafluoride (SF_6), argon (Ar) and oxygen (O_2). The SF_6 is

replaced with CF_4 for Sets III, IV and V, since the pillar diameter is smaller for these samples and a slower etch rate is required to avoid over etching at these small dimensions.

The plasma is created using radio frequency (RF) power by applying an oscillating electric field to the etch gas. The oscillating electric field ionizes the gas molecules by stripping them of electrons, and this creates a plasma with a positive charge. The ionized gas contains $SF_{(1-5)}^{+}$ ions. The wafer is negatively charged by an accelerating voltage, and this causes the ions to accelerate towards the wafer, thus striking and etching the surface.

Sputtering occurs when high energetic ions (Ar^{+}) hit the surface and remove atoms from the surface of the substrate. Sputtering is a highly anisotropic directional etch process. For sputtering to occur the Ar^{+} ions hit the surface of the wafer and remove the substrate atoms. This is the result of the Ar^{+} ions having a high kinetic energy.

By-products $SiF_{(1-2)}^{+}$, are created on the substrate surface during the etching process. The by-products need to be removed since they form a layer that is harder to etch. The by-products form on the sides of the pillars. Oxygen (O_2) helps to remove the by-products. The percent O_2 is tested for optimum pillar shape and is varied between 20% and 50%. As the percent O_2 is increased, more by-product is removed, and the walls of the pillars become straight.

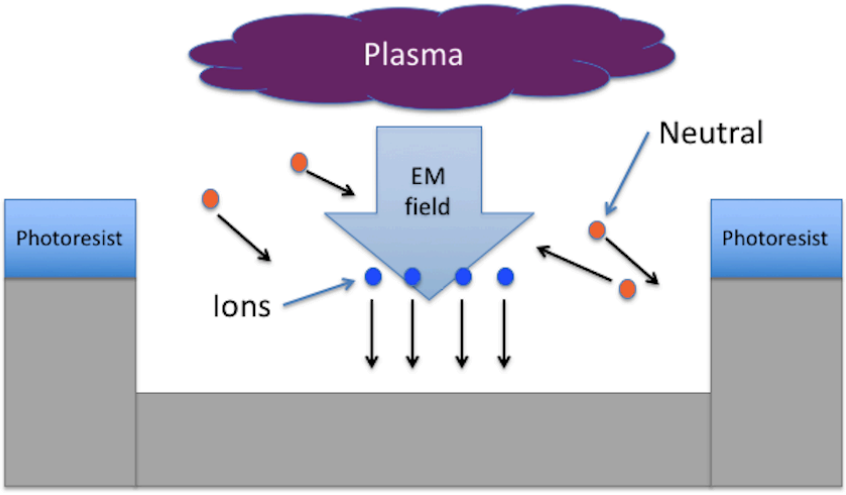


FIGURE 3.10: SCHEMATIC OF REACTIVE ION ETCH (RIE) METHOD.

The substrate is etched using the following procedure:

Step 1: The chamber pressure is pumped to 30 mTorr.

Step 2: The chamber is purged with Ar to remove any residual gases that are present.

Step 3: The gases (SF_6, O_2, and Ar) are pumped into the chamber. The parameters for the gases are 30 sccm for SF_6, 40 sccm for CF_4, 15 sccm for O_2, and 5 sccm for Ar [90].

Step 4: The chamber pressure is stabilized and the RF power is turned on to approximately 100 W, and the accelerating voltage is set to 20 V. The ions are accelerated to the surface during a predetermined etch time.

Step 5: Once etching is complete, the chamber is purged with Ar gas to remove the remaining gases left following the etch process.

Step 6: The chamber is brought back to atmospheric pressure to allow the substrate to be removed.

The profilometer is used to measure the pillar height in order to determine the etch rate (approximately 140 nm/min of Si). After the etch process, PR remains on the surface of the pillars as shown in Fig. 3.11.

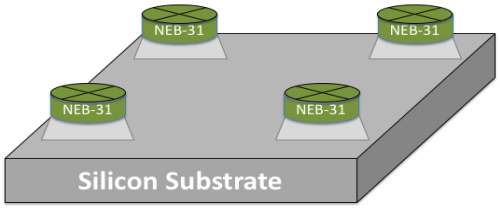


FIGURE 3.11: PHOTORESIST LEFT ON PILLARS AFTER THE REACTIVE ION ETCH (RIE) PROCESS.

3.3.5 PHOTORESIST REMOVAL PROCESS

The substrate is placed in a Piranha solution to help remove the remaining NEB-31 PR shown in Fig. 3.11. The removal of the PR is performed as follows:

Step 1: A Piranha mixture of 50 ml H_2SO_4 and 10 ml H_2O_2, is created by pouring H_2O_2 into a beaker containing H_2SO_4.

Step 2: The Piranha solution is poured into a Teflon dish over the Si substrate.

Step 3: The Piranha solution and samples are heated to 110˚C on a hot plate for 8 minutes.

Step 4: The substrate is removed, rinsed in a beaker with deionized water for 10 minutes, and is dried with nitrogen (N_2) gas.

Step 5: The substrate is placed in a beaker filled with acetone for 8 hours.

Step 6: The substrate is then submerged in methanol for 10 minutes, rinsed with DI water for 10 minutes, and dried with N_2 gas.

Fig. 3.12 illustrates the final patterned substrate.

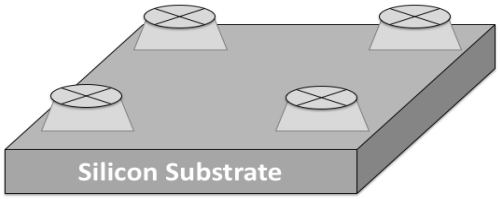


FIGURE 3.12: FINAL PATTERNED SUBSTRATE

3.3.6 PATTERN CHARACTERIZATION

A (FEI NNS450) scanning electron microscope (SEM) is used to characterize the patterned surface, to measure the diameter of the Si pillars, and to determine if the PR is removed from the top of the pillars. The SEM operates at a beam voltage of 10 kV to 15 kV, at a working distance of 5 mm. Immersion mode is used in order to obtain higher resolution at higher magnification. A tilt angle of 45˚ used in order to view the shape of the Si pillars.

The average pillar diameter and pitch for each Set is determined by measuring 20 pillars in four different locations on the patterned Si sample. The targeted and the measured average pillar and pitch values, along with the calculated pitch/diameter ratios, are listed in Table 3.8. Each sample is identified by the notation Si211-S2_1, which indicates the type of substrate (Si211), the Set (S2), and the experiment from that set (1).

TABLE 3.8: PILLAR DIAMETER, PITCH, AND PITCH/DIAMETER RATIO FOR EACH SET OF EXPERIMENTS

Sample	Desired Pitch	Measured Pitch (Average)	Desired Diameter	Measured Diameter (Average)	Pitch/Diameter Ratio
Si211-S1_1	600 nm	592 nm	200 nm	204 nm	2.9
Si211-S2_1	400 nm	403 nm	200 nm	191 nm	2.11
Si211-S3_1	200 nm	205 nm	100 nm	94 nm	2.18
Si211-S4_1	100 nm	106 nm	50 nm	54 nm	1.96
Si111-S5_1	100 nm	108 nm	50 nm	56 nm	1.93

3.4 CdTe Growth on Patterned Si(211) and Si(111) Substrates using the CSS Method

3.4.1 SURFACE PREPARATION

Before deposition, the Si samples are prepared by (1) removing the organic contaminates from the surface, and (2) removing the oxide layer on the surface [61]. In the first step, the Si samples are placed in a piranha solution to remove organics from the surface. The samples are then placed in a buffered oxide etch (BOE) solution to remove the native oxide which is approximately 2 nm thick. A solution consisting of 50 parts of ammonium fluoride (NH_4F) to 1 part of hydrogen fluoride (HF) or 50:1 is used to create the BOE solution. A Teflon beaker is used for the BOE solution, since it etches glass. BOE is poured into the beaker and the substrate is dipped in the solution for 60 seconds. The substrate is removed, rinsed in a beaker that

contains deionized water for 10 min, and is dried with nitrogen (N_2) gas.

3.4.2 ANNEALING OF CDTE SOURCE DOPED WITH ZN

The bulk CdTe source is annealed prior to each deposition to remove the oxide layer that forms as a result of exposure to the atmosphere. This also helps to remove any materials on the surface of the source. The source anneal recipe is shown in Table 3.9. An anneal time of 10 minutes is used for the CdTe source doped with 5% Zn. When the source is changed to CdTe with 10% Zn the anneal time is increased to 30 minutes for the CdTe source with 10% Zn, to ensure a clean source that it will sublimate during the deposition process.

TABLE 3.9: SOURCE ANNEAL RECIPE

	Purging Steps						Source Anneal	Cooling Step
Time (seconds)	60	60	60	60	60	60	600	120
Helium (SLPM)	0	4	0	4	0	4	0.1	0
Oxygen (SLPM)	0	0	0	0	0	0	0	0
Substrate Temp. (˚C)	0	0	0	0	0	0	0	0
Source Temp. (˚C)	0	0	0	0	0	0	600	0
Pressure (Torr)	0.1	100	0.1	100	0.1	100	5	0.1

3.4.3 CLOSE SPACED SUBLIMATION (CSS)

The close spaced sublimation (CSS) technique is used in this study because it results in higher growth rates compared to other methods, such as metalorganic vapor phase epitaxy

(MOVPE) and molecular beam epitaxy (MBE). The higher deposition rate is the result of the atoms proximity to one another. The atoms are compact in the bulk substrate, versus in power form, this allows for easier transfer of energy from one atom to another atom. The CSS technique involves the sublimation of a source material on to a substrate, where the separation distance is small. This short separation distance in the diffusion process results in high growth rates. The He gas in the chamber helps carry the atoms of the source material and helps in the selective growth process [78]. There is a difference in temperature between the source and substrate and this is the driving force for sublimation of the source material. The deposition takes place under a pressure defined by the vapor pressure of the source material. This vapor pressure is formed by the heated atoms and the gas flow in the chamber. The gas helps to carry the heated atoms and helps in the selective growth process. The CSS layout is shown in Fig. 3.13 and Fig. 3.14.

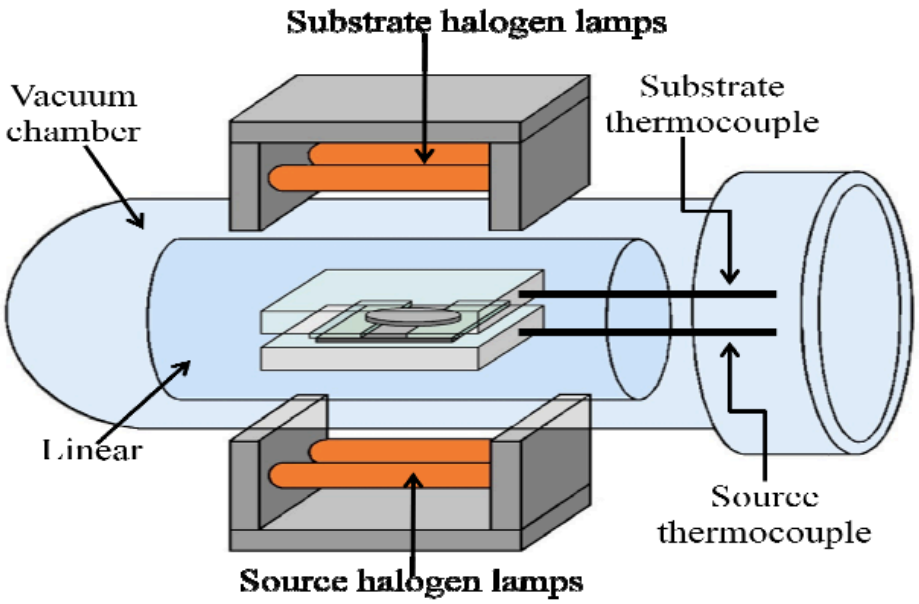


FIGURE 3.13: THE CSS REACTOR LAYOUT [29]

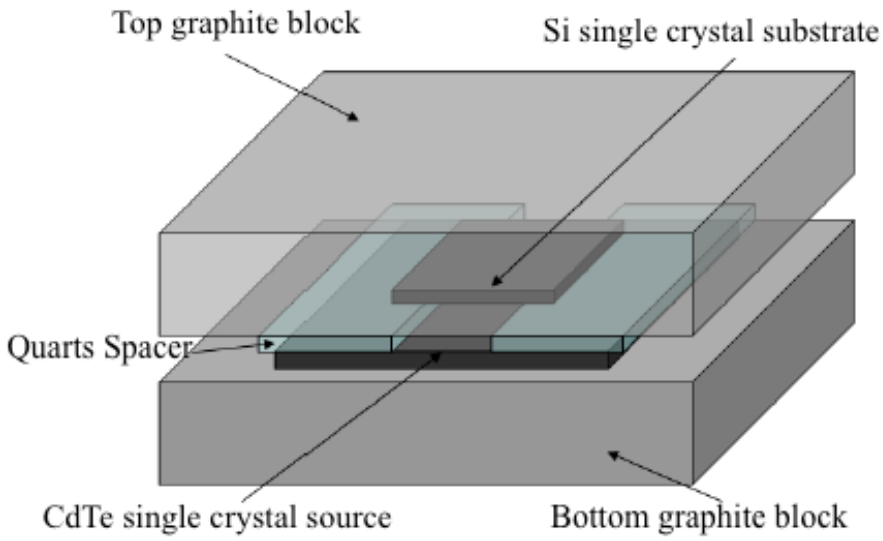


FIGURE 3.14: THE LAYOUT OF THE SOURCE AND SUBSTRATE IN THE CSS CHAMBER [29]

Bulk CdTe (111) with twins is used as the source material from Keystone Crystal Corporation. Two CdTe sources are used in this study, one is doped with 5% Zn and the other is doped with 10% Zn. The Zn doping is varied to better understand the effect on the quality of CdTe growth and on the CdTe/Si interface. TEM analysis will be used to identify the CdTe growth orientation and the quality of the CdTe/Si interface. A CdTe bulk source wafer is used instead of powder CdTe, since it is safer to handle the bulk material, and it results in a more uniform deposition [Escobedo 2010]. Depositions rates of 0.1 to 4680 μm/hr can be achieved using the CSS method [29].

A schematic of the CSS is shown in Fig. 3.13 and Fig. 3.14, where the different parts are connected as followed: (1) the CdTe doped with Zn source is placed on the bottom graphite block, (2) two 1 mm thick glass slides are placed on top of each edge of the source, (3) the substrate is placed on top of the glass slides, (4) the top graphite block is placed on top of the substrate, and (5) the bell jar and liner are positioned to close the chamber. The liner made of quartz glass is placed in between the graphite blocks and the bell jar in order to isolate the CdTe.

The quartz glass bell shaped tube is used to form a seal that allows the pressure in the CSS to drop down to 0.1 Torr.

A MKS mass flow controller monitors the pressure as gas is pumped into the chamber. The MKS mass flow controller compares the pressure to a set value, defined by the user on the software. The MSK mass flow controller adjusts the valve in order to control the flow rate of the gas. Halogen lamps that are rated at 1 kW are placed outside the bell-shaped glass and are used to heat the graphite blocks independently. The halogen lamps are placed in aluminum reflectors, that have a parabolic shape to ensure the graphite blocks are heated to the optimal temperature. Thermocouples are inserted into each graphite block to monitor and control the temperature through the Lab VIEW program.

The CSS is operated by Lab VIEW 7.1 which is used to control the following parameters:

- Time of each step
- Helium flow rate
- Oxygen flow rate
- Substrate temperature
- Source temperature
- Pressure

Operation of the CSS can be summarized by the following steps: (1) the bell jar is positioned to form a seal with the metal plate to prevent atmospheric gases from entering the chamber after the vacuum has been achieved. An O-ring and high vacuum grease ensure that a good seal is made, (2) the chamber is purged and He gas is vented into the chamber four times to ensure that He is the only gas present during the deposition, (3) a MKS mass flow controller controls the valve to allow or prevent He from entering the chamber, (4) the chamber is pumped

down to 1.5 Torr, with a flow rate of He at 0.05 (SLPM), (5) both top and bottom halogen lamps are turned on until a temperature of 300˚C is attained within the graphite blocks (the temperature is monitored by thermocouples inside each graphite block to help control the source and substrate temperatures, which control the growth), (6) then the temperature of the blocks is increased to the desired deposition temperature, (7) CdTe is deposited for a specified time, (8) the graphite blocks are cooled to 400˚C (this is achieved by using a chiller to flow cold water through the top and bottom aluminum blocks that house the lamps and turning off the lamps), and (9) the system is turned off and the source and substrate temperatures are decreased to room temperature.

In this study the source and substrate temperatures are varied to determine the optimum growth parameters.

3.4.4 CdTe Growth Parameters

The deposition parameters that are varied in this study are the source temperature, substrate temperature, and the duration of the deposition step. The pressure is kept at a constant value of 1.5 Torr during the deposition process, and helium flow is kept at a constant rate of 0.05 SLPM.

The CSS temperature profiles are analyzed to determine the ramp up and the ramp down of the source and substrate temperatures as illustrated in Fig. 3.15. The ramp up step is incorporated so that the source and substrate have a minimum ΔT at the beginning of the temperature-stabilizing step. The ramp up step increases both the source and substrate temperatures to 300˚C. The ramp down step allows the source and substrate temperatures to be reduced to the same specified value, and both the source and substrate temperatures are lowered to 400˚C. Since the source and substrate temperatures are set to the same values, sublimation is

prevented during this step. Both ramp steps are implemented to help control the deposition. Better control of the source and substrate temperatures during the deposition helps to prevent a larger ΔT that causes undesired growth.

Table 3.10 illustrates the steps implemented for the CSS deposition process in this study. The first six steps are used to purge the chamber of any atmospheric gases that may be present in the chamber. This is accomplished by reducing the pressure in the chamber and then increasing the pressure by filling the chamber with He gas. This allows the chamber to only be filled with He gas. The next step pumps in He gas and stabilizes the pressure in the chamber to 1.5 Torr. For the temperature ramp up step, the source and substrate graphite blocks are heated to 300˚C. Then the source and substrate graphite blocks are heated to the desired temperatures for the deposition and deposition occurs for a specified time. After the deposition, both the source and substrate temperatures are reduced to 400˚C to stop the sublimation process. Last, the source and substrate lamps are turned off along with the gas, to allow the source and substrate to reach room temperate.

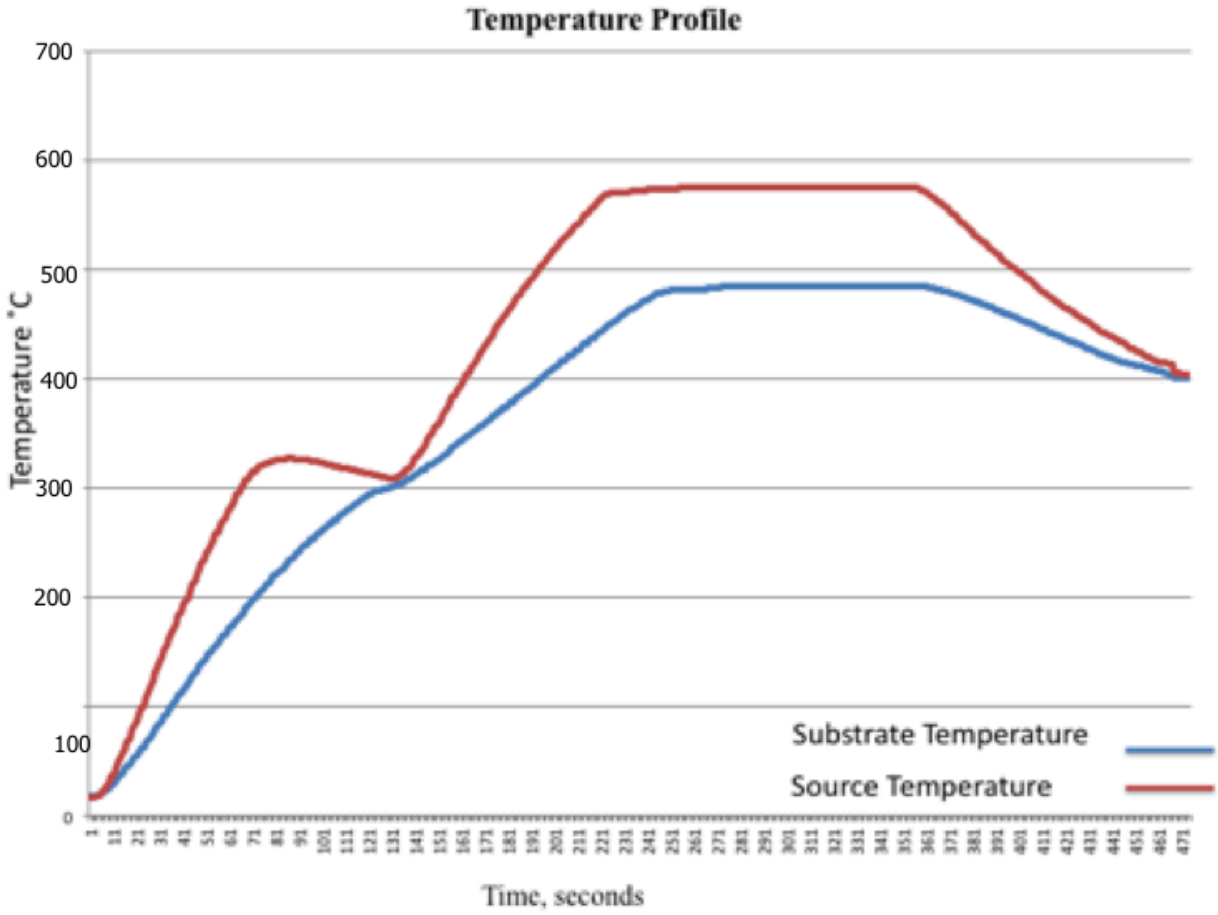


FIGURE 3.15: TEMPERATURE PROFILE OF THE CSS WITH SOURCE TEMPERATURE OF 575˚C AND SUBSTRATE TEMPERATURE OF 485˚C.

TABLE 3.10: CSS DEPOSITION PROCESS FOR INITIAL SAMPLES

	Purging Step						Pressure Stabilization Steps	Temperature Ramp Up Step	Temperature Stabilization Steps	Deposition Step	Temperature Ramp Down Step	Cool Down Step
Time (seconds)	60	60	60	60	60	60	600	180	200	180	290	120
Helium (SLPM)	0	4	0	4	0	4	0.05	0.05	0.05	0.05	0.05	0
Oxygen (SLPM)	0	0	0	0	0	0	0	0	0	0	0	0
Substrate Temp. (°C)	0	0	0	0	0	0	0	300	485	485	400	0
Source Temp. (°C)	0	0	0	0	0	0	0	300	575	575	400	0
Pressure (Torr)	0.1	100	0.1	100	0.1	100	1.5	1.5	1.5	1.5	1.5	1.5

3.5 Material Characterization

3.5.1 SCANNING ELECTRON MICROSCOPE (SEM)

The scanning electron microscope (SEM) (FEI NNS450) is used to characterize the patterned structure, to measure the diameter of the Si pillars, and to determine if the PR is removed from the top of the pillars. The SEM is used in immersion mode, which results in higher resolution at higher magnification. The SEM at used at low magnification (8kX) and high magnification (100kX) to observe the morphology of the samples in this study. The SEM scans the sample with an electron beam, operating at a voltage of 10 kV. The SEM image is the result of secondary electrons being ejected by the electron beam and read by the detector. The SEM is

capable of capturing images with a resolution of 1 nm. The SEM chamber operates at a pressure of 2.44 x 10^{-7} Torr, the working distance is 5 mm, and the stage can be tilted from 0˚ to 45˚.

After removing the samples from the deposited chamber, the samples are characterized in the SEM. The SEM is used to characterize the growth of the grains and help identify the deposition parameters for each Set. The samples with the highest quality growth for each set are selected for the FIB process and then characterized with the using transmission electron microscopy (TEM).

3.5.2 ENERGY DISPERSIVE X-RAY SPECTROSCOPY (EDX)

Energy dispersive X-ray spectroscopy (EDX) is used for analysis of the elemental or chemical composition of the sample. EDX allows for the use of compositional contrast to identify what particular elements are present in the sample and their relative concentration, number of atoms. EDX analysis involves the generation of an X-ray spectrum for the entire scan area of the SEM, specified by the user. The SEM uses backscattered electrons to from an image, and the contrast in the image results from the different atomic number elements and their distribution. The EDX works by analyzing each element, which is done by identifying the unique atomic structure from the set of peaks on its X-ray emission spectrum. Each element has a unique atomic structure allowing unique set of peaks on its X-ray emission spectrum. A high-energy beam of electrons is focused on the sample, and this beam excites an electron in an inner shell and ejecting it. An electron from a higher-energy shell fills the lower shell. The difference in energy between the higher-energy shell and the lower energy shell is released as an X-ray. The number and energy of the X-rays, that are emitted from a specimen are measured by the EDX detector.

3.5.3 X-RAY DIFFRACTION (XRD)

The X-ray diffraction (XRD) (Bruker Advance D8 X-ray Diffractometer) is used to characterize the crystal structure and atomic spacing of CdTe. The XRD works by generating X-rays from a cathode ray tube. This is accomplished by heating a source that emits electrons. Electrons are then accelerated by a high voltage towards the sample. The incident X-rays interact with the sample to produce constructive interference. This interaction is defined by Bragg's Law ($n\lambda=2d\sin(\theta)$). Bragg's Law relates the wavelength of the X-ray radiation (λ) to the diffraction angle (θ), and the lattice spacing (d) of the sample. The reflection is associated with planes of atoms running through the crystal. The X-rays passing through the centers of the atoms of the crystal lattice are reflected towards the detector. The orientation of a particular set of planes is identified by three Miller indices (h, k, l) and their d spacing. The X-ray radiation reflected by the atoms is detected by the X-ray detector. The X-ray source and the detector scan from 20˚ to 90˚ through the 2θ angles, and all the diffraction directions can be obtained for the sample. The Eva software can be used to calculate the full width at half max (FWHM) to determine the quality of the growth material. The FWHM is calculated by finding the max intensity of each peak, dividing the value by half. Then finding the two x-values that correspond to the half max value and subtracting them. The FWHM is in arcseconds and can identify variations in the microstructure, stress, and strain accumulation in the material being analyzed. The larger the value, the more stress and strain is present in the structure.

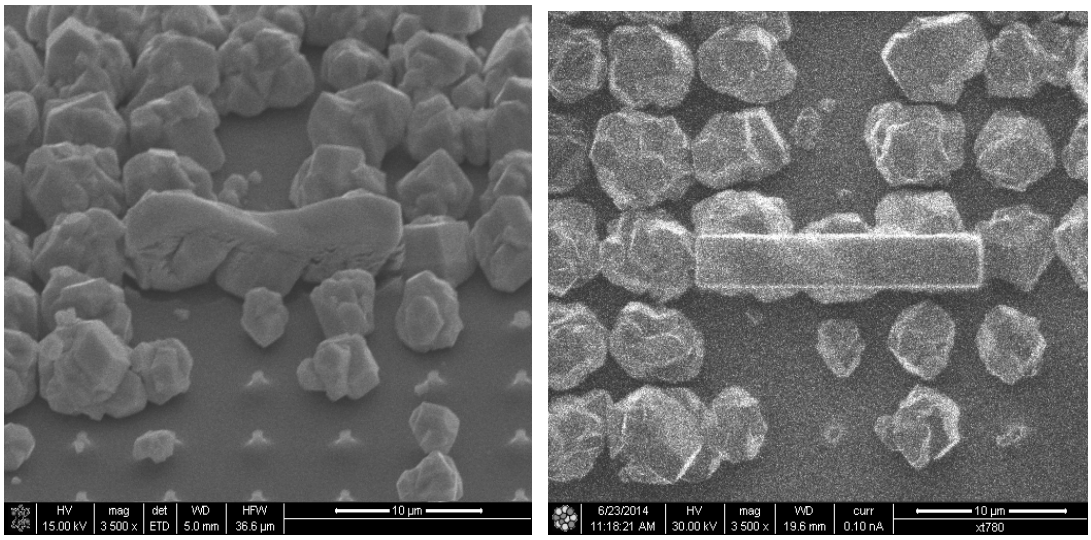
3.5.4 FOCUSED ION BEAM (FIB) FOR TEM SAMPLE PREP

The focused ion beam (FIB) tool uses a finely focused beam of gallium (Ga) ions, for sample milling in the SEM (FEI NNL650). The FIB is used for both high-resolution imaging and

micromachining. The FIB has the capability to use gas-injection for enhanced etching or deposition of materials such as platinum (Pt). The FIB used in this study is located at the Center for Integrated Nanotechnology (CINT), in Albuquerque, NM. TEM samples are selected based on SEM image results. The FIB process uses a Ga source ion beam to micro machine samples down to a thickness of approximately 100 nm. A 100 nm thickness is required in order for the sample to be thin enough so that the electron beam can be reflected and transmitted through the sample, which is how the diffraction pattern and high resolution image are obtained.

The process used to machine a TEM sample is described in five steps:

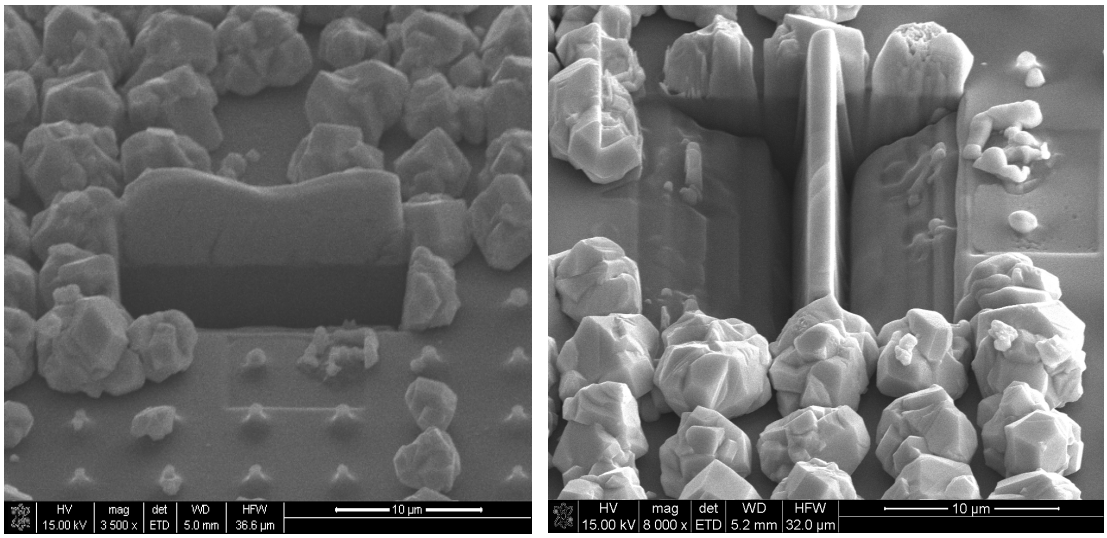
Step 1: The FIB process starts by depositing platinum (Pt) on top of the area of interest of the substrate. This is accomplished by a Pt needle being inserted close to the sample surface. The Pt needle then inserts Pt gas and the ion beam helps bond the Pt to the sample surface. The deposition of Pt prevents the grain of interest from being damaged by the ion beam (Fig. 3.16). The ion beam condition for the deposition of Pt is 30 kV at 0.1 nA. These conditions allow for the deposition of Pt without etching the area of interest.



(a) **(b)**

FIGURE 3.16: PT IS DEPOSITED USING THE ION BEAM AT 30 KV AND 0.1 NA. (A) SHOWS THE SUBSTRATE TILTED AT 52˚, AND (B) IS THE TOP VIEW OF THE DEPOSITED PT.

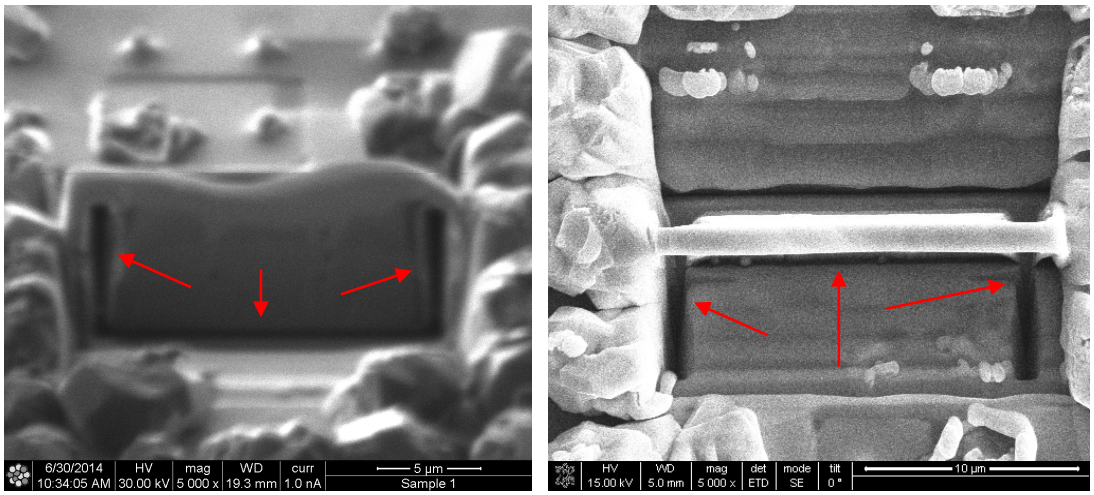
Step 2: Using an ion beam condition of 30 kV and 3 nA, two trenches are etched on each side of the sample (Fig. 3.17). This is to allow the sample to be easily removed from the substrate. Using an ion beam condition of 30 kV and 1 nA, the sample is then thinned until it is approximately 1 µm thick. This is to ensure the sample does not fall off the nanomanipulator.



(a) (b)

FIGURE 3.17: SEM VIEW OF THE SAMPLE AFTER (A) THE FIRST TRENCH AT 3 NA AND (B) AFTER BOTH TRENCHES ARE ETCHED.

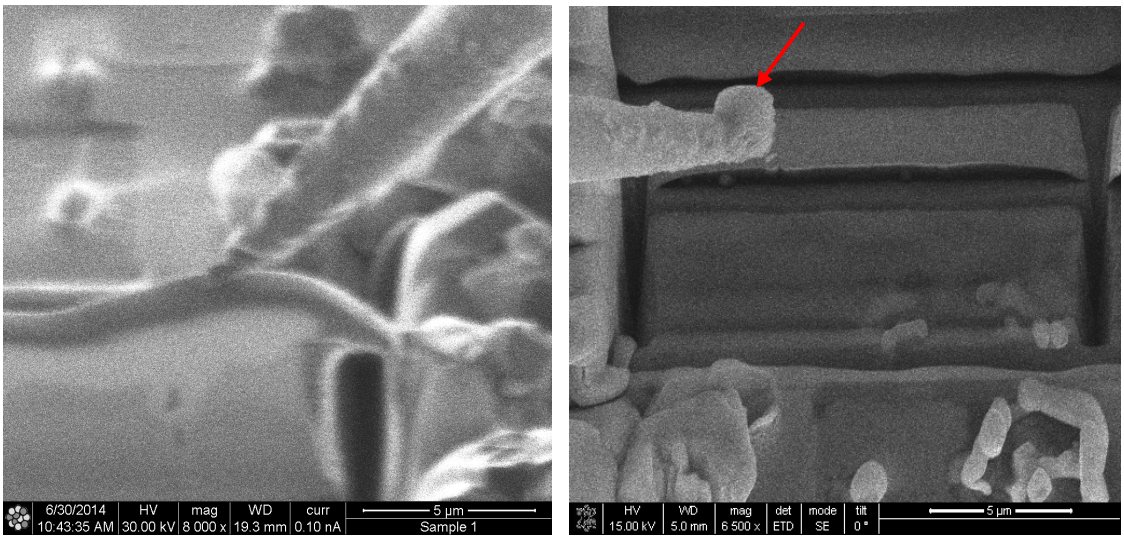
Step 3: A cut is made under the sample that is in the shape of a U. This allow for the sample to be separated from the substrate easily. After the U is complete only a tab of Pt, on each side, holds the sample in place (Fig. 3.18).



(a) (b)

FIGURE 3.18: A U CUT IS MADE TO ALLOW THE SAMPLE TO BE EASILY REMOVED FROM THE SUBSTRATE. (A) ILLUSTRATION OF THE U-CUT FROM THE VIEW OF THE ION BEAM, AND (B) A SURFACE VIEW OF THE CUT CAN BE SEEN ON THE BOTTOM SIDE OF THE SAMPLE.

Step 4: A nanomanipulator probe, that is in the SEM chamber, is inserted to remove the sample from the substrate. The nanomanipulators probe is brought closer until it makes contact with the top of the sample. The needle is then bonded to the sample with Pt at a beam condition of 30 kV and 0.1 nA. Pt is deposited on the sample and on the probe, to ensure the sample stays connected with the probe (Fig. 3.19). After the U-cut, the sample is connected by two tabs, that connect the sample to the substrate (Fig. 3.18 (a)). These tabs help attach the sample to the substrate and prevent the sample from falling over. When the two tabs are cut, the sample is only attached to the nanomanipulators probe and is now free from the substrate.



(a) (b)

FIGURE 3.19: (A) SHOWS THE NANOMANIPULATORS PROBE MAKING CONTACT WITH THE SAMPLE. (B) SHOWS THE BALL ON PT BONDING THE SAMPLE AND NANOMANIPULATORS PROBE TOGETHER.

Step 5: The nanomanipulators probe is used to place the sample on a copper grid at a beam condition of 30 kV and 0.1 nA. This is to ensure the sample stays on the copper grid and does not fall off. The copper grid is used to hold the sample while in the TEM holder. The copper grid allows for the placement of the sample in the TEM and helps with charge dissipation during imaging.

Step 6: Once the sample is placed on the copper grid, it is thinned to approximately 100 nm using a beam condition of 30 kV at 1 nA. A sample width of 100 nm or less is the ideal width to view the same sample in the TEM.

3.5.5 TRANSMISSION ELECTRON MICROSCOPY (TEM)

Two transmission electron microscopy (TEM) tools are used in this study, the first is the (JEOL JEM 3200 FS), a Cryo-TEM, Fig. 3.20 located in the Chemistry department at the University of Texas at El Paso. The Cryo TEM is mainly used for biological samples and can operate at low temperatures. As a result of the nature of the tool, only high resolution transmission electron microscopy (HRTEM) images can be obtained. It is not possible to obtain diffraction patterns from the Cryo TEM since damage to the camera is possible. Dr. Bernal operated the tool and collected data for this study.

FIGURE 3.20: TEM MODEL JEOL JEM 3200 FS AT UNIVERSITY OF TEXAS AT EL PASO FOR THIS STUDY

Most of the HRTEM images and diffraction patterns for this study are acquired using the TEM (FEI TECNAI G2 F20 X-TWIN) located at the Microelectronics Research Center at the University of Texas at Austin, Fig. 3.21. Dr. Palard operated the tool and collected the corresponding TEM images and diffraction patterns.

FIGURE 3.21: TEM MODEL FEI TECNAI G2 F20 X-TWIN AT THE UNIVERSITY OF TEXAS AT AUSTIN

The TEM beam is created by heating a source material that results in the emission of electrons. This is known as thermionic emission and the TEM source is commonly made of tungsten. These electrons are a type of ionized radiation, where the inner-shell electrons are removed by overcoming the attractive force of the nucleus. The electron beam that is produced ranges from 5 nm to 0.1 nm in diameter. When the electrons hit the sample, some electrons are transmitted through the sample while and others scatter secondary electrons from the sample/material. These secondary electrons are detected by the detector and form the HRTEM image. Secondary electrons are either, elastic scattered or inelastic scattered electrons, from the sample. Elastic scattering is dominant when the sample is thin and crystalline. Theses electrons are viewed on the fluorescent screen, when the beam is adjusted for elastic scattering. The fluorescent screen is located at the bottom of the TEM. When capturing an image, the fluorescent screen, Fig. 3.22 is moved to the side and the image is captured on the computer using the

charge-coupled detector (CCD) camera. The image captured by the CCD camera is the image seen on many publications and used for TEM characterization.

The TEM has between 7 to 8 lenses: 1 gun lens, 2 condenser lenses, 1 object lens, 1-2 intermediate lenses, and 1-2 projector lenses (Fig. 3.22). The electrons are emitted from the electron gun. The gun lens controls the divergence and convergence of electron paths emitted from the gun, and controls the current in the beam hitting the specimen. The condenser lens controls the spot size, which affects the beam current. The object lens is the first step to focus and magnify the image. The projector lens controls the final magnification. The first two condenser lenses are adjusted to illuminate the sample which helps to locate the sample. This is done at around 10kX-100kX magnification and the view of the sample is typically several micrometers across. The condenser lenses ensure that the beam is correctly focused on the sample. The objective lens consists of a strong magnetic field (~2 Tesla). The magnetic field acts like a condenser lens and converges the beam and helps to focus it on the sample. The objective lens helps to ensure the electron beam is perpendicular to the sample, to ensure that electrons penetrate the sample. The intermediate lens is used to switch between TEM modes, such as imaging mode, diffraction mode, bright field, and dark field. Bright field mode is the most commonly used mode and is when the aperture is placed in the back focal plane of the objective lens. The bright field mode has a low contrast, where the image is dark with a bright background. While in dark field has a high contrast, where the sample appears bright with a dark background. The diffracted beams result in strong interaction with the specimen which provides more information about planar defects and stacking faults. The draw back to dark field is low light levels on the image. This means the sample must be strongly illuminated and can result in

damage to the sample. The projection lens is used to center the image of the sample on the fluorescent screen or the CCD camera.

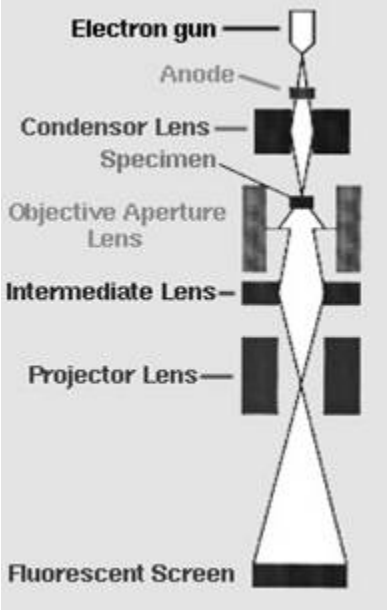


FIGURE 3.22: DIAGRAM OF THE LENS IN THE TEM TOOL [93].

The TEM analysis includes both the (HRTEM) mode and diffraction mode. HRTEM mode is the imaging mode in the TEM, that allows for direct imaging of the atomic structure of the sample. Diffraction mode is a crystallographic technique used to identify the planes of atoms visible in HRTEM mode. Electrons pass through the sample and hit the fluorescent screen or CDD camera and form a periodic pattern of spots that can be interpreted to determine the orientation of planes in the sample.

HRTEM and diffraction patterns can provide the following information:

- The diffraction patterns are used to identify the orientation of each film. Identification of the spots on the diffraction pattern correspond to the orientation of planes of the material. This helps to identify the growth direction of the film and how the pillar affects the growth of the CdTe film.

- The diffraction pattern is used to index the planes of atoms on the HRTEM image. This information helps to identify the planes of atoms on the HRTEM image for each material at the interface. This information also helps to determine the misorientation at the interface.
- The planes on the HRTEM image are verified by confirming the angle between two planes. The values that are measured are compared to the theoretically values.
- The TEM is used to identify the misorientation angle between the CdTe film and Si substrate. The orientation of similar planes, such as (111), are compared for CdTe and Si. The angle between the planes for CdTe and Si is then measured. This value is the misorientation angle between the two films.

HRTEM images are also used to identify defects found at the CdTe/Si interface. Defects include twins, threading dislocations, and precipitates. The length of the threading dislocations is measured from the HRTEM image.

Diffraction Pattern:

The TEM diffraction pattern provides information on the crystal structure, lattice parameter (d_0), and crystallinity. Electrons pass through the sample and hit the fluorescent screen or CDD camera and from a periodic pattern of spots that correspond to an orientation of planes in the sample. The diffraction spots help identify the atomic planes on the HRTEM image. An example of a diffraction pattern for Si(111) is demonstrated in Fig. 3.23. The center spot is the largest and has the highest intensity of electrons since it is generated from the electron beam. The diffraction spots are identified in Fig. 3.23 (b).

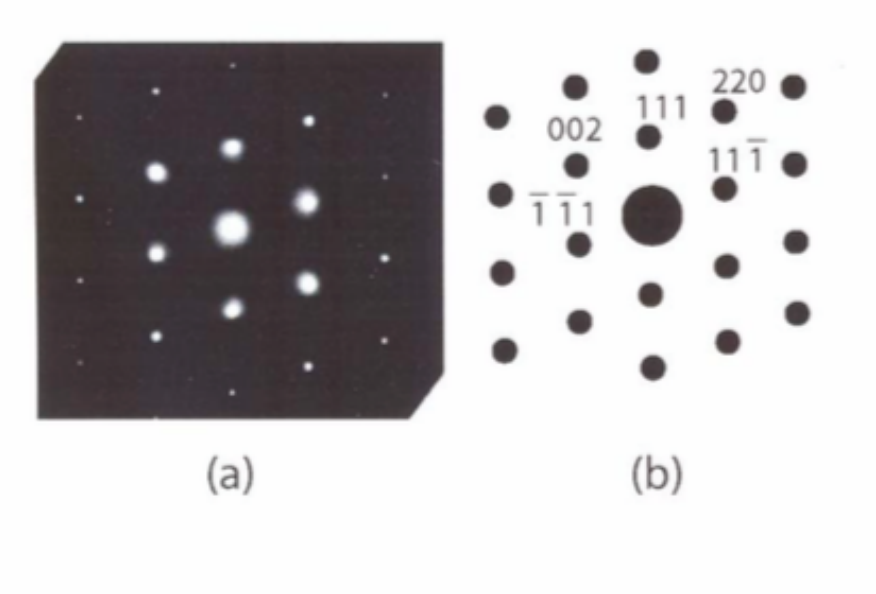


FIGURE 3.23: DIFFRACTION PATTERNS FOR SI GROWN IN THE [111] DIRECTION [91].

The principle of crystallography uses a low index diffraction pattern, such as the (111) for a face centered cubic (FCC) material. The low index orientation is observed close to the transmitted electron beam, and the index increases with distance away from the electron beam spot. The diffraction pattern is part of a three dimensional sphere in reciprocal space. The sphere is broken up into zones called Laue zones. The central zone is called the zero-order Laue zone and the next is the first-order Laue zone. The zero-order Laue zone is often used to identify the rest of the diffraction spots, since the brightest spot is the electron beam, as shown in Fig. 3.23 (a).

The TEM is aligned with the zero-order Laue zone for Si. This is accomplished by tilting the sample in the x and y direction. After the zero order Laue zone is found for Si diffraction pattern the CdTe diffraction pattern is obtained. As a result, the diffraction pattern for CdTe is not always a zero order Laue zone. When the diffraction pattern of two different materials is

taken at the interface, both materials are overlaid on the image, as shown in Fig. 3.24 in a study by Sarney [91].

The way the spots are identified is by measuring the distance between the center beam and another spot this is r_1 and the measurement is repeated for r_2. Then r_1 is divided by r_2 and the resulting value is compared to a chart that has d_2/d_1 and the closets value is matched. The value of d is the lattice spacing between atom planes. Once the value is found, the value of d_2 corresponds to the spot with the measurement of r_1. This process is repeated till most dots are identified.

The spots on the diffraction pattern will be verified using the equation

$$\alpha(\vec{n}, n) = \cos^{-1} \frac{|h_1 \cdot h_2 + k_1 \cdot k_2 + l_1 \cdot l_2|}{\sqrt{h_1^2 + k_1^2 + l_1^2} \cdot \sqrt{h_2^2 + k_2^2 + l_2^2}} \quad (4)$$

Where $\alpha(\vec{n}, n)$ is the angle between planes and (h_i,k_i,l_i) are the Miller indices for each plane. This equation gives the theoretical value for the angle between two planes. This equation is used to help identify and validate the planes on the diffraction pattern.

HRTEM Imaging Planes:

High resolution for the TEM is defined at any magnification greater than 300,000X. For this study, the magnification is between 1MX to 1.5MX. HRTEM allows direct imaging of the atomic structure of the sample, and it is possible to view the atomic planes and defects. The HRTEM image is acquired by switching the TEM into imaging mode. The magnification is increase to 1MX to 1.5MX and the focus is adjusted until the atoms are in view. Then the image is acquired on the CCD camera.

After the image is focused on the area of interest in HRTEM mode, the TEM is switched to diffraction mode to find the zero-order Laue for the sample. This is done by tilting the sample

holder in the x-axis and y-axis. Once the zero-order Laue is found, the diffraction image is taken, the aperture is switched to HRTEM, and then the HRTEM image is taken of the same area. The acquisition of the diffraction and HRTEM images is repeated for each area of interest. The tilt angle for the sample kept constant during CdTe characterization.

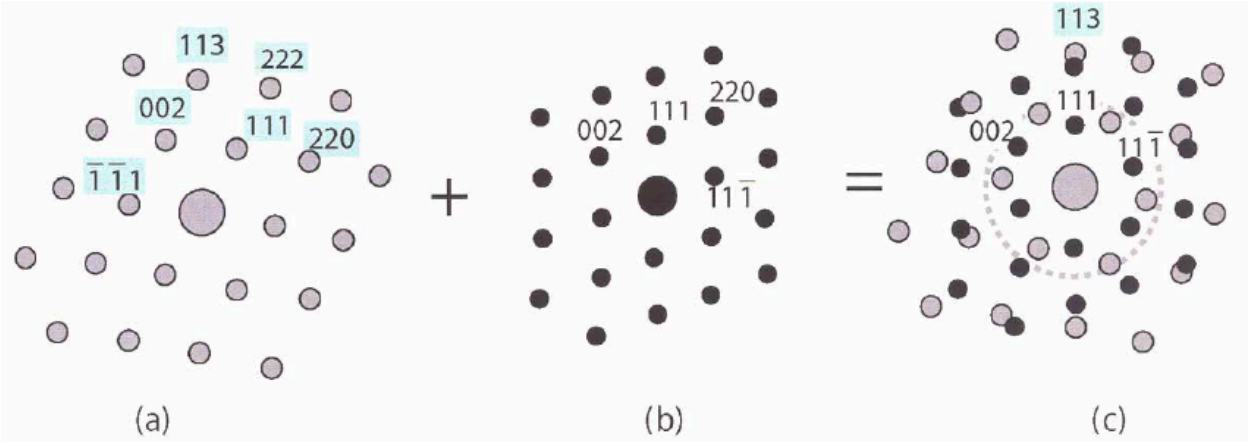


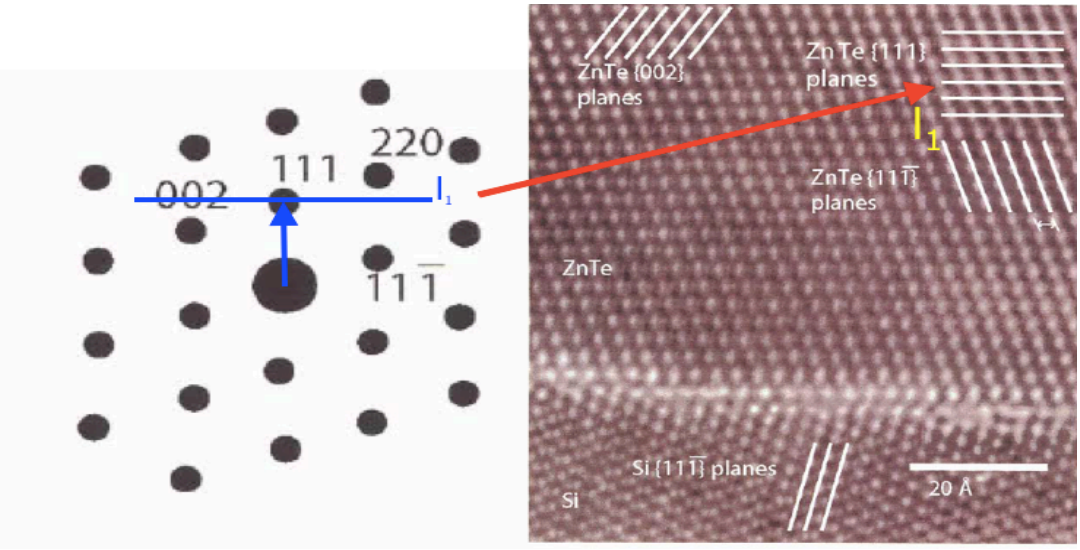
FIGURE 3.24: (A) DIFFRACTION PATTERNS FOR SI. (B) DIFFRACTION PATTERN FOR ZNTE. (C) DIFFRACTION PATTERN FOR SI AND ZNTE INTERFACE [91].

Fig. 3.25 (b) is a HRTEM image of ZnTe growth on Si(111), and will be used to explain how the atomic planes are identified on the HRTEM image. The orientation of the planes is obtained from Fig. 3.24.

The planes on the HRTEM image are identified as described below:

1. The diffraction pattern is indexed as described above.
2. A vector line is drawn from the transmitted beam (center bright spot on diffraction pattern) to the spot of interest l_1 (Fig. 3.25 (a)).
3. A line is drawn that is perpendicular to l_1 from step 2.
4. The perpendicular line from step 3 is transferred to the HRTEM image to determine if the oriented is at the same angle, the red arrow on Fig. 2.25. This step is repeated until all the

planes of interest on the HRTEM are identified (Fig. 3.25 (b)). (modify image (l_1) make 1 bigger and arrow)



(a) (b)

FIGURE 3.25: IDENTIFY OF THE {111} PLANE (A) A VECTOR IS DRAWN PERPENDICULAR TO THE ARROW TO THE {111} DIFFRACTION SPOT (B) {111} LINE IS SUPERIMPOSED ON THE HRTEM IAMGE TO IDENTIFY THE {111} PLANE

Identification of Misorientation:

Once the planes are identified on the HRTEM image, the misorientation angle between similar sets of planes can be calculated between CdTe and Si, across the CdTe/Si interface.

Chapter 4: Results and Discussions

4.1 Pattern Characterization

The parameters used for the four different nano-scale patterns, using NEB-31 as the photoresist. As the pattern dimensions are decreased, the current for the beam condition is reduced. The lithography conditions used to create the substrate patterns for Sets I – V vary, and the pattern strategies to create well-defined features for each set are summarized in Table 4.1.

TABLE 4.1: SUMMARY OF PATTERN PARAMETERS FOR SETS I-V

Set	Substrate	Pitch	Diameter	Beam condition
Set I	**Si(211)**	**600 nm**	**200 nm**	**Aperture 7, 6 nA**
Set II	**Si(211)**	**400 nm**	**200 nm**	**Aperture 6, 2 nA**
Set III	**Si(211)**	**200 nm**	**100 nm**	**Aperture 6, 400 pA**
Set IV	**Si(211)**	**100 nm**	**50 nm**	**Aperture 6, 400 pA**
Set V	**Si(111)**	**100 nm**	**50 nm**	**Aperture 6, 400 pA**

Set I (600 nm x 200 nm) Strategy:

The electron beam condition for Set I (200 nm x 600 nm pattern) is 130 µm Aperture (Ap) with 6 nA, and the dose value (based on the recipe at CINT) is 350 µC/cm^2 for a beam current of 6 nA (Fig. 4.1 (a)). The etch gases used in the RIE process and their respective flow rates are 30 sccm for SF_6, 15 sccm for O_2, and 5 sccm for Ar, with an etch time of 90 seconds. The 50% O_2 results in slightly straight pillar side walls. However, the walls of the pillars are rough with a slight under- cut of the pillars (Fig. 4.2). The 30% O_2 results in curved pillar side walls and are smoother (Fig. 4.3).

Set II (400 nm x 200 nm) Strategy:

When the same beam conditions from Set I are applied to the 200 nm x 100 nm pattern, the pattern is over exposed and PR is observed between the pillars after the develop process. In it can be seen that after the etch process, the edge of the pattern has been etched, and the area in between the pillars is not etched. To help mitigate the over exposure of the pattern, the current is reduced from 6 nA to 2 nA. Fig. 4.4 shows a well-developed pattern with the new electron beam condition of 60 μm Ap with 2 nA. The same dose value of 350 $\mu C/cm^2$ is used for the 200 nm x 600 nm pattern. A well-developed pattern is achieved with the new beam conditions and no PR is found in between the pillars. The etch time and the gas parameters are the same as those used for Set I. Fig. 4.1(b) shows the final resulting pattern for this set.

Set III (200 nm x 100 nm) Strategy:

The beam conditions from Set II are adjusted for the 200 nm x 100 nm pattern. The electron beam condition for Set III is adjusted from 60 μm Ap with 2 nA, to 60 μm Ap with 400 pA. This creates a well-developed PR on the edges of the sample, but is not distinguishable at the center. This is due to charging of the E-beam as the pattern is decreased, seen in Fig. 4.5. To help reduce the charging effects of the beam on the pattern, a checkerboard pattern is developed, with one square patterned area surrounded by squares that are not patterned (Fig. 4.6 (a)). This is a change from the pattern layout used for Set I and II, which is a square pattern (Fig. 4.6 (b)). The checkerboard pattern results in a well-developed pattern at the center. A few rows at the edge of the pattern fall over as a result of capillary effects during the develop and drying processes (Fig. 4.7).

A dosing test was conducted for this set since PR is observed between the pattern area for the dose of 350 $\mu C/cm^2$ seen in Fig 4.8. The dose values range between 80 $\mu C/cm^2$ to 150 $\mu C/cm^2$. The optimum dose value observed for the 100 nm x 200 nm pattern is 110 $\mu C/cm^2$. In

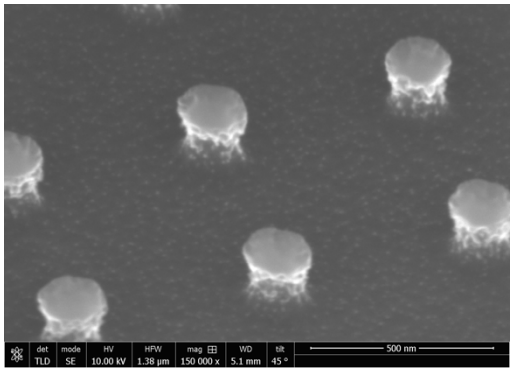
addition, etching the 100 nm x 200 nm pattern with SF_6, O_2 and Ar results in a severe undercut of the pillars (Fig. 4.9 (a)). As a result of the undercut, some of the pillars have fallen over and have affected the final pattern. The etch recipe is changed to CF_4 and Ar to prevent the pillars from falling over and yield a well-defined pattern (Fig. 4.9 (b)). The etch time is 8 minutes and 30 seconds, using these gases. The resulting pillars are close to the desired dimensions and the side walls of the pillars are smooth compared to the previous sets. Fig. 4.1 (c) shows the final resulting pattern for this set.

Set IV and V (100 nm x 50 nm) Strategy:

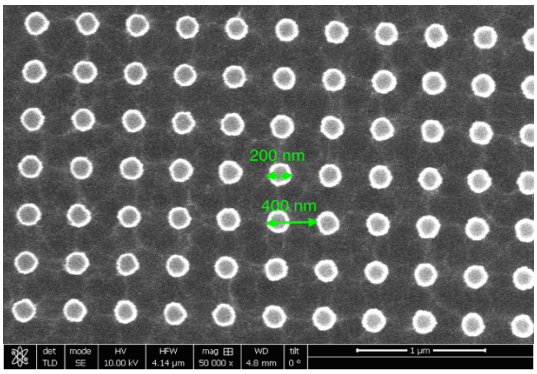
The beam conditions and the checkerboard layout used to develop the pattern for Set III is examined for the 100 nm x 50 nm pattern (Sets IV-V). The use of the same beam conditions results in an over exposure of the pattern and the PR is found in between the pillars. A reduction of the current is not possible due to the correlation of pattern time vs current. As the beam current is reduced, the pattern time increases exponentially. A mixture of propylene glycol monomethyl ether acetate (PGMEA) and NEB-31 is used to thin the PR at a ratio of 2:1. The thinner PR has a thickness of 120 nm after the PR is developed and the thinner PR results in almost all the PR pattern tilting over.

To help the PR stay up right after the developer step, the pre-bake and the post-bake times are varied from 1:30 minutes to 3:00 minutes in 15 second intervals. The pre-bake time has no effect on the pillar stability. A post-bake time of 2:30 minutes results in the PR adhering to the substrate and less pillars tilting over. The dose value for the 50 nm x 100 nm pattern is varied from 140 $\mu C/cm^2$ to 170 $\mu C/cm^2$ in 5 $\mu C/cm^2$ intervals. The best dose is found to be 145 $\mu C/cm^2$. The outer edges of each square pattern are still susceptible to pillars tilting over, but the center of the pattern is well-defined. The same etch process is used as in Set III, but an etch time of 4:30

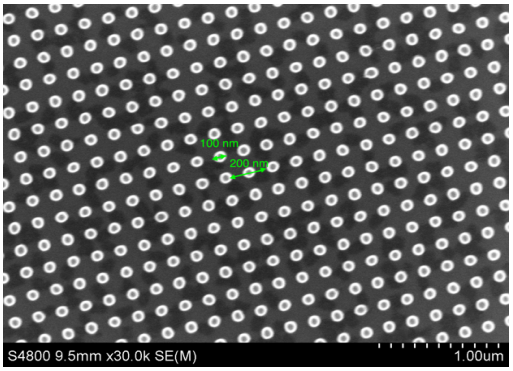
minutes is used, as a result of the thinner PR. The benefit of using CF_4 with Ar to etch the 50 nm x 100 nm pattern can clearly be seen in Fig. 4.10. Figure 4.1 (d) and Fig 4.1 (e) shows the final resulting patterns for Sets IV and V, respectively.



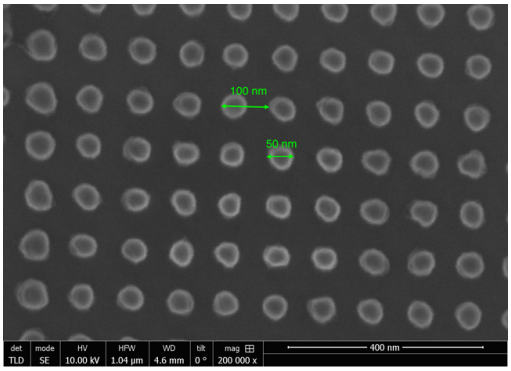
(a)



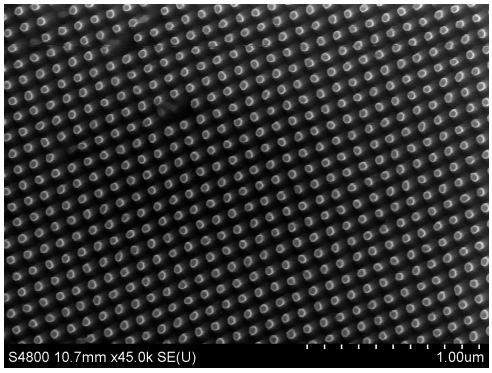
(b)



(c)



(d)



(e)

FIGURE 4.1: SEM IMAGES OF (A) 200 NM X 600 NM SI (211) PATTERN, (B) 200 NM X 400 NM SI (211) PATTERN, (C) 100 NM X 200 NM SI (211) PATTERN, (D) 50 NM X 100 NM SI (211) PATTERN, AND 50 NM X 100 NM SI (111) PATTERN

A study is conducted to determine the effect of O_2 on the pattern quality and the CdTe growth for both the 200 nm x 600 nm and the 200 nm x 400 nm patterns. It is discovered that using 50% of O_2 results in straight and rough sidewalls (Fig. 4.2), while reducing the percent oxygen to 30% O_2, results in smoother and rounder sidewalls (Fig. 4.3). This allows for a better understanding of how the pillar structure affects the growth. Comparing the growth of 50% O_2 to 30% O_2 for the 200 nm x 600 nm growth shows the growth is similar, but the grains are larger of the growth with 30% O_2. The growth for the 200 nm x 400 nm pattern with 30% O_2 results in better quality over the 50% O_2.

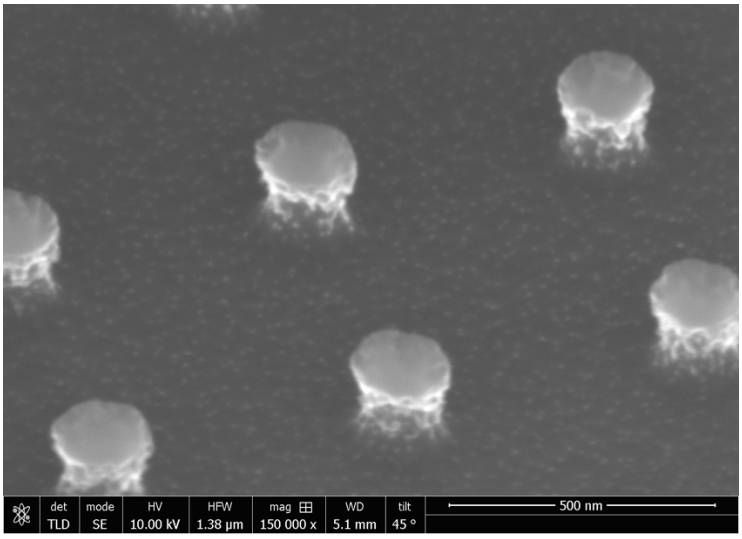


FIGURE 4.2: ROUGH SIDE WALLS AS A RESULT OF INITIAL ETCH PROCESS WITH SF_6, O_2, AND AR FOR SET I.

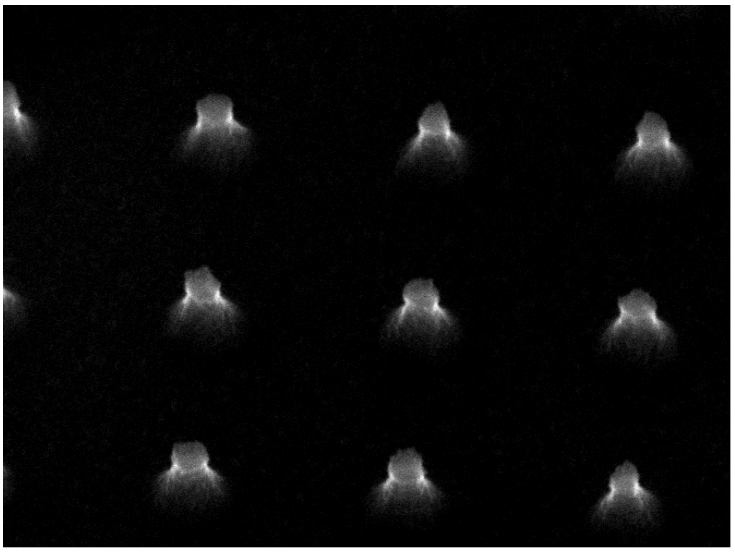


FIGURE 4.3: PILLARS ETCHED WITH 30%O_2 HAVE MORE ROUNDED SIDEWALLS AT THE BOTTOM.

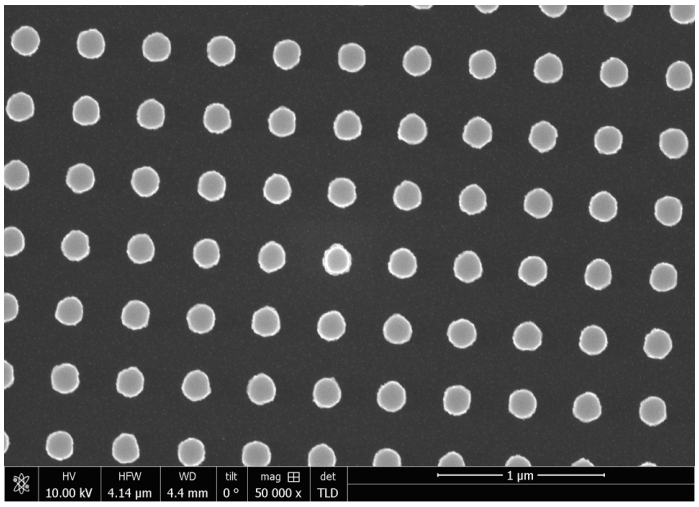


FIGURE 4.4: WELL- DEVELOPED PATTERN FOR THE 200 NM X 400 NM PATTERN AFTER A REDUCTION IN THE BEAM CURRENT TO 2 NA.

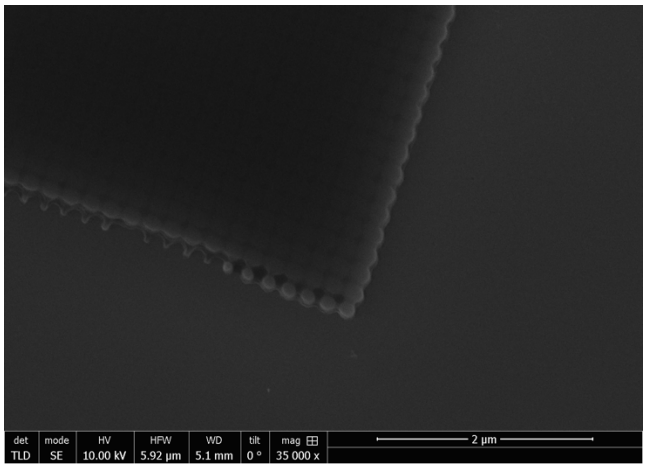
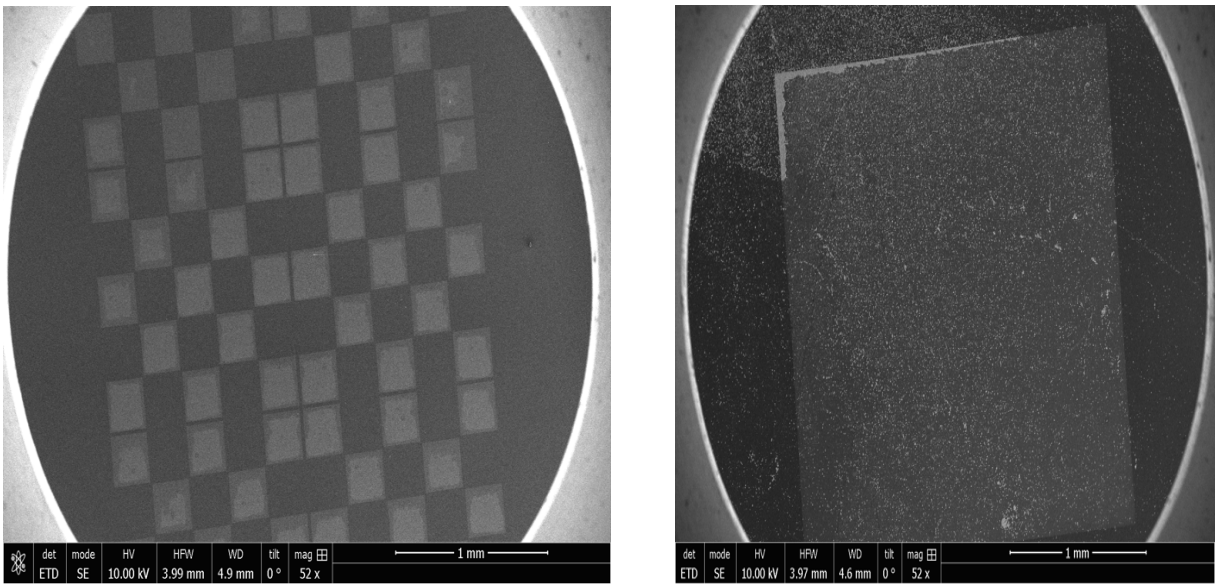


FIGURE 4.5: PATTERN OF 200 NM X 100 NM WITH SET II PARAMETERS ILLUSTRATING THE CHARGING EFFECT DUE TO SMALLER PILLAR SIZE.



(a) (b)

FIGURE 4.6: COMPARISON OF (A) THE NEW PATTERN TO HELP REDUCE CHARGING, TO (B) THE ORIGINAL PATTERN LAYOUT FOR SETS I AND II.

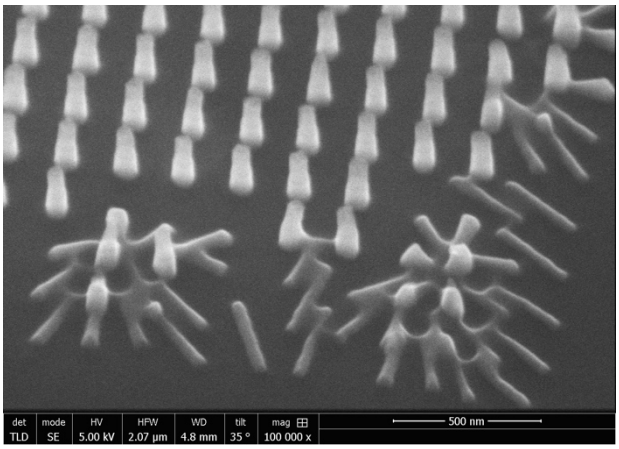


FIGURE 4.7: PILLARS DETACHED FROM SUBSTRATE DUE TO CAPILLARY FORCES DURING THE DEVELOP AND DRYING PROCESSES.

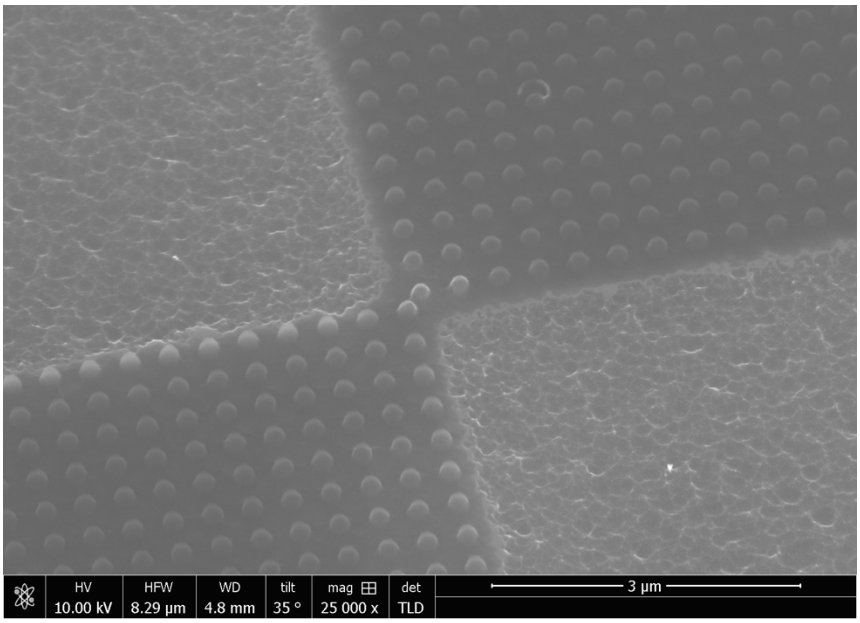
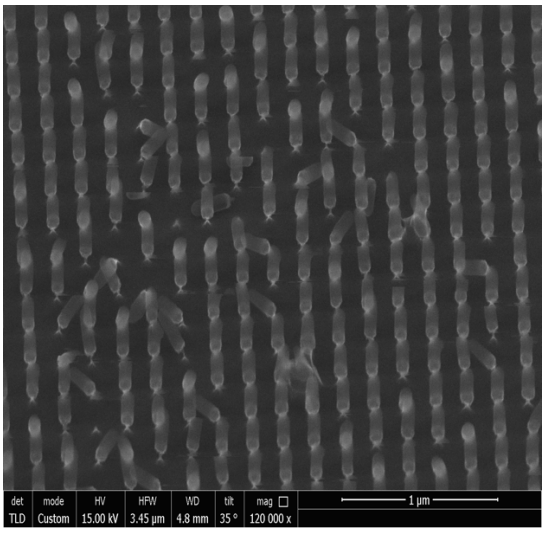
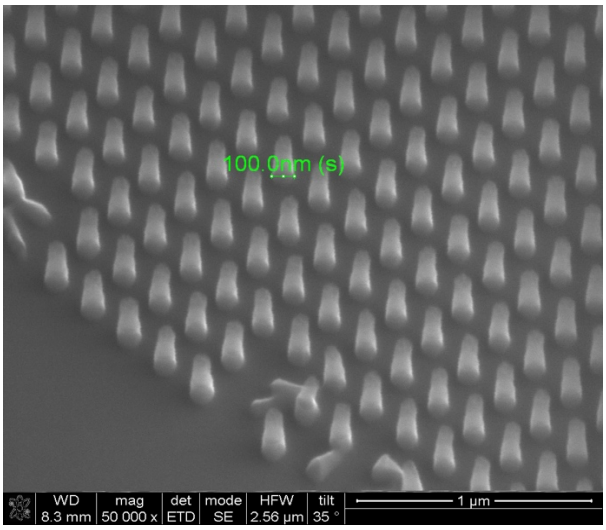


FIGURE 4.8: RE-DESIGNED PATTERN FOR SETS III-V. THERE IS PR IN BETWEEN PILLAR PATTERN.

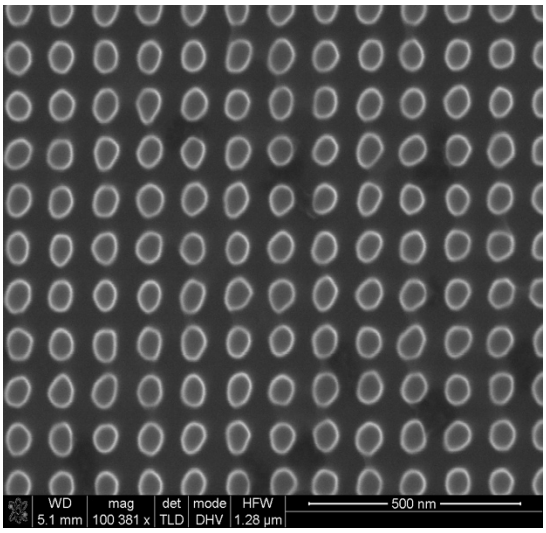


(a)

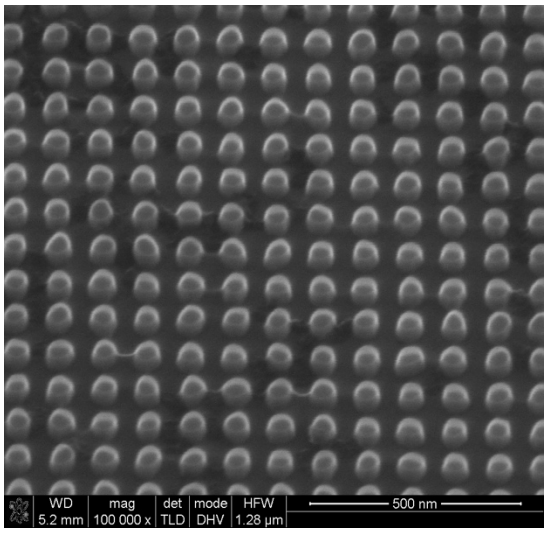


(b)

FIGURE 4.9: ETCHING OF THE 100 NM X 200 NM PATTERN WITH SF_6 RESULTED IN (A) SEVERE UNDER CUT WITH THE SI PILLARS FALLING OVER, COMPARED TO (B) USING AN CF_4 ETCH WHICH RESULTS IN A WELL-DEFINED PATTERN.



(a)



(b)

FIGURE 4.10: (A) SURFACE VIEW OF 50 X 100 NM SI PATTERN ETCHED BY CF_4 AND AR, AND (B) SURFACE TILTED 45˚.

4.2 Growth of CdTe Doped with Zn via CSS Method

CdTe doped with 5% and 10% Zn is grown on Si(211) and Si(111) substrates using the CSS method to promote selective growth on the samples. Si pillar diameters range from ~200 nm to ~50 nm after dry etching is complete. Procedures are identified to promote high quality growth of single crystal CdTe doped with Zn on the Si pillars. The CdTe growth occurs on top of or around the pillars, and results in selective growth for most of the samples.

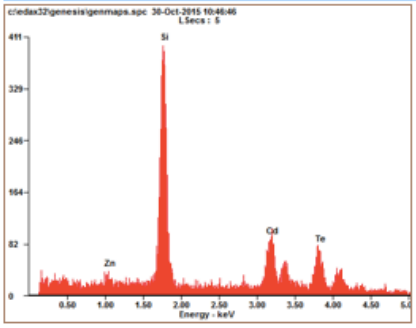
The CSS parameters that affect the growth in this study are the pressure, the deposition time, the source temperature, and the substrate temperature. It is also noted that the p/d ratio also influences the selective growth of CdTe, and the optimum ratio is identified by comparing the results of Set I (p/d=3) to those of Set II (p/d=2). This growth follows the diffusion-limited model based on a pressure of ~1.5 Torr [72]. The initial temperature parameters tested are based on the work done by Diaz et. al. [29, 61], where selective growth of CdTe on Si(211) and Si(111) substrates without a mask is reported. The CSS parameters developed by Diaz that resulted in the best growth are T_{sub}=450˚C, T_{sou}=550˚C, pressure of 0.25 Torr, and a deposition time of 5 minutes. The parameters are modified in this study in order to achieve high quality selective growth of CdTe doped with Zn on pillars as small as 50 nm.

4.2.1 EDX ANALYSIS

EDX is used to identify if there is Zn in the CdTe growth and to identify the percent of Zn in the growth. Fig. 4.11 shows the EDX analysis of the 400 nm x 200 nm pattern with 5% Zn source. The four elements that are present are Si, Cd, Zn, and Te atoms; no other elements are

detected in the scan. The red square covers one grain on the Si substrate and Si is the highest peak. The EDX analysis shows the concentration of Zn in the growth is 10% (Fig. 4.11). This value of Zn is much higher than the CdTe source, which contains 5% Zn.

Fig. 4.12 shows the EDX analysis for the 200 nm x 100 nm pattern with CdTe doped with 10% Zn. The Si substrate results in the highest peak in the EDX analysis. The EDX analysis shows the concentration of Zn in the CdTe growth is 22%. This value of Zn is again much higher than the CdTe source, which contains 10% Zn. Both EDX studies indicate that the percent Zn is approximately double the expected value. This can be attributed to Zn–Te bond being more stable than the Cd–Te bond [67], which can produce a higher concentration of Zn in the sample.



Element	Wt%	At%
ZnL	03.32	02.97
SiK	31.42	65.32
CdL	30.12	15.64
TeL	35.13	16.07
Matrix	Correction	ZAF

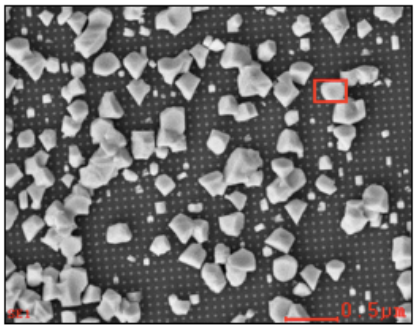


FIGURE 4.11: EDX ANALYSIS FOR SET II (400 NM X 200 NM PATTERN) – CDTE GROWTH WITH 5% ZN

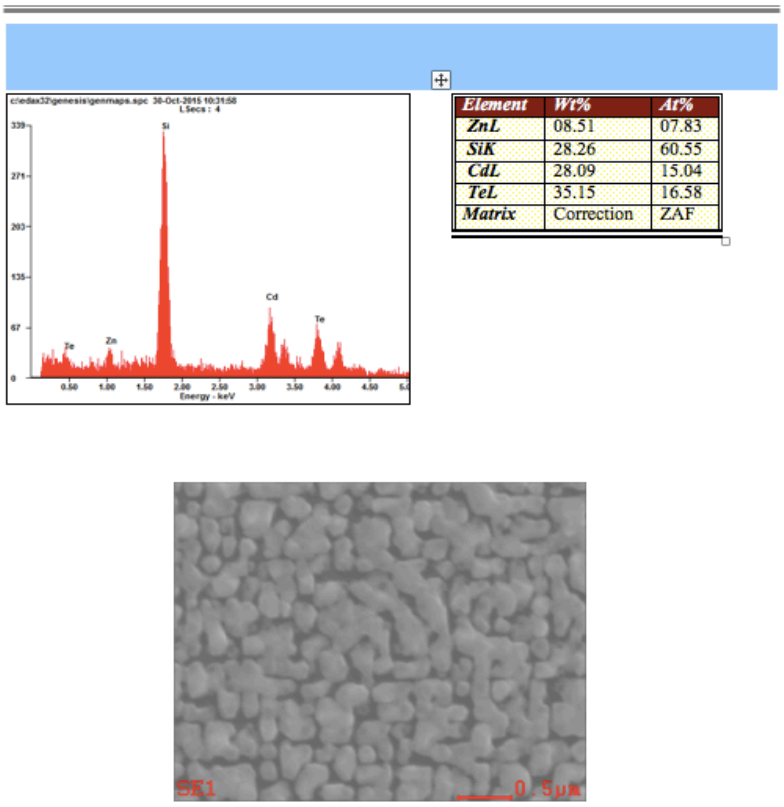


FIGURE 4.12: EDX ANALYSIS FOR SET III (200 NM X 100 NM PATTERN) – CDTE GROWTH WITH 10% ZN.

4.2.2 CDTE DOPED WITH 5% ZN GROWN ON SI(211) WITH 200 X 600 NM PATTERN (SET I)

The first set of experiments are preformed to find the ideal growth temperatures for CdTe doped with Zn growth on Si (211) substrates. Zn is believed to affect the preferred source and substrate temperatures. A pillar diameter of 200 nm and a pitch of 600 nm is used for Set I. The source is annealed before each experiment to ensure a clean surface of the source for sublimation. For Set I experiments, the deposition time is varied from 3 minutes to 5 minutes, the pressure is approximately 1.5 Torr, the source temperature is varied from 550˚C to 585˚C, and

the substrate temperature is varied from 450˚C to 505˚C. The CdTe source that is used for Set I contains 5% Zn with twins. The effect of the percent O_2 in the RIE etch process on the CdTe growth is also examined in Set I. The samples and parameters for Set I are listed in Table 4.2.

TABLE 4.2 SUMMARY OF GROWTH PARAMETERS FOR SET I

Fabrication Parameters	Sample name	Tsor (˚C)	Tsub (˚C)	Reactor Pressure (Torr)	Substrate	Pitch/Diameter (nm)	Zinc Doping (%)	Deposition time (min)	Average Grain Size (μm)
Optimization of Deposition Temperatures	S1_1	550	450	1.5	Si (211)	600/200	5	5	0.372
	S1_2	575	460	1.5	Si (211)	600/200	5	5	1.051
	S1_3	575	475	1.5	Si (211)	600/200	5	3	1.683
	S1_4	575	465	1.5	Si (211)	600/200	5	3	0.452
	S1_5	575	455	1.5	Si (211)	600/200	5	3	1.188
	S1_6	575	485	1.5	Si (211)	600/200	5	3	0.638
	S1_7	585	505	1.5	Si (211)	600/200	5	3	1.078
	S1_8	585	485	1.5	Si (211)	600/200	5	3	1.493
	S1_9	585	495	1.5	Si (211)	600/200	5	3	1.384
	S1_10	575	485	1.5	Si (211)	600/200	5	3	1.115

SEM micrographs of the samples listed in Table 4.2, are included in Figs. 4.13 through 4.22. Samples S1_1 through S1_9 are etched with 50% O_2 and sample S1_10 is etched with 30% O_2.

The temperature profile used for the S1_1 sample, is based on parameters used by Diaz [29]. With the presence of Zn, the growth appears needle-like and some pillars have sets of three needle-like grains (Fig. 4.13). Based on these results, the source temperature is increased for the remainder of the experiments in this set. The remainder of the samples are associated with source temperatures of 575˚C and 585˚C.

The source temperature is increased from 550˚C to 575˚C for sample S1_2, with a substrate temperature of 460˚C. The growth quality is improved (Fig. 4.14) compared to sample

S1_1 (Fig. 4.13), but is not characterized as high quality growth. Rod like grains that are misoriented in different directions and pyramid shaped grains are observed. Based on the growth for the first two samples, the next four samples in Set I focus on a source temperature of 575˚C. The deposition time for Sample S1_2 is five minutes, and due to the large amount of growth, the time is reduced to three minutes for the rest of the experiments in Set I.

The substrate temperature is increased to 475˚C for sample S1_3, since the deposition time is lowered to 3 minutes. This results in the largest grains within this set (Figs. 4.15). A high source temperature and a ΔT of 100˚C is a factor for this type of growth. The grains appear to be polycrystalline and there is less growth compared to the S1_2 sample.

Due to the low number of grains in sample S1_3, the substrate temperature is reduced from 475˚C to 455˚C, in order to increase the number of nucleation sites for sample S1_4 (Fig. 4.16). In sample S1_4, the grains appear rod like and are oriented in different directions. Some grains have three to four nucleation sites extending from the same pillars.

The substrate temperature is reduced further for Sample S1_5, from 465˚C to 455˚C, to try to increase the number of nucleation sites. This results in an increase in growth and the grains cover most of the substrate surface (Fig. 4.17). These grains have flat rough surfaces that are misoriented with respect to the substrate surface.

The substrate temperature was increased from 455˚C to 485˚C for sample S1_6. The source and substrate temperature of 575˚C and 485˚C, respectively for this sample, result in the highest quality growth for this set (Fig. 4.18). The grains have flat smooth surfaces, although some surfaces are misoriented with respect to the substrate surface, and the growth is non-uniform throughout the sample.

Both the source and substrate temperature are increased for sample S1_7, from 575 and 485, respectively, to 585˚C and 505˚C, respectively. The grains cover the entire surface and most of the CdTe grains have a triangular shape and are merging with each other (Fig. 4.19). There are a few large CdTe grains that have smooth flat surfaces, but the growth is considered uncontrolled.

For this reason, the substrate temperature is lowered from 505˚C to 485˚C for sample S1_8. This sample has the second largest grains in Set I (Fig. 4.20). A few CdTe grains appear to be crystalline, while all the large grains appear to be polycrystalline.

The substrate temperature was increased slightly from 485˚C to 495˚C for sample S1_9. The increase in the substrate temperature resulted in the entire substrate being covered by CdTe grains. These grains appear polycrystalline and some grains have a pyramid shape (Fig. 4.21).

Samples S1_6 and S1_10 have the same source and substrate temperatures. However, sample S1_6 is etched with 50% O_2 (Fig. 4.18), while sample S1_10 is etched with 30% O_2 (Fig. 4.22). The 50% O2 etch resulted in straighter, but rougher Si pillar sidewalls for the substrate in sample S1_6. The 30% O2 etch resulted in curved and smooth Si pillar sidewalls for sample S1_10. The grains for sample S1_10 are double the size of the grains in sample S1_6. The grain size could be a result of the smoother sidewalls allowing the CdTe atoms to move more easily on the substrate surface.

The source temperature of 575˚C and substrate temperature of 485˚C was identified as the sample with the most uniform, high quality growth for Set I. Thus, sample S1_6 was selected for TEM analysis. High quality growth is defined as crystalline grains with smooth surfaces that are parallel to the substrate and pillar surface. X-ray Diffraction (XRD) and Atomic Force Microscopy (AFM) are used to characterize sample S1_6. The source temperature of

575˚C and substrate temperature of 485˚C are applied to Set II, since sample S1_6 resulted in the best growth for Set I.

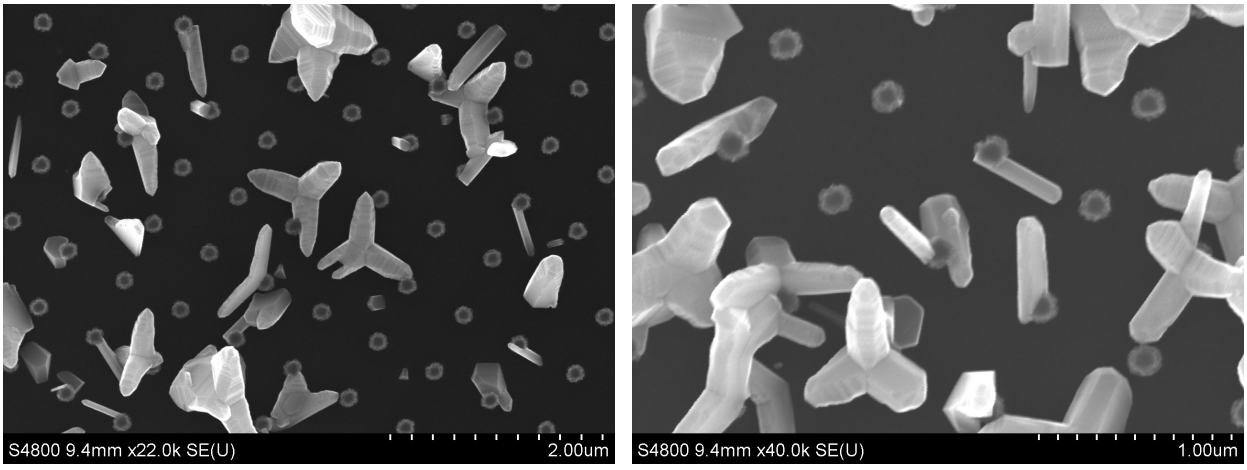


FIGURE 4.13: SAMPLE S1_1, SI (211), 200 NM X 600 NM PATTERN, 5% ZN DOPING, T_{SOURCE}= 550˚C, $T_{SUBSTRATE}$= 450˚C AND 50% O_2.

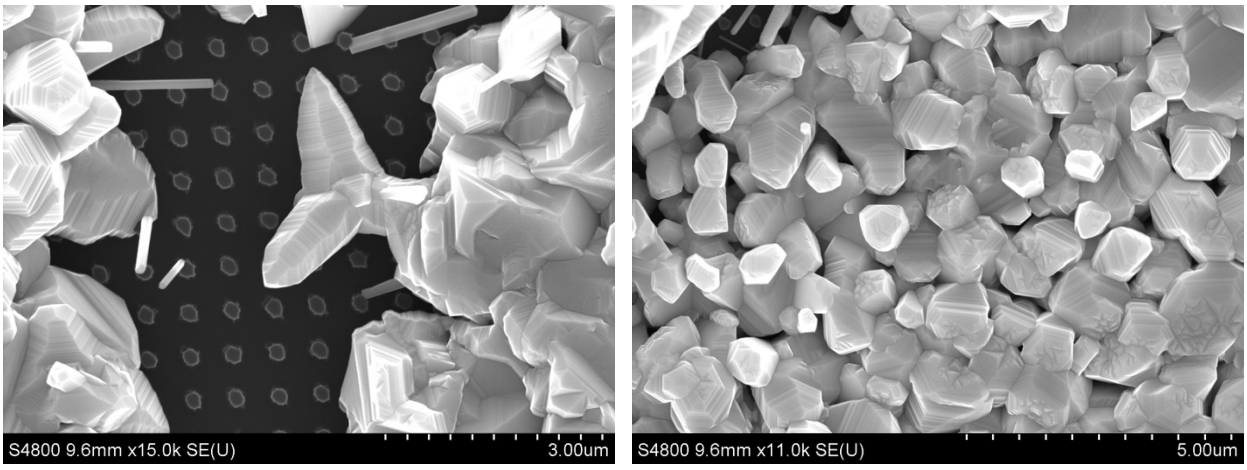


FIGURE 4.14: SAMPLE S1_2, SI (211), 200 NM X 600 NM PATTERN, 5% ZN DOPING, T_{SOURCE}= 575˚C, $T_{SUBSTRATE}$= 460˚C, AND AND 50% O_2.

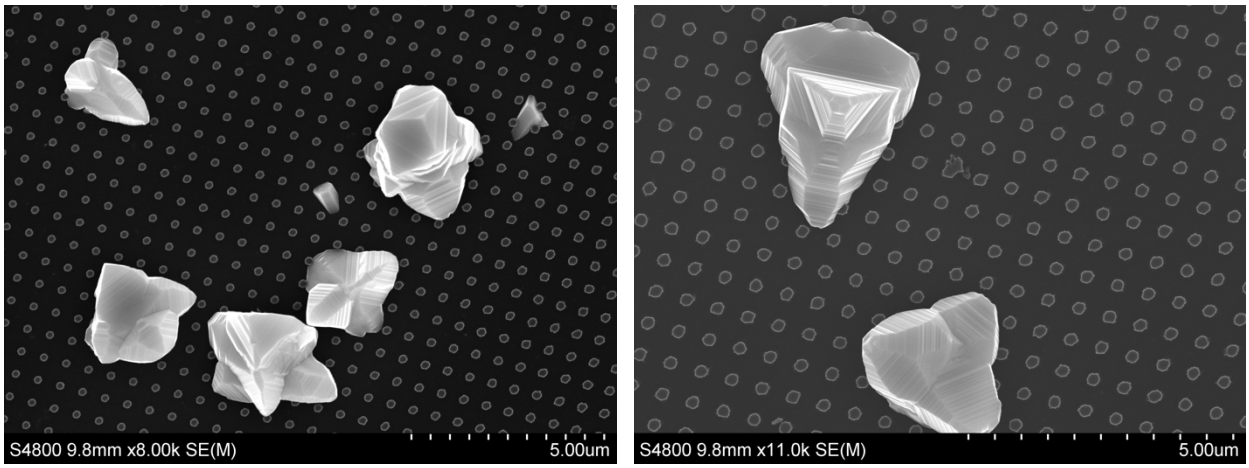


FIGURE 4.15: SAMPLE S1_3, SI (211), 200 NM X600 NM PATTERN, 5% ZN DOPING, T_{SOURCE}= 575˚C, $T_{SUBSTRATE}$= 475˚C, AND 50% O_2.

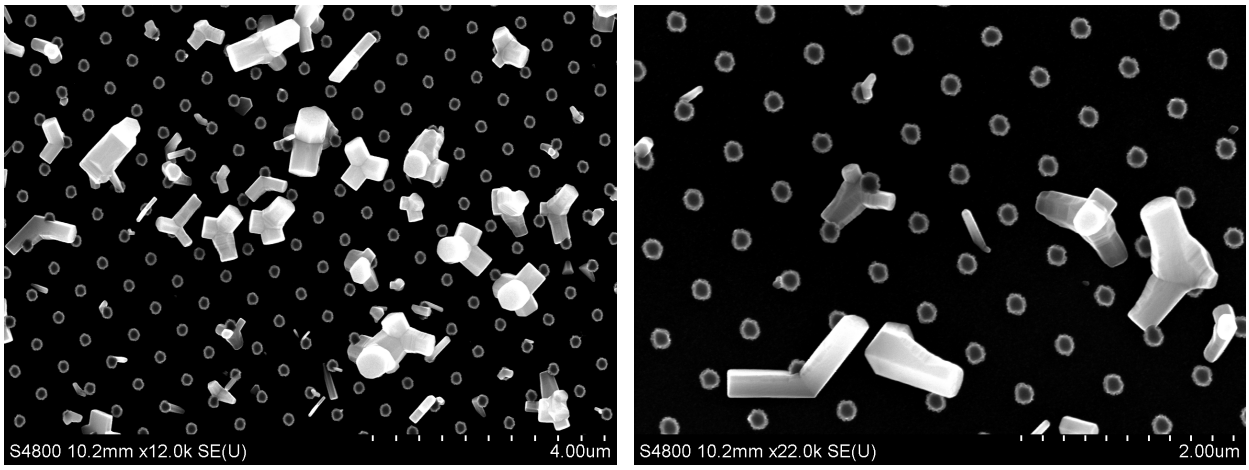


FIGURE 4.16: SAMPLE S1_4, SI (211), 200 NM X 600 NM PATTERN, 5% ZN DOPING, T_{SOURCE}= 575˚C, $T_{SUBSTRATE}$= 465˚C, AND 50% O_2.

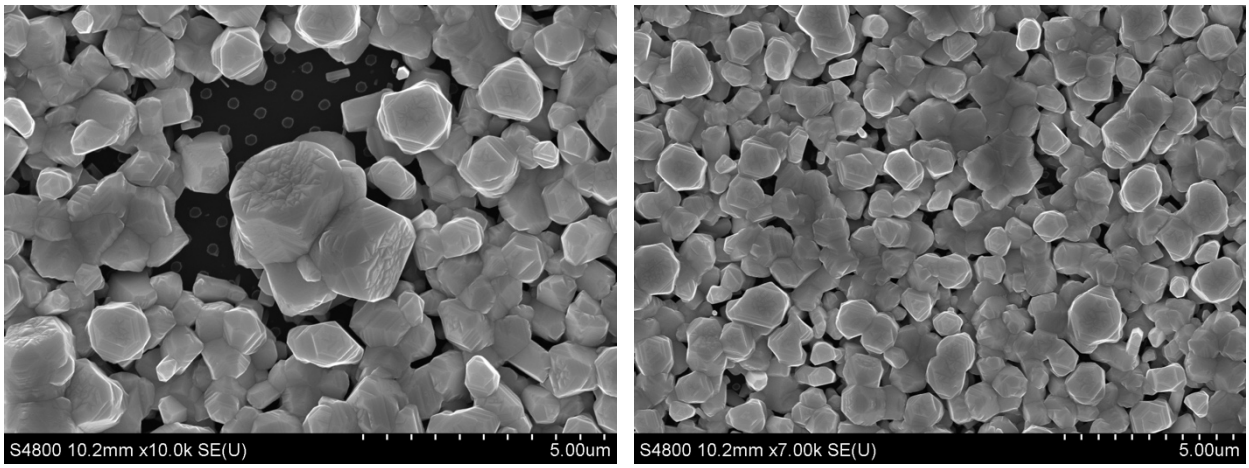


FIGURE 4.17: SAMPLE S1_5, SI (211), 200 NM X 600 NM PATTERN, 5% ZN DOPING, T_{SOURCE}= 575˚C, $T_{SUBSTRATE}$= 455˚C, AND 50% O_2.

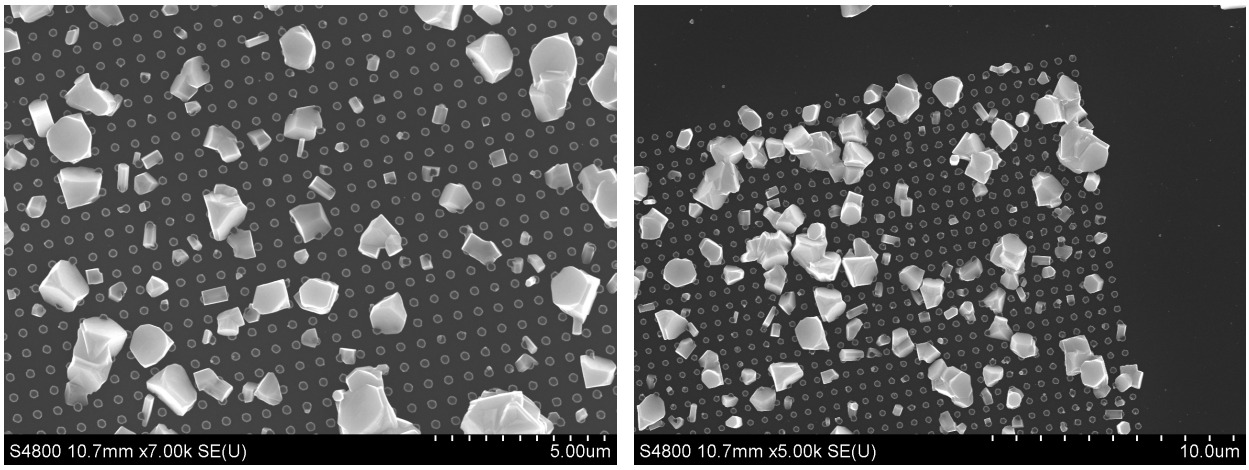


FIGURE 4.18: SAMPLE S1_6, SI (211), 200 NM X 600 NM PATTERN, 5% ZN DOPING, T_{SOURCE}= 575˚C, $T_{SUBSTRATE}$= 485˚C, AND 50% O_2.

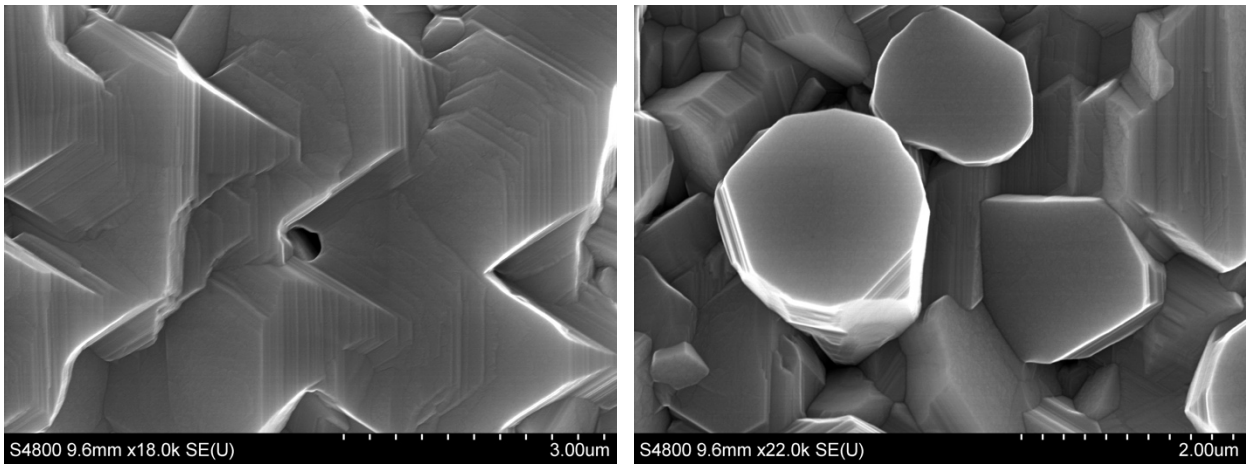


FIGURE 4.19: SAMPLE S1_7, SI (211), 200 NM X 600 NM PATTERN, 5% ZN DOPING, T_{SOURCE}= 585˚C, $T_{SUBSTRATE}$= 505˚C, AND 50% O_2.

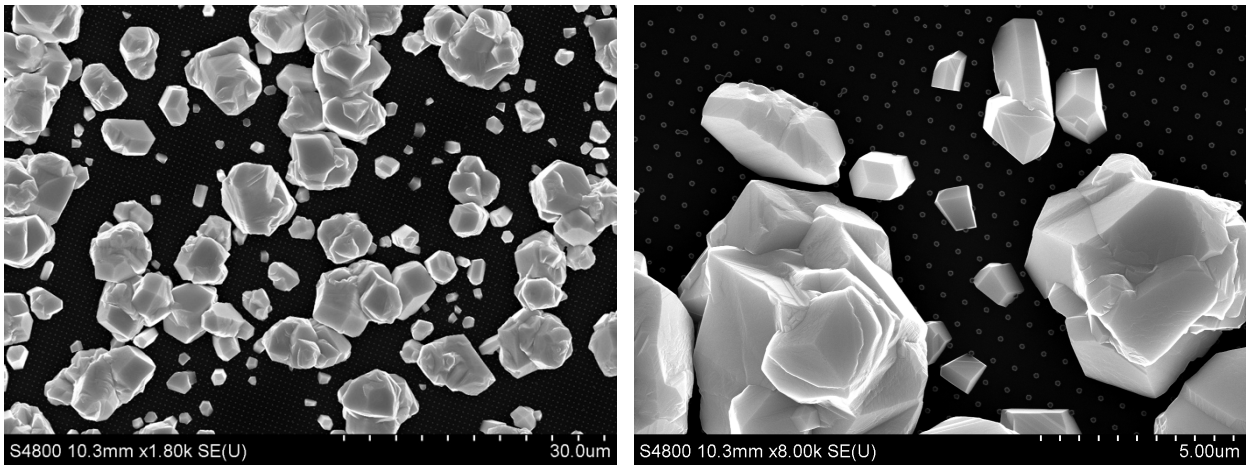


FIGURE 4.20: SAMPLE S1_8, SI (211), 200 NM X 600 NM PATTERN, 5% ZN DOPING, T_{SOURCE}= 585˚C, $T_{SUBSTRATE}$= 485˚C, AND 50% O_2.

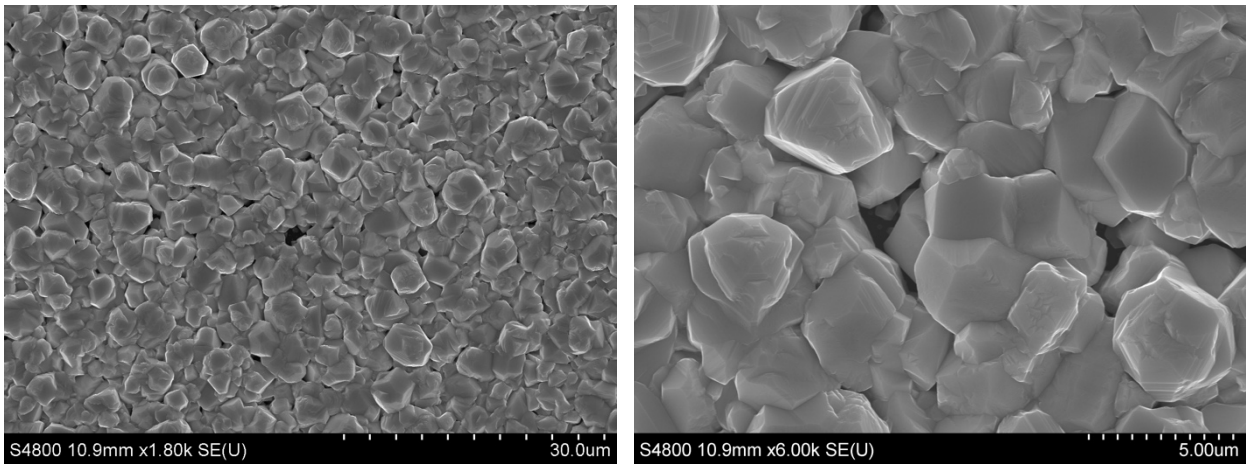


FIGURE 4.21: SAMPLE S1_9, SI (211), 200 NM X 600 NM PATTERN, 5% ZN DOPING, T_{SOURCE}= 585˚C AND $T_{SUBSTRATE}$= 495˚C, AND 50% O_2.

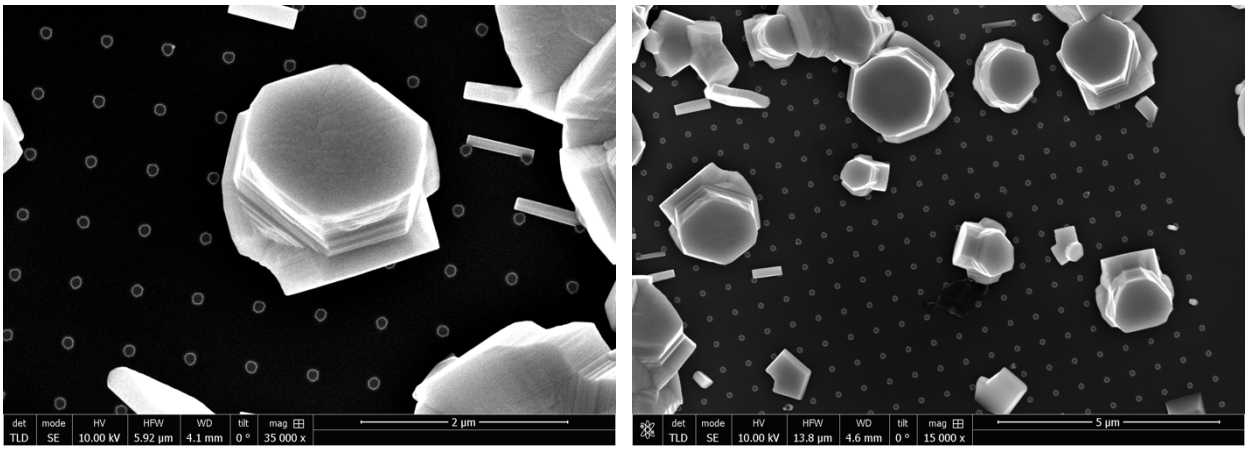


FIGURE 4.22: SAMPLE S1_10, SI (211), 200 NM X 600 NM PATTERN, 5% ZN DOPING, T_{SOURCE}= 575˚C, $T_{SUBSTRATE}$= 485˚C, AND 30% O_2.

XRD analysis of sample S1_6 resulted in two dominant peaks, (111) and (220) (Fig. 4.23). Table 4.3 shows the calculated d spacing, full width at half max (FWHM), and the crystal grain size for the XRD analysis obtained from the EVA software. The XRD data shows that the (111) and (220) peak theoretical data for CdTe doped with 5% Zn matches closely to the

measured data shown in Table 4.3. There is a leftward shift of all the measured peaks relative to the theoretical values, which is indicative of a uniform strain on the film [94]. The XRD data shows that there are several sub-grains growing in other orientations.

The AFM was used to analyze the surface and cross-section of the grains for sample S1_6. The 2D and the 3D image of a grain with a smooth surface are seen in Fig. 4.24 (a-b). Contact mode was used to obtain the best image of the grains. The use of contact mode resulted in damage to the grain's surface, as seen in the center grain. The AFM tip makes contact and damages the surface of the grain. The cross section of the grain in Fig. 4.24 (a) is shown in Fig. 4.24 (c). The average surface roughness (R_a) of the grain is 49 nm and the value is higher than the surface roughness of 1.698 nm [95].

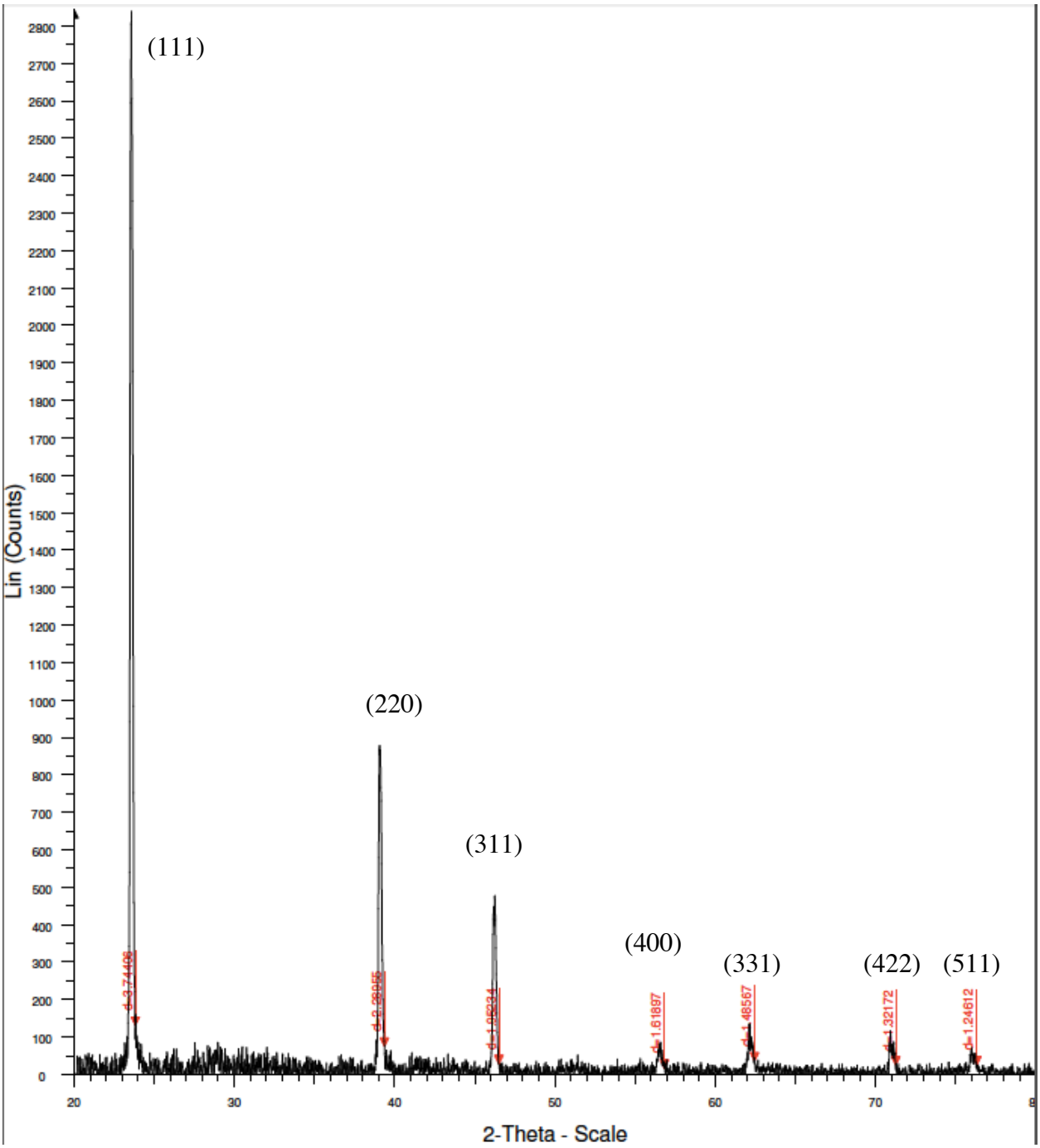
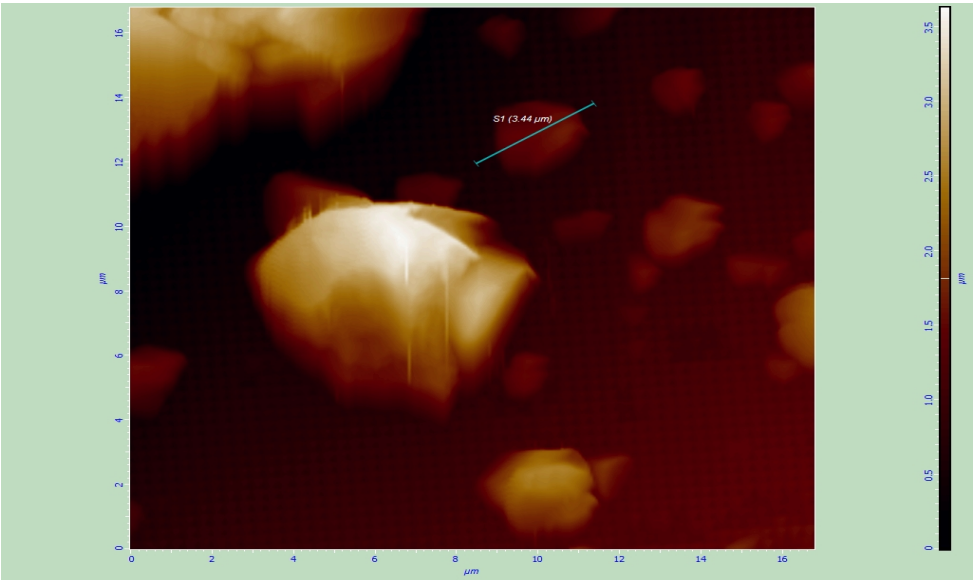


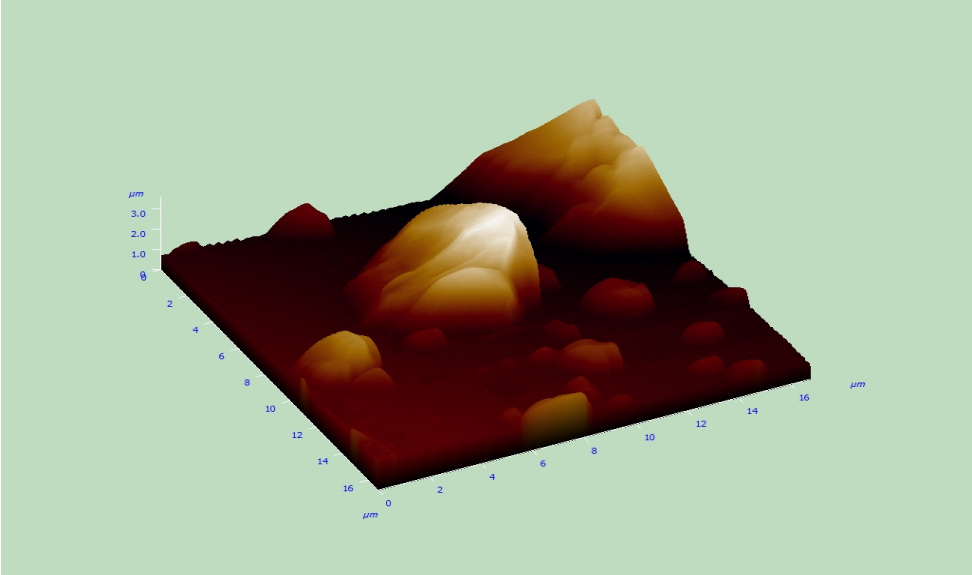
FIGURE 4.23: XRD ANALYSIS OF SAMPLE S1_6.

TABLE 4.3: THE XRD FOR SET I (600 NM X 200 NM)-CDTE GROWTH WITH 5% ZN.

Crystal Orientation	Theoretical d (Å)	Measured d (Å)	FWHM (˚)	Crystal Grain Size (nm) Measured	Measured 2θ anlge
(111)	3.74406	3.78189	0.12	67.6	23.440
(220)	2.28955	2.3067	0.0859	94.78	39.016



(a)



(b)

(c)

FIGURE 4.24: AFM ANALYSIS OF SAMPLE S1_6. (A) 2D IMAGE, (B) 3D IMAGE, AND (C) GRAIN CROSS SECTION.

4.2.3 CdTe Doped with 5% Zn Grown on Si(211) with 200 x 400 nm Pattern (Set II)

The second set of experiments is focused on growing CdTe doped with 5% Zn on 200 nm Si(211) pillars with a pitch of 400 nm. The CdTe growth on a patterned substrate with a p/d ratio to two will be compared with the growth from Set I, where the p/d ratio is three. For Set II the source temperature is 575˚C with a substrate temperature of 485˚C for all experiments in this set. The deposition time is varied from 3 minutes to 7 minutes with the pressure set at approximately 1.5 Torr. The CdTe source contains 5% Zn with twins. The O_2 in the RIE etch process is 50 % O_2 for sample S2_1 and for sample, S2_2 and S2_3, RIE etch process is 30% O_2. The growth parameters for Set II are shown in Table 4.4, and SEM micrographs of the samples are included in Figs. 4.25 through 4.27.

Table 4.4: Summary of growth Parameters for Set II

Fabrication Parameters	Sample name	Tsor (˚C)	Tsub (˚C)	Reactor Pressure (Torr)	Substrate	Pitch/Diameter (nm)	Zinc Doping (%)	Deposition time (min)	Average Grain Size (µm)
Optimization of Deposition Temperatures	S2_1	575	485	1.5	Si (211)	600/200	5	3	0.904
	S2_2	575	485	1.5	Si (211)	600/200	5	3	0.789
	S2_3	575	485	1.5	Si (211)	600/200	5	5	1.817

The CdTe growth on sample S2_1(etched with 50% O_2) with a deposition time of three minutes is shown in Fig. 4.25. The CdTe grains have smooth surfaces, but appear to be misoriented with respect to the surface of the substrate. The larger CdTe grains appear to be

polycrystalline. Sample S2_2 (etched with 30% O_2) with a deposition time of three minutes is shown in Fig. 4.26. These growth conditions resulted in considerable improvement in CdTe growth over S2_1, with uniform growth and crystalline grains with smooth flat surfaces. Sample S2_3 (30% O_2 etch) is shown in Fig. 4.27. The deposition time was increased from 3 to 5 minutes in order to try to improve the uniformed growth from sample S2_2. The deposition rate increased, along with the average grain size. The grains for sample S2_3 include small triangular sub-grains.

Comparing the growth of the RIE etch with varying O_2 of Set I to Set II, there is a noticeable difference. In Set I, there is a very minimal difference between the use of 30% and 50% O_2 on the growth quality. But, in Set II, the O_2 plays a more noticeable role in the growth process, between S2_1 and S2_2. S2_2 has more growth and appears to be higher quality compared to S2_1.

Comparing the pitch/diameter ratio of Set I to Set II, sample S1_6 (Fig. 4.16), has similar growth to sample S2_2 (Fig. 4.26). Sample S2_2 has more high quality grains with smooth flat surfaces, and a more uniformed growth compared to sample S1_6 from Set I. Based on the results from Sets I and II, it was decided to maintain a pitch/diameter ratio of 2 for the remaining sets (Sets III - V).

Selective growth was observed for all the samples in Set II. Since sample S2_2 contained the highest quality growth, it was selected for XRD, AFM, and TEM analysis.

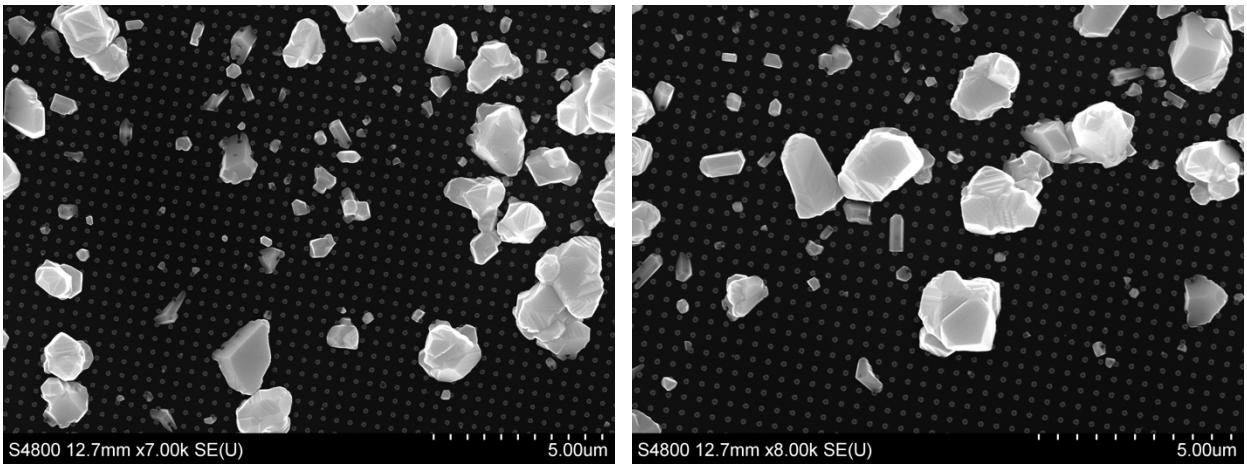


FIGURE 4.25: SAMPLE S2_1, SI (211), 200 NM X 400 NM PATTERN, O_2% =50%, TIME=3MIN, 5% ZN DOPING, T_{SOURCE}= 575˚C AND $T_{SUBSTRATE}$= 485˚C.

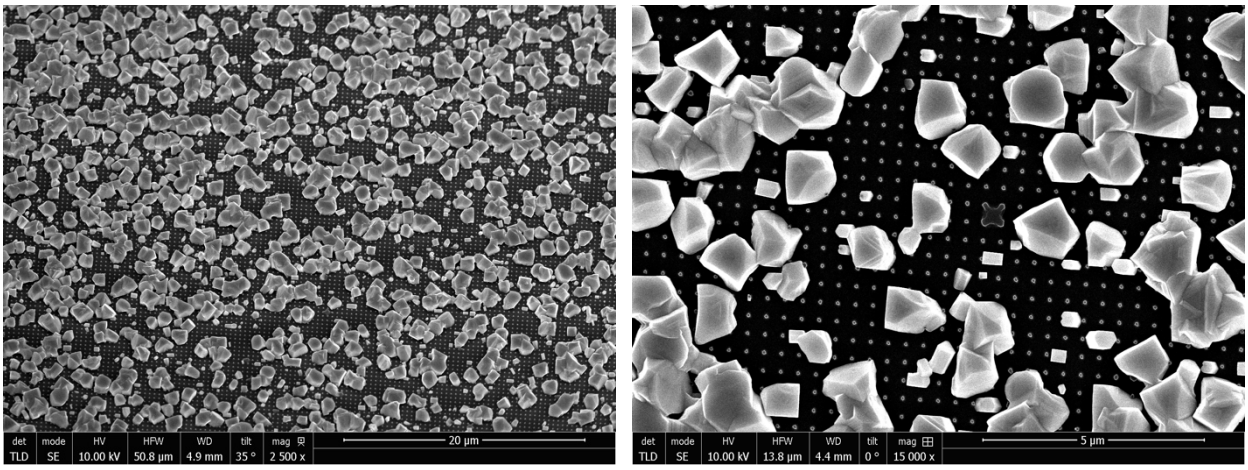


FIGURE 4.26: SAMPLE S2_2, SI (211), 200 NM X 400 NM PATTERN, O_2% =30%, TIME=3MIN, 5% ZN DOPING, T_{SOURCE}= 575˚C AND $T_{SUBSTRATE}$= 485˚C.

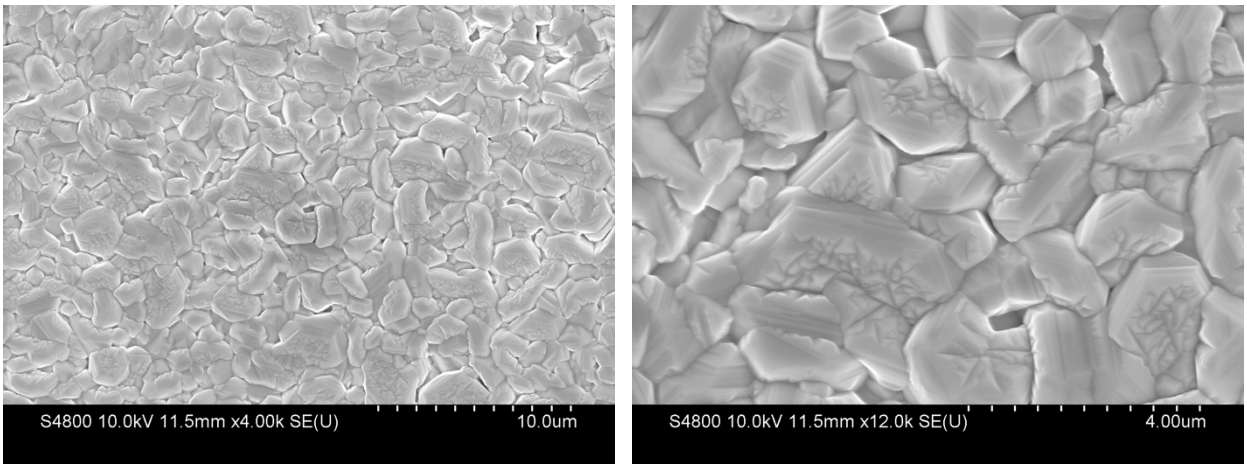


FIGURE 4.27: SAMPLE S2_3, SI (211), 200 NM X 400 NM PATTERN, O_2% =30%, TIME=5MIN, 5% ZN DOPING, T_{SOURCE}= 575˚C AND $T_{SUBSTRATE}$= 485˚C.

Sample S1_6 from Set I (Fig. 4.18) is compared to sample S2_2 from Set II (Fig. 4.26) through XRD analysis. XRD analysis shows the dominant peaks for Sample S2_2 (400 nm x 200 nm pattern) are associated with the CdTe(422) and CdTe(111) orientations (Fig. 4.28). The CdTe(422) orientation is parallel to the CdTe(211) orientation. Table 4.5 shows the theoretical and measured d spacing, FWHM, and the crystal grain size for sample S2_2. The XRD data shows that the peaks closely match theoretical data for CdTe with 5% Zn obtained from the EVA software, and the values for the S2_2 sample (400 nm x 200 nm pattern) are closer to the values provided by the XRD data sheet for CdTe with 5% Zn, compared to the S1_6 sample (600 nm x 200 nm pattern). Consequently, the data shows that a p/d ratio of two results in higher quality growth compared to a p/d ratio of three based on XRD. The CdTe(422) peak for sample S2_2 has a higher intensity. The FWHM of the CdTe(111) peak for sample S2_2 is smaller than that of sample S1_6, and the FWHM of the CdTe(422) orientation for sample S2_2 is larger than the FWHM of the CdTe(111) peak.

The AFM is used to analyze the surface of grains from sample S2_2 (Fig. 4.29). The AFM characterizes one of the CdTe grains in 2D (Fig. 4.29 (a)), 3D (Fig. 4.29 (b)), and shows the cross section of the CdTe grain (Fig. 4.29 (c)). Contact mode is again used to obtain the best images of the grains. Fig. 4.29 (c) shows the cross section of a single grain from the image in Fig. 4.29 (a and b). The 3D image includes a grain with a flat surface, where the surface of the grain is misoriented with respect to the surface of the substrate. The average surface roughness (R_a) is 34 nm. The surface is smoother than S1_6, but is still higher than the surface roughness of 1.698 nm [95].

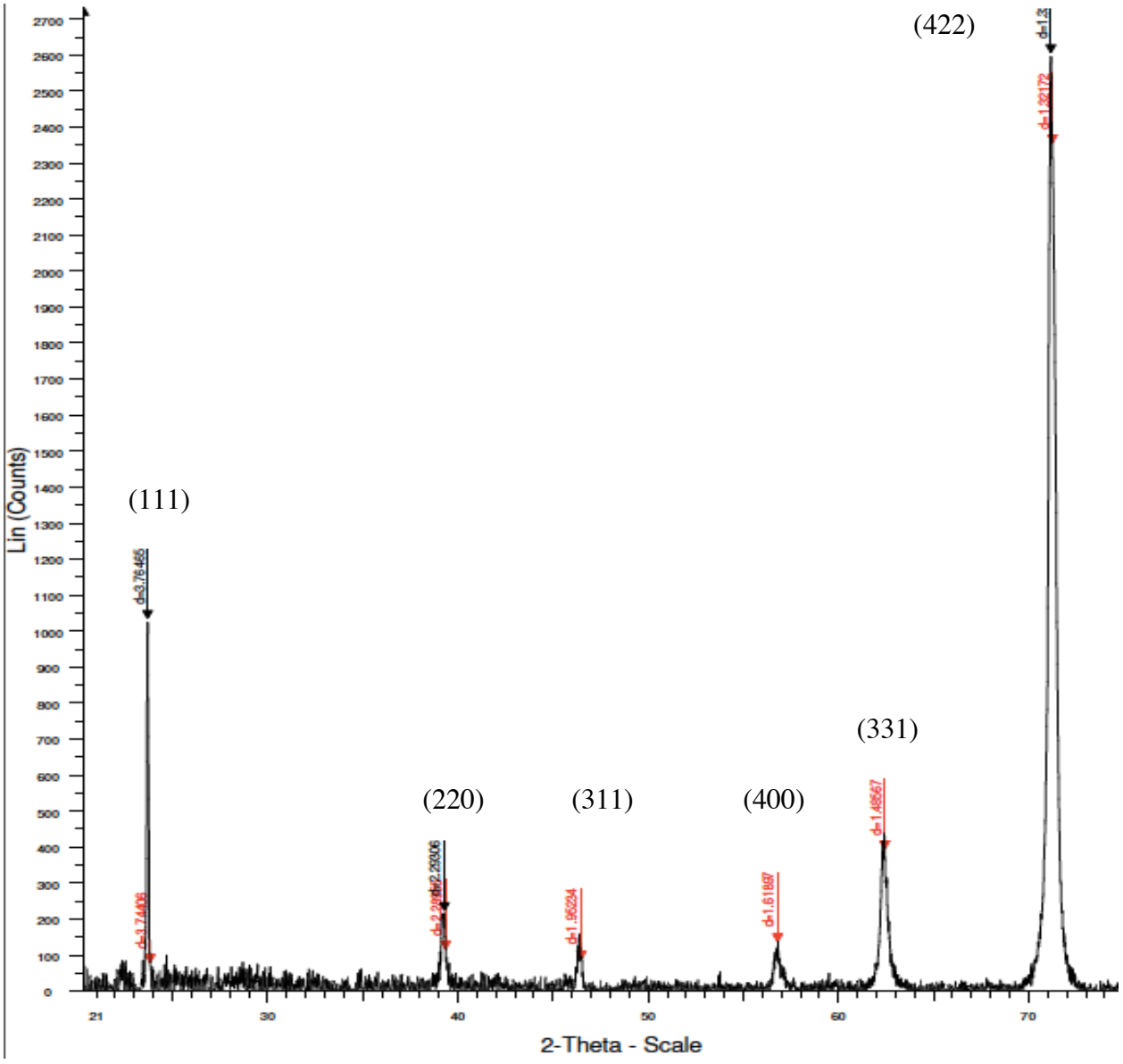
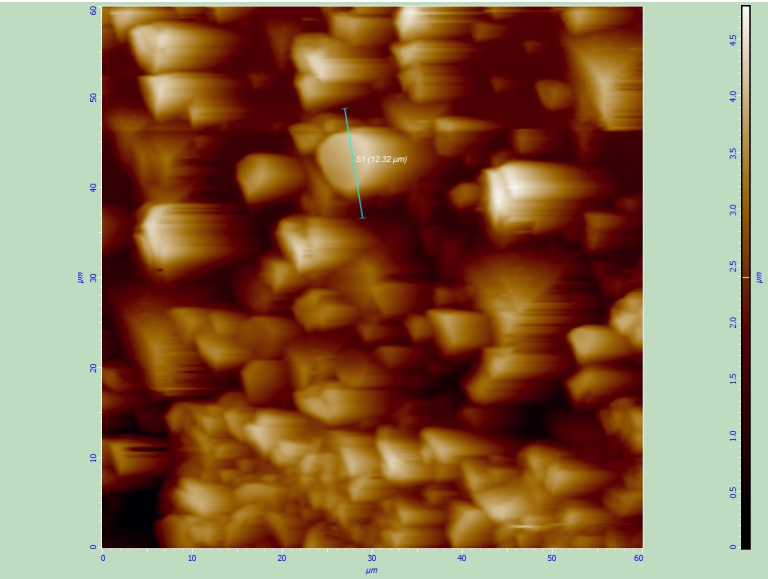


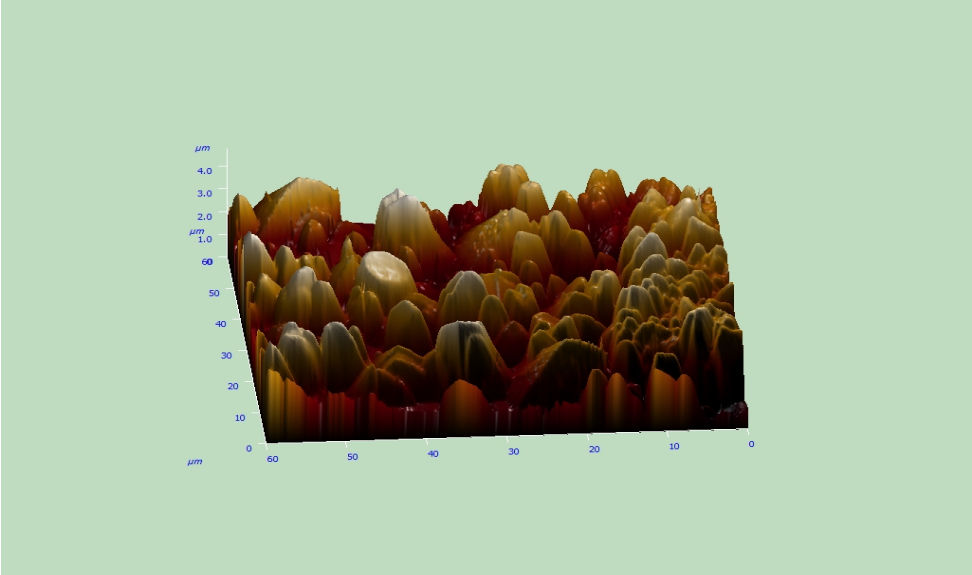
FIGURE 4.28: XRD ANALYSIS OF CDTE PEAKS IN SAMPLE S2_2.

TABLE 4.5: XRD FOR SET II (400 NM X 200 NM)-CDTE GROWTH WITH 5% ZN.

Crystal Orientation	Theoretical d (Å)	Measured d (Å)	FWHM (˚)	Crystal Grain Size (nm) Measured	Measured 2θ anlge
(111)	3.74406	3.76461	0.0626	129.95	23.412
(422)	1.32177	1.3230	0.421	NA	70.986



(a)



(b)

(c)

FIGURE 4.29: AFM ANALYSIS OF SAMPLE S2_2. (A) 2D IMAGE, (B) 3D IMAGE, AND (C) GRAIN CROSS SECTION.

4.2.4 CdTe Doped with 5% and 10% Zn Grown on Si(211) with 100 x 200 nm Pattern (Set III)

The third set of experiments (Set III) are performed to find the ideal growth temperature for CdTe doped with 5% and 10% Zn growth on Si (211) substrates. A pillar diameter of 100 nm, a pitch of 200 nm and a p/d ratio of two is used for Set III. A CdTe source with 5% Zn is annealed before each experiment to ensure a clean surface of the source for sublimation. For Set III experiments, the deposition time is varied from 1:30 minutes to 3 minutes, the pressure is approximately 1.5 Torr, the source temperature is varied from 565˚C to 595˚C, and the substrate temperature is varied from 445˚C to 485˚C. For Set III experiments with a CdTe source doped with 10% Zn, the deposition time is varied from 2 minutes to 8:30 minutes, the pressure is approximately 1.5 Torr, the source temperature is varied from 600˚C to 570˚C, and the substrate temperature is varied from 470˚C to 485˚C. The RIE etch process is changed to CF_4 and Ar for Set III due to the undercut caused by SF_6. The growth parameters for Set III are shown in Table 4.6, and SEM micrographs of the samples are included in Figs. 4.30 through 4.46.

TABLE 4.6: SUMMARY OF GROWTH PARAMETERS FOR SET III

Fabrication Parameters	Sample name	Tsor (˚C)	Tsub (˚C)	Reactor Pressure (Torr)	Substrate	Pitch/Diameter (nm)	Zinc Doping (%)	Deposition time (min)	Average Grain Size (µm)
Optimization of Deposition Temperatures	S3_1	575	485	1.5	Si (211)	200/100	5	3	1.002
	S3_2	585	485	1.5	Si (211)	200/100	5	3	0.894
	S3_3	585	485	1.5	Si (211)	200/100	5	1.5	0.973
	S3_4	585	485	1.5	Si (211)	200/100	5	2	0.812
	S3_5	595	485	1.5	Si (211)	200/100	5	2	3.469
	S3_6	600	470	1.5	Si (211)	200/100	10	5	0.778
	S3_7	585	485	1.5	Si (211)	200/100	10	2	0.181
	S3_8	595	480	1.5	Si (211)	200/100	5	2	0.783
	S3_9	565	475	1.5	Si (211)	200/100	5	3	0.397
	S3_10	575	495	1.5	Si (211)	200/100	5	1.5	2.359
	S3_11	565	455	1.5	Si (211)	200/100	5	3	0.543
	S3_12	565	485	1.5	Si (211)	200/100	5	3	4.897
	S3_13	565	445	1.5	Si (211)	200/100	5	3	0.315
	S3_14	575	485	1.5	Si (211)	200/100	10	5	0.143
	S3_15	575	485	1.5	Si (211)	200/100	10	8.5	0.222
	S3_16	570	485	1.5	Si (211)	200/100	10	3	0.872
	S3_17	580	485	1.5	Si (211)	200/100	10	5	0.111

Sample S3_1 is implemented based on the previous results of Set II. The growth results in big grains that appear polycrystalline, with some smaller grains with smooth surfaces. The small grains appear crystalline and the surface of the grain is misoriented from the surface of the substrate.

Sample S3_2 shows the best growth from Set III, with 5% Zn. A source temperature of 585˚C and substrate temperature of 485˚C is used for sample S3_2 (Fig. 4.31). The growth is improved and resulted in big and small grains that appear crystalline in structure. Along with these types of grains, there are rod shaped and V shaped grains occurring as well. The V shaped grains are parallel with the substrate surface, and appear to show two grains joined in the middle.

Samples S3_3 and S3_4 are grown at the same temperature as sample S3_2, but with reduced time. Fig. 4.32, shows the growth of sample S3_3 at 1:30 minutes and results in less growth, most of the grains are large with a few small grains. This can explain the high substrate temperature, which results in less nucleation sites. The atoms from the source travel further on the substrate before nucleating on the pillars. The growth of S3_4 shows the growth when the time is increased to 2 minutes (Fig. 4.33). This growth is different from the two previous samples and results in the larger grains appearing more polycrystalline in structure.

The growth for sample S3_5, where the substrate temperature is kept at 485˚C and the source temperature is increased to 595˚C is shown in Fig. 4.34. The effect of change in the pattern from a square to a checkerboard pattern can be seen on this pattern. It can be observed that the CdTe growth favors the pattern area vs the non-pattern area. This change in the pattern also affects the growth. The patterned area shows the greatest growth rate compared to the two previous patterns. The entire patterned area is covered and the growth appears polycrystalline. Some of the larger grains have flat smooth surfaces, are parallel to the substrate surface, and some have a pyramid shape. The grains in this sample are the largest in Set III at 3.469 μm.

The growth for sample S3_6 is the first sample with 10% Zn (Fig.4.35), with a source temperature of 600˚C and a substrate temperature of 470˚C. These temperatures are chosen to ensure sublimation of the source, and are based on the literature [63, 66]. There is a good amount of growth with rod type grains, needle grains, and polycrystalline grains. The polycrystalline grains are the most abundant in this sample. Closer to the center of the sample the entire area is covered with growth.

The growth for sample S3_7, is doped with 10% Zn, has a source temperature of 585˚C, and a substrate temperature of 485˚C (Fig. 4.36). There is less growth, than in sample S3_6, but

more growth on each pillar than the 5% Zn samples. Most of the growth is composed of three nucleation sites on each pillar with rod like growth. This sample has the most rod like grains. The rod like grains are more vertical than previous samples.

The temperature is changed for sample S3_8, with a source temperature of 595˚C, a substrate temperature of 480˚C, and the doing is decreased back to 5% Zn for sample S3_8 (Fig. 4.37). The temperature of the source is increased from sample S3_5, to 595˚C to see if it would result in larger crystalline grains. The grains size does increase, but the larger grains appear polycrystalline.

The source and substrate temperature are lower than the rest of the Set III for sample S3_9 (Fig. 4.38), with a source temperature of 565˚C and substrate temperature of 475˚C. The temperature is decreased to see the effect of the growth on 100 nm x 200 nm pattern. The time is increased from 2 minutes to 3 minutes; due to a lower temperature, which slows down the growth rate, and 5% Zn doping is used. The growth of the smaller grains appears crystalline. Some of the grains are misoriented from the surface of the substrate. The growth for the larger grains results in three grains growing per nucleation site. The three grains per nucleation site do not have needle like ends; but rather have flat ends that are not parallel to the surface of the substrate.

The CdTe growth with a source temperature of 575˚C, a substrate temperature of 495˚C, and 5% Zn doping is used for sample S3_10 (Fig. 4.39). The substrate temperature is increased from 475˚C to 495˚C to reduce the number of nucleation sites, and the source temperature is increased in order to increase the grain size. The time is reduced to decrease the number of grains. This growth results in larger grains and less nucleation sites (Fig. 4.39). Few grains are crystalline and most appear to be polycrystalline.

The same source temperature of 565˚C as used in S3_9 is used and the substrate temperature is reduced of 455˚C for sample S3_11 (Fig. 4.40). The time of deposition is 3 minutes with a Zn doping of 5%. The reduction in the substrate temperature took place to help increase the number of nucleation sites. The growth results in less nucleation sites than in sample S3_9. The growth results in smaller grains being crystalline, the larger grains appearing to be polycrystalline, and the average grain size is larger in S3_11 than in sample S3_9.

The same source temperature of 565˚C as sample S3_11 is used and the substrate temperature is increased from 455˚C to 485˚C for S3_12 (Fig. 4.41). The deposition time is 3 minutes with 5% Zn doping. The increase of the substrate temperature results in less nucleation. There are a few small grains that are single crystal, few grains appear to have a V-shape, and larger grains are polycrystalline.

The source temperature is the same as sample S3_12 and the substrate temperature is further reduced to 445˚C for sample S3_13 (Fig. 4.42). The deposition time is 3 minutes and the source is doped with 5% Zn. The CdTe growth results in the most nucleation on individual pillars with small grains. The small and medium-sized grains appear cystalline and the large grains appear polycrystalline.

For sample S3_14, the doping is increased to 10% Zn, with a time of 5 minutes, a source temperature is 575˚C and a substrate temperature of 485˚C (Fig. 4.43). The growth quality appears to be crystalline, but the growth is only on a small percentage of the pattern.

The same parameters as sample S3_14 are used for sample S3_15, with an increased in deposition time of 8:30 minutes (Fig. 4.44). There is more growth and the grains are larger than in sample S3_14. The small grains are single crystal and the larger grains are a mix of crystalline

and polycrystalline. The large grains are merge together, but most grain surface are misoriented with respect to the surface of the substrate.

The same substrate temperature of 485˚C, with a lower source temperature of 570˚C are used for sample S3_16 (Fig. 4.45). The source temperature is increased to 580˚C for samples S3_17 (Fig. 4.46). Both samples have a doping of 10% Zn, sample S3_16 has a deposition time of 3 minutes, and sample S3_17 has a deposition time of 5 minutes. As a result of the low deposition time, there is little growth on sample S3_16. Sample S3_17, has growth on all of the pillars and merging of grains can be observed, but some of these grains have a rough surface. The individual grains have smooth surfaces and appear to be crystalline. Sample S3_17 was selected for TEM analysis.

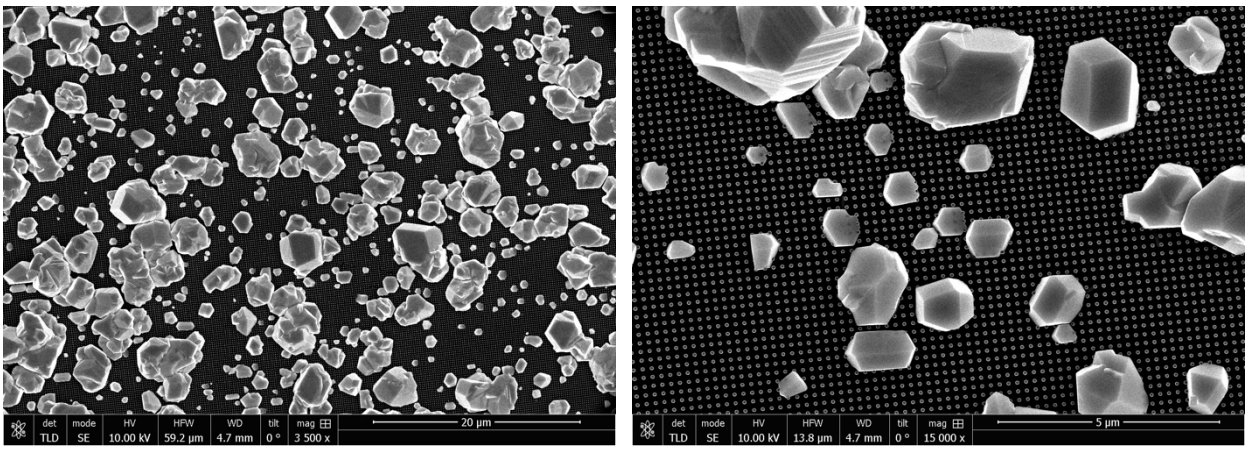


FIGURE 4.30: SAMPLE S3_1, SI (211), 100 NM X 200 NM PATTERN, 5% ZN DOPING, TIME =3 MIN., T_{SOURCE}= 575˚C AND $T_{SUBSTRATE}$= 485˚C.

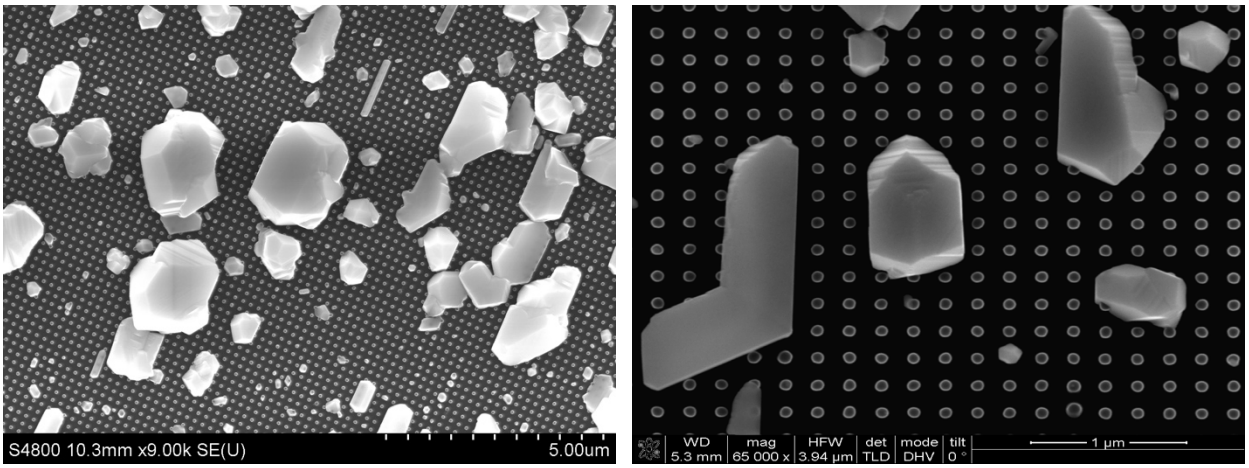


FIGURE 4.31: SAMPLE S3_2, SI (211), 100 NM X 200 NM PATTERN, 5% ZN DOPING, TIME =3 MIN., T_{SOURCE}= 585˚C AND $T_{SUBSTRATE}$= 485˚C.

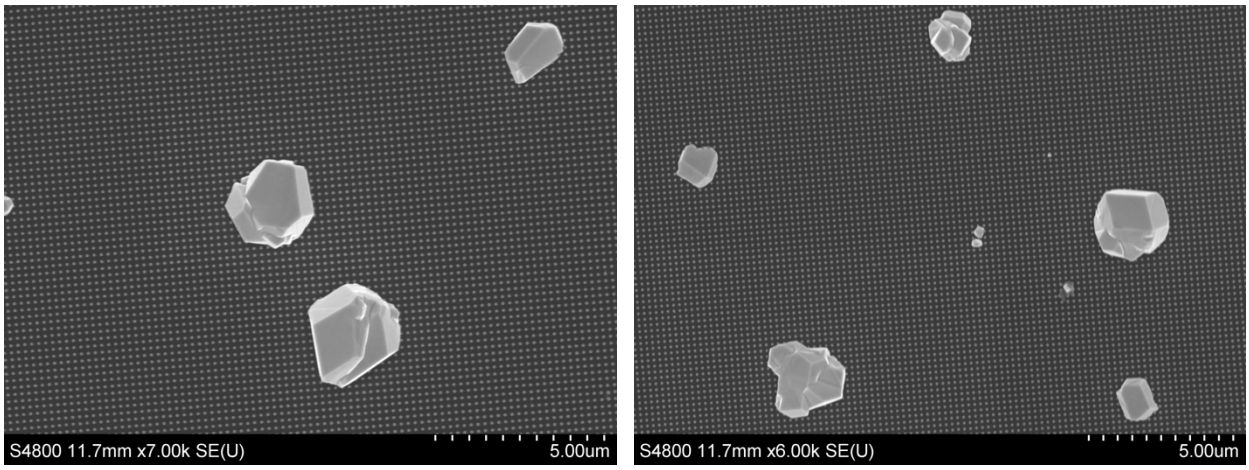


FIGURE 4.32: SAMPLE S3_3, SI (211), 100 NM X 200 NM PATTERN, 5% ZN DOPING, TIME =1:30 MIN., T_{SOURCE}= 585˚C AND $T_{SUBSTRATE}$= 485˚C.

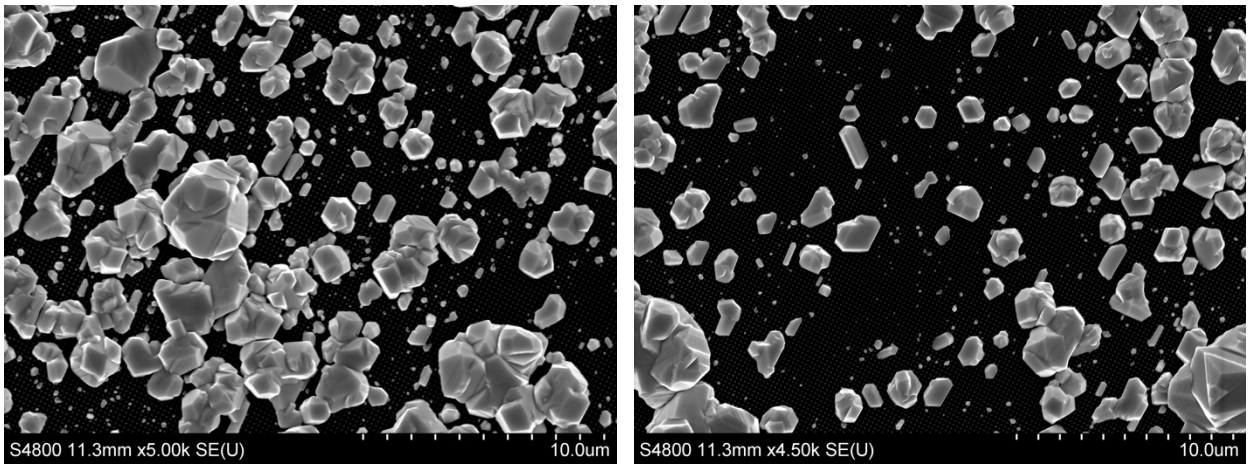


FIGURE 4.33: SAMPLE S3_4, SI (211), 100 NM X 200 NM PATTERN, 5% ZN DOPING, TIME =2 MIN., T_{SOURCE}= 585˚C AND $T_{SUBSTRATE}$= 485˚C.

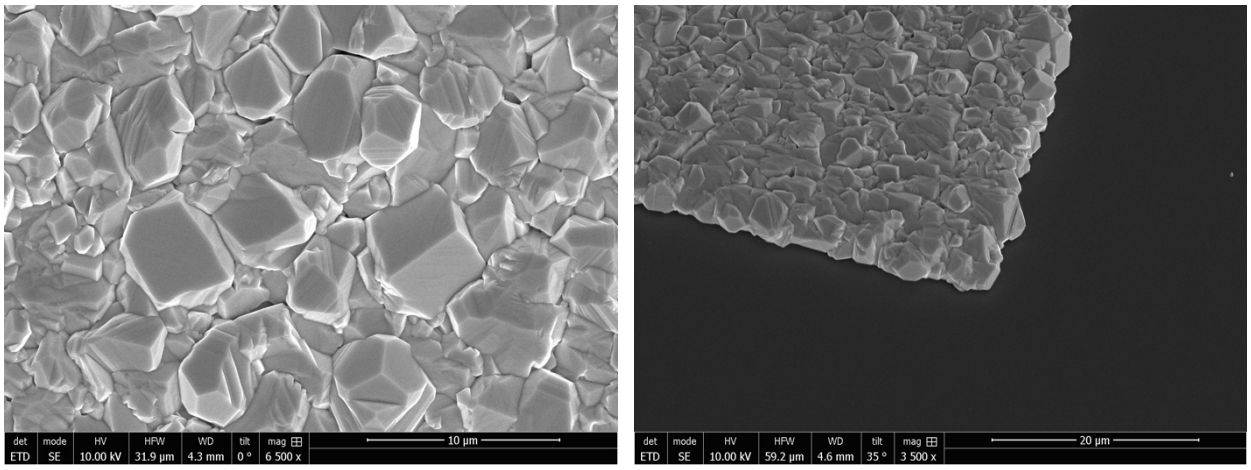


FIGURE 4.34: SAMPLE S3_5, SI (211), 100 NM X 200 NM PATTERN, 5% ZN DOPING, TIME =2 MIN., T_{SOURCE}= 595˚C AND $T_{SUBSTRATE}$= 485˚C.

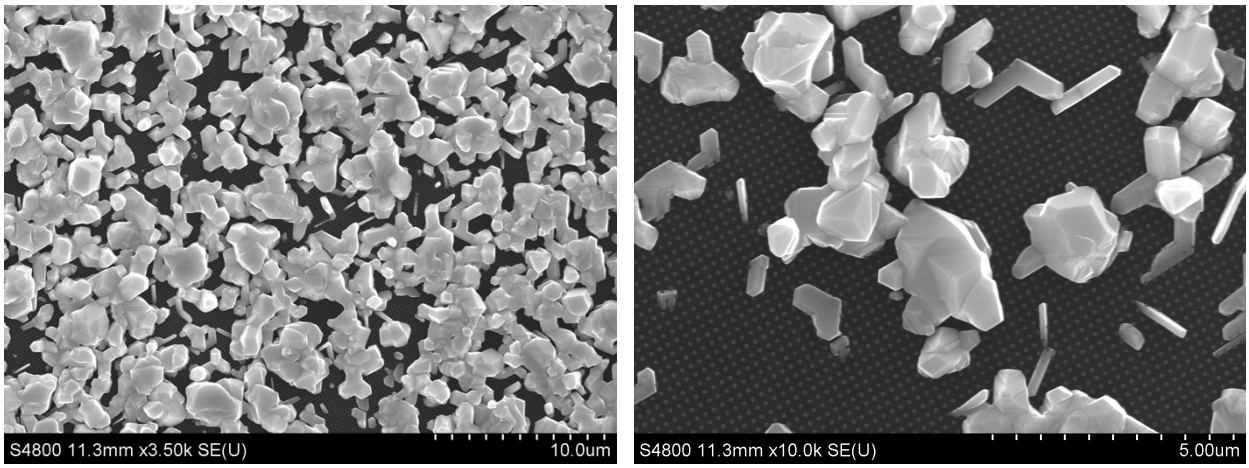


FIGURE 4.35: SAMPLE S3_6, SI (211), 100 NM X 200 NM PATTERN, 10% ZN DOPING, TIME =5 MIN., T_{SOURCE}= 600˚C AND $T_{SUBSTRATE}$= 470˚C.

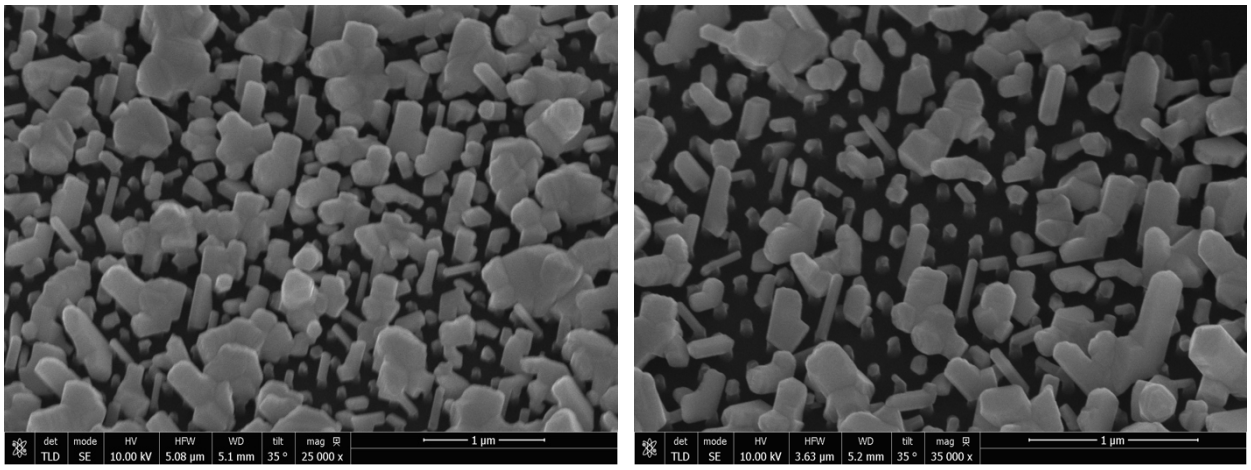


FIGURE 4.36: SAMPLE S3_7, SI (211), 100 NM X 200 NM PATTERN, 10% ZN DOPING, TIME =2 MIN., T_{SOURCE}= 585˚C AND $T_{SUBSTRATE}$= 485˚C.

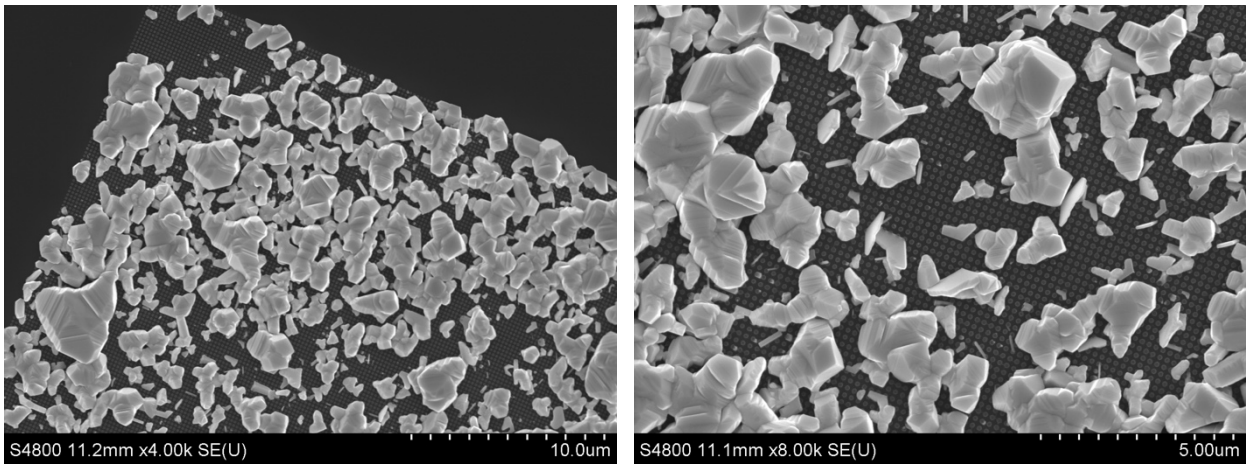


FIGURE 4.37: SAMPLE S3_8, SI (211), 100 NM X 200 NM PATTERN, 5% ZN DOPING, TIME =2 MIN., T_{SOURCE}= 595˚C AND $T_{SUBSTRATE}$= 480˚C.

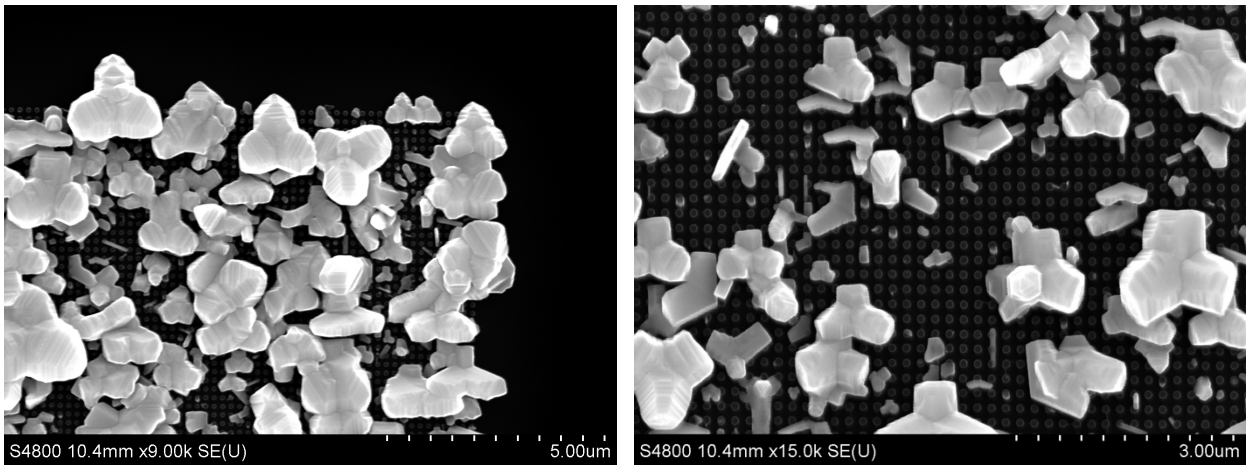


FIGURE 4.38: SAMPLE S3_9, SI (211), 100 NM X 200 NM PATTERN, 5% ZN DOPING, TIME =3 MIN., T_{SOURCE}= 565˚C AND $T_{SUBSTRATE}$= 475˚C.

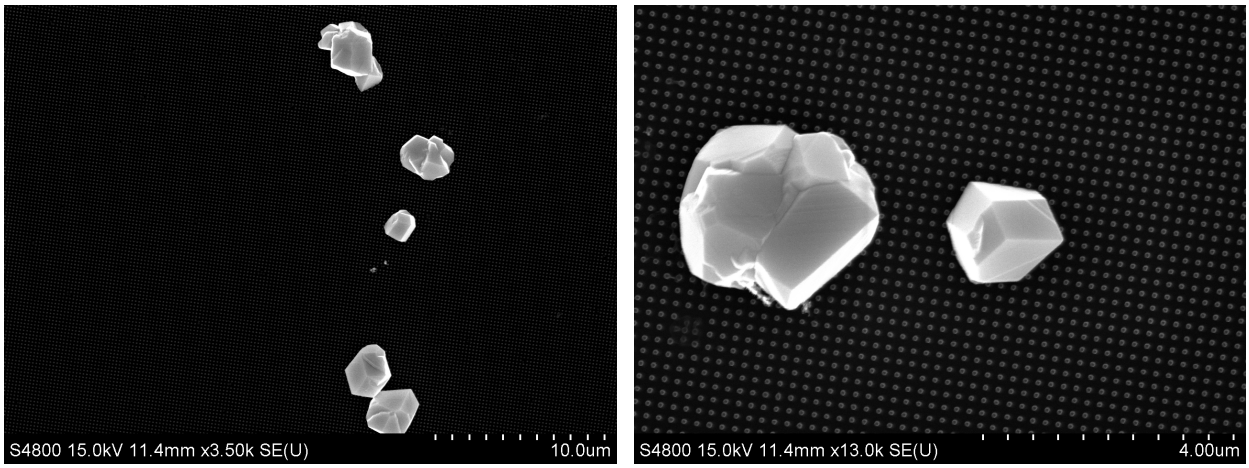


FIGURE 4.39: SAMPLE S3_10, SI (211), 100 NM X 200 NM PATTERN, 5% ZN DOPING, TIME =1:45 MIN., T_{SOURCE}= 575˚C AND $T_{SUBSTRATE}$= 495˚C.

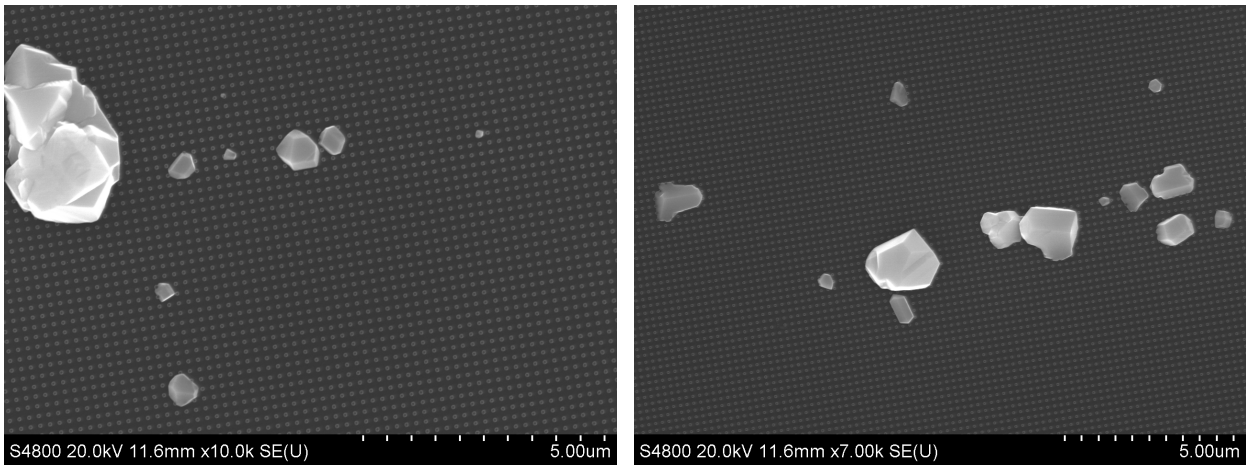


FIGURE 4.40: SAMPLE S3_11, SI (211), 100 NM X 200 NM PATTERN, 5% ZN DOPING, TIME =3 MIN., T_{SOURCE}= 565˚C AND $T_{SUBSTRATE}$= 455˚C.

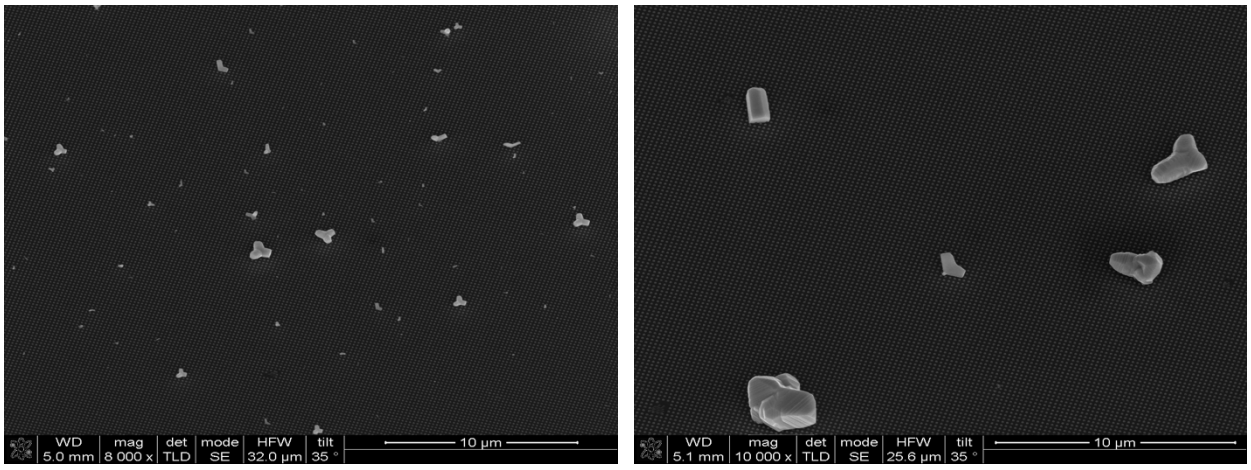


FIGURE 4.41: SAMPLE S3_12, SI (211), 100 NM X 200 NM PATTERN, 5% ZN DOPING, TIME =3 MIN., T_{SOURCE}= 565˚C AND $T_{SUBSTRATE}$= 485˚C.

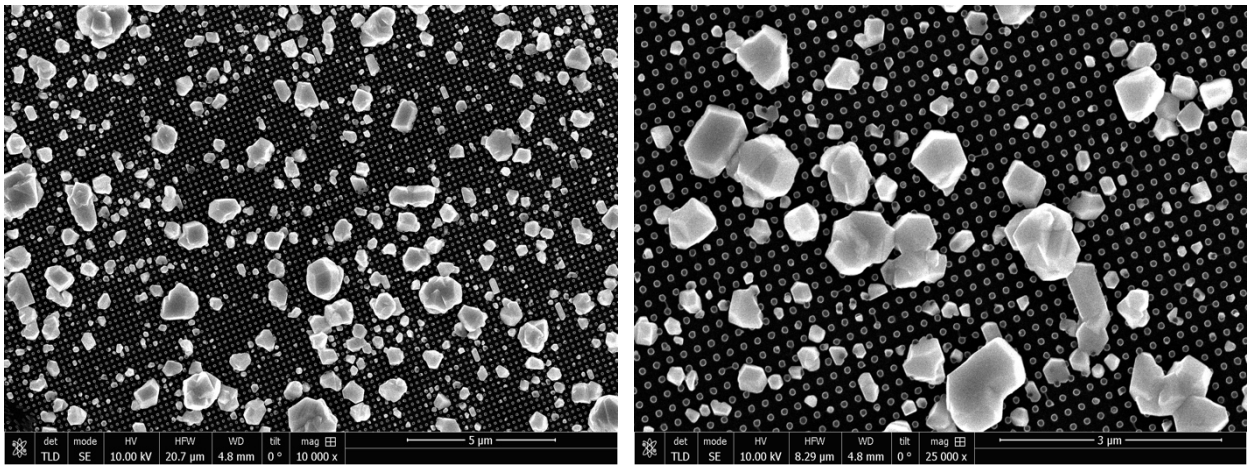


FIGURE 4.42: SAMPLE S3_13, SI (211), 100 NM X 200 NM PATTERN, 5% ZN DOPING, TIME =3 MIN., T_{SOURCE}= 565˚C AND $T_{SUBSTRATE}$= 445˚C.

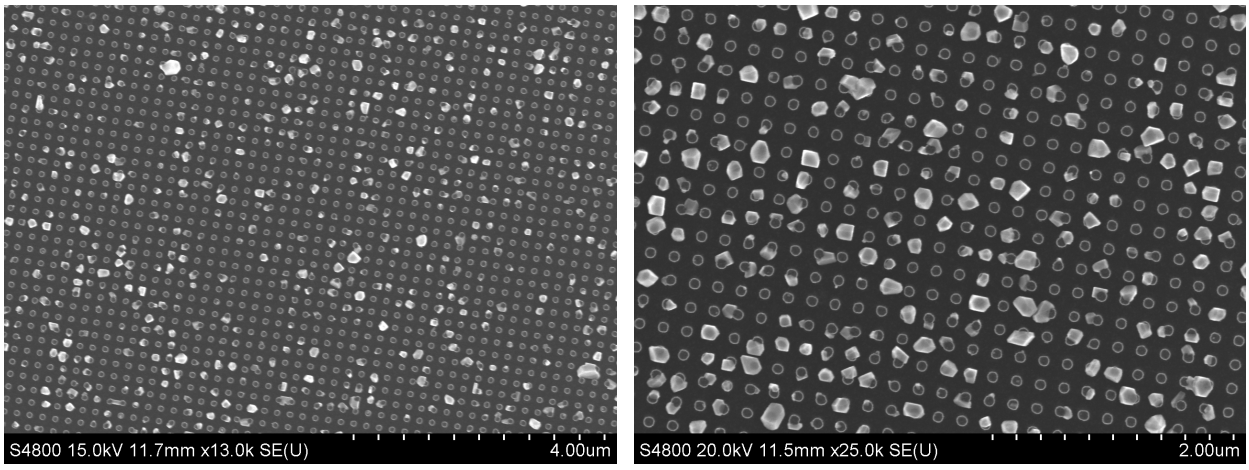


FIGURE 4.43: SAMPLE S3_14, SI (211), 100 NM X 200 NM PATTERN, 10% ZN DOPING, TIME =5 MIN., T_{SOURCE}= 575˚C AND $T_{SUBSTRATE}$= 485˚C.

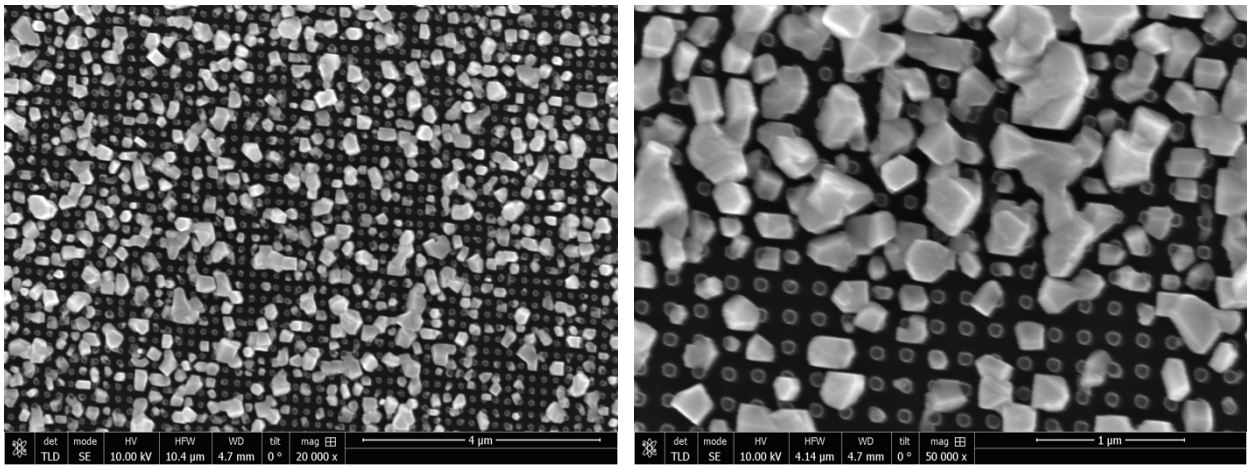


FIGURE 4.44: SAMPLE S3_15, SI (211), 100 NM X 200 NM PATTERN, 10% ZN DOPING, TIME =8:30 MIN., T_{SOURCE}= 575˚C AND $T_{SUBSTRATE}$= 485˚C.

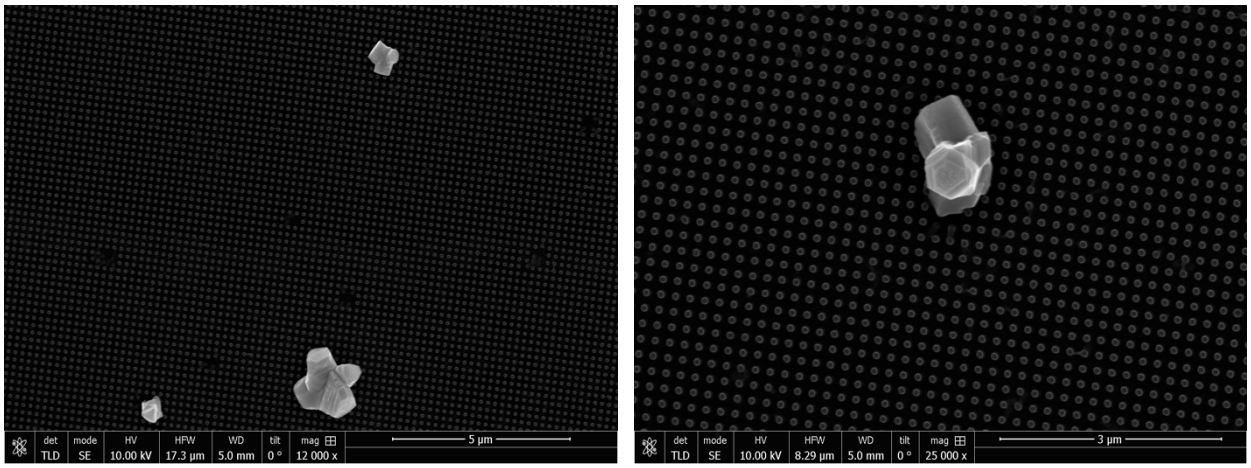


FIGURE 4.45: SAMPLE S3_16, SI (211), 100 NM X 200 NM PATTERN, 10% ZN DOPING, TIME =3MIN., T_{SOURCE}= 570˚C AND $T_{SUBSTRATE}$= 485˚C.

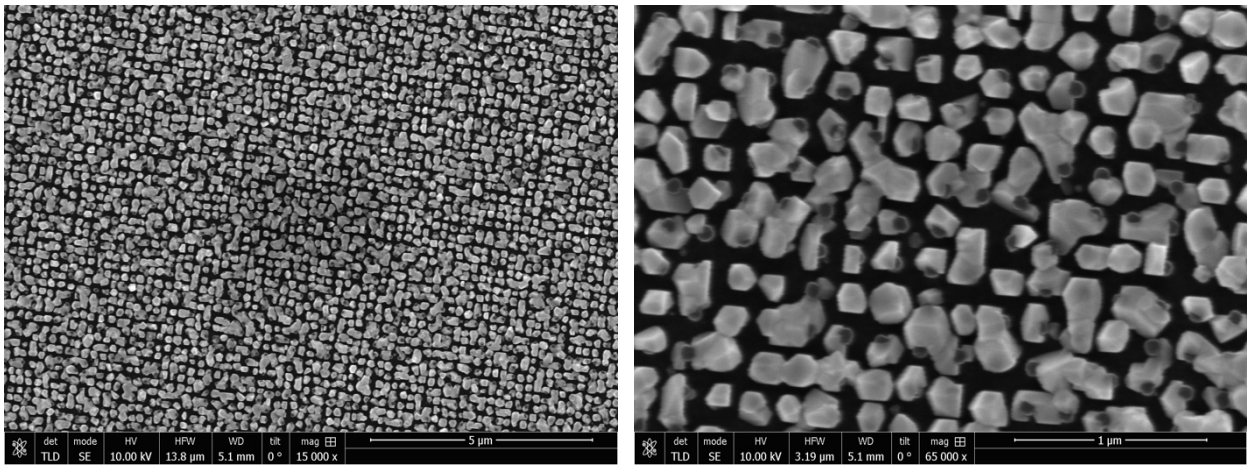


FIGURE 4.46: SAMPLE S3_17, SI (211), 100 NM X 200 NM PATTERN, 10% ZN DOPING, TIME =5 MIN., T_{SOURCE}= 580˚C AND $T_{SUBSTRATE}$= 485˚C.

4.2.5 CDTE DOPED WITH 5% AND 10% ZN GROWN ON SI(211) WITH 50 X 100 NM PATTERN (SET IV)

The fourth set of experiments are performed to find the ideal growth temperatures for CdTe doped with 5% and 10% growth on Si (211) substrates, while reducing the diameter and

pitch to the smallest dimensions in this study. A pitch of 100 nm and a pillar diameter of 50 nm and a p/d ratio of two is used for Set IV. The source is annealed before each experiment to ensure a clean surface of the source for sublimation. For Set IV experiments, the deposition time is varied from 2 minutes to 7 minutes and pressure is approximately 1.5 Torr.

The source temperature is varied from 565˚C to 585˚C and the substrate temperature is varied from 455˚C to 485˚C for Zn with 5%. The source temperature varies from 575˚C to 580˚C and the substrate temperature varies from 465˚C to 485˚C for Zn with 10%. Two CdTe sources contain twins and is doped with 5% and 10% Zn. In this set of experiments, the etch process is with CF_4 and Ar, and as a result of a thinner resist, the etch time is reduced 4:30 minutes. The growth parameters for Set IV are shown in Table 4.7, and SEM micrographs of the samples are included in Figs. 4.47 through 4.54.

TABLE 4.7: SUMMARY OF GROWTH PARAMETERS FOR SET IV

Fabrication Parameters	Sample name	Tsor (˚C)	Tsub (˚C)	Reactor Pressure (Torr)	Substrate	Pitch/Diameter (nm)	Zinc Doping (%)	Deposition time (min)	Average Grain Size (µm)
Optimization of Deposition Temperatures	S4_1	585	485	1.5	Si (211)	100/50	5	2	2.45
	S4_2	565	465	1.5	Si (211)	100/50	5	2	1.983
	S4_3	565	455	1.5	Si (211)	100/50	5	2	0.391
	S4_4	565	455	1.5	Si (211)	100/50	5	2:30	0.453
	S4_5	580	485	1.5	Si (211)	100/50	10	3	0.288
	S4_6	580	475	1.5	Si (211)	100/50	10	3	0.253
	S4_7	575	475	1.5	Si (211)	100/50	10	7	0.255
	S4_8	575	465	1.5	Si (211)	100/50	10	5	0.136

The growth of sample S4_1 has a source temperature of 585˚C and a substrate temperature of 485˚C (Fig. 4.47). This temperature is chosen from the initial results of Set III. This smaller pattern resulted in higher deposition on pattern area, than in Set III. The pillars are

not shown, and the growth is polycrystalline. Based on these results the temperature is reduced for the next experiments with 5% Zn doping.

The source temperature is reduced to 565˚C and the substrate temperature is 465˚C, for sample S4_2 (Fig. 4.48). This results in less growth and larger grains. Few grains are single crystal, a few have a smooth flat surface, and the rest of the grains are polycrystalline.

Sample S4_3 keeps the same source temperature and time as sample S4_2, but reduces the substrate temperature to 455˚C (Fig. 4.49). This increases the nucleation sites on the substrate and almost all the grains are single crystal for this growth. The smaller grains have flat, smooth surfaces, and the large size grains have a pyramid shaped.

Sample S4_4 has the same parameters as S4_3, but with 30 seconds added to the end of the deposition time. During this extra 30 seconds the source temperature is increased to 570˚C to increase the growth of the grains (Fig. 4.50). The grains size is larger than in sample S4_3, but results in most of the larger grains being polycrystalline, and the medium to small grains are crystalline.

The Zn doping is changed to 10% for sample S4_5, the source temperature is 580˚C, the substrate temperature is 485˚C, and the time is 3 minutes (Fig. 4.51). This is based on the best growth of Zn doping with 10% in Set III. The growth is less, occurs over multiple pillars, and has larger grains than the growth on sample S3_17. The growth has multiple grains with flat ends, few nucleation site and rod like grains.

Sample S4_6 has same source temperature, time, and the doping as the previous experiment, but reduces the substrate temperature from 485˚C to 475˚C in order to increase the number of nucleation sites (Fig. 4.52). The number of grains increases, the grains appear

polycrystalline, and the grains are growing upwards. Some small grains appear to be triangular and some look crystalline.

The source temperature is reduced to 575˚C for sample S4_7, and the substrate temperature is reduced to 475˚C (Fig. 4.53). The time is increased to 7 minutes due to the source sublimating less at this temperature. There is less growth for both the large and small grains, which appear to be crystalline, but a few of the large grains are polycrystalline. The small grains are on individual pillars, and the large grains have a combination of flat surfaces and rod shapes.

The substrate temperature further to 465˚C for sample S4_8, the time is reduced to 5 minutes, and the source temperature is the same, 575˚C (Fig. 4.54). Most of the small and medium grains are single crystal. The large grains are polycrystalline but are rare. This growth closely resembles the growth for sample S3_17 for 10% Zn. Sample S4_8 was selected for TEM analysis.

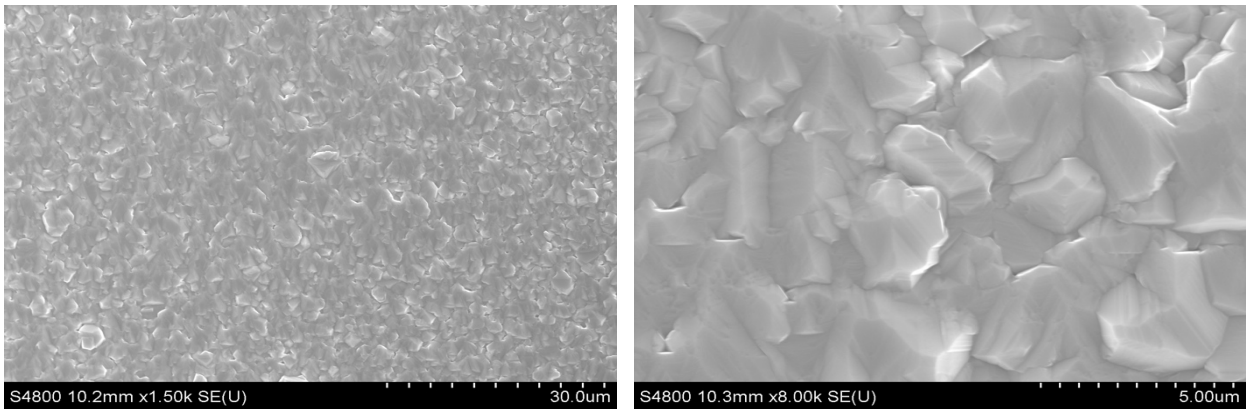


FIGURE 4.47: SAMPLE S4_1, SI (211), 50 NM X 100 NM PATTERN, TIME =2MIN, 5% ZN DOPING, T_{SOURCE}= 585˚C AND $T_{SUBSTRATE}$= 485˚C.

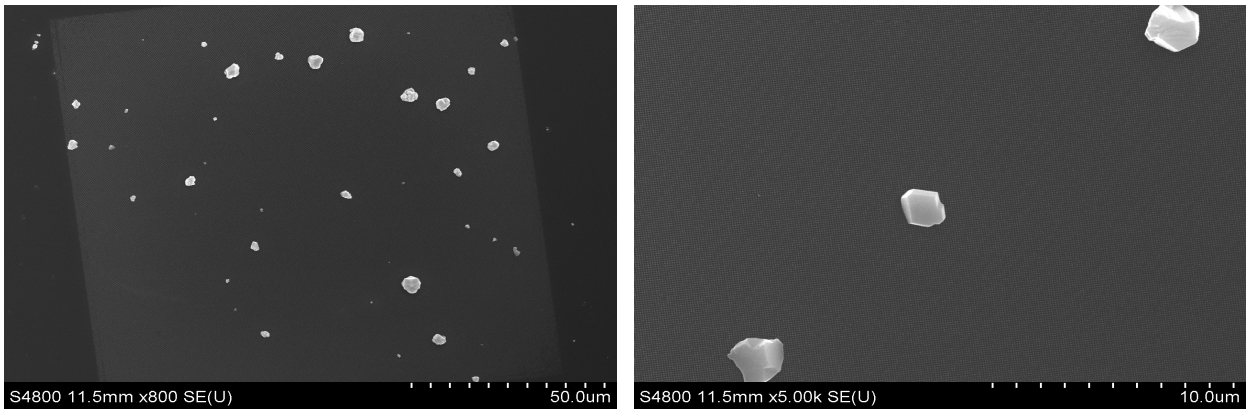


FIGURE 4.48: SAMPLE S4_2, SI (211), 50 NM X 100 NM PATTERN, TIME =2MIN, 5% ZN DOPING, T_{SOURCE}= 565˚C AND $T_{SUBSTRATE}$= 465˚C.

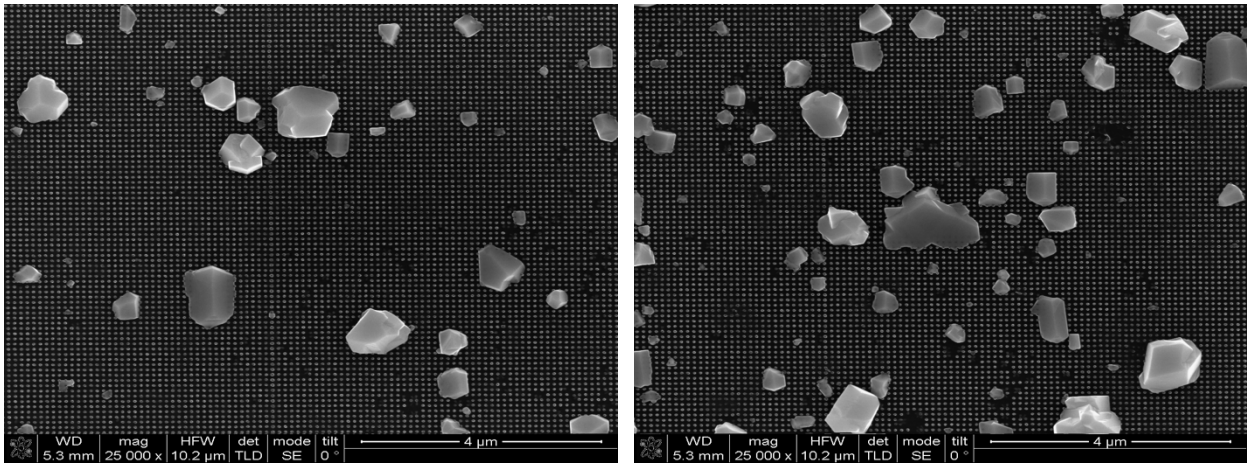


FIGURE 4.49: SAMPLE S4_3, SI (211), 50 NM X 100 NM PATTERN, TIME =2MIN, 5% ZN DOPING, T_{SOURCE}= 565˚C AND $T_{SUBSTRATE}$= 465˚C.

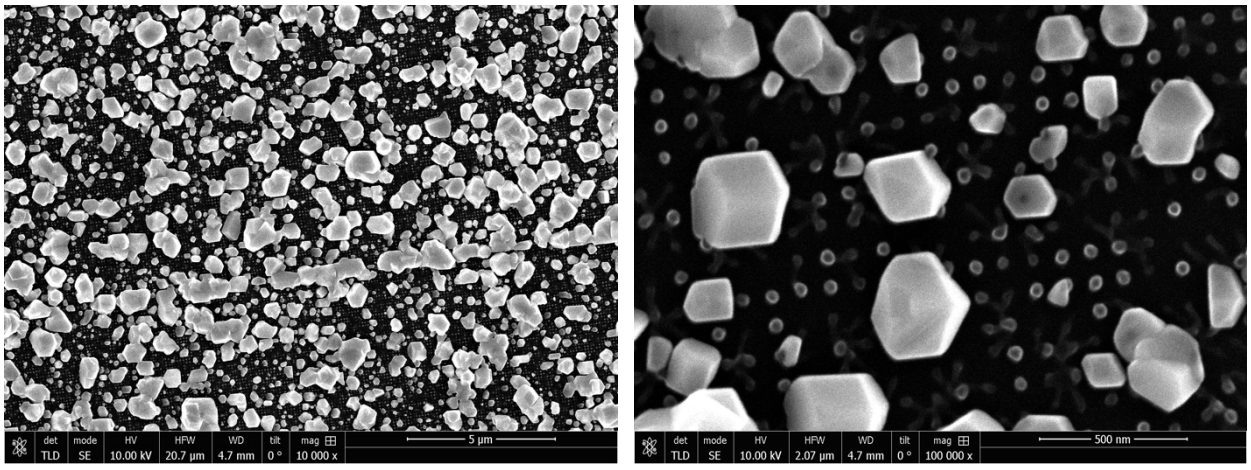


FIGURE 4.50: SAMPLE S4_4, SI (211), 50 NM X 100 NM PATTERN, TIME =2:30MIN, 5% ZN DOPING, T_{SOURCE}= 565˚C AND $T_{SUBSTRATE}$= 465˚C. WITH 30 SECOND RAMP UP OF T_{SOURCE} =570˚C

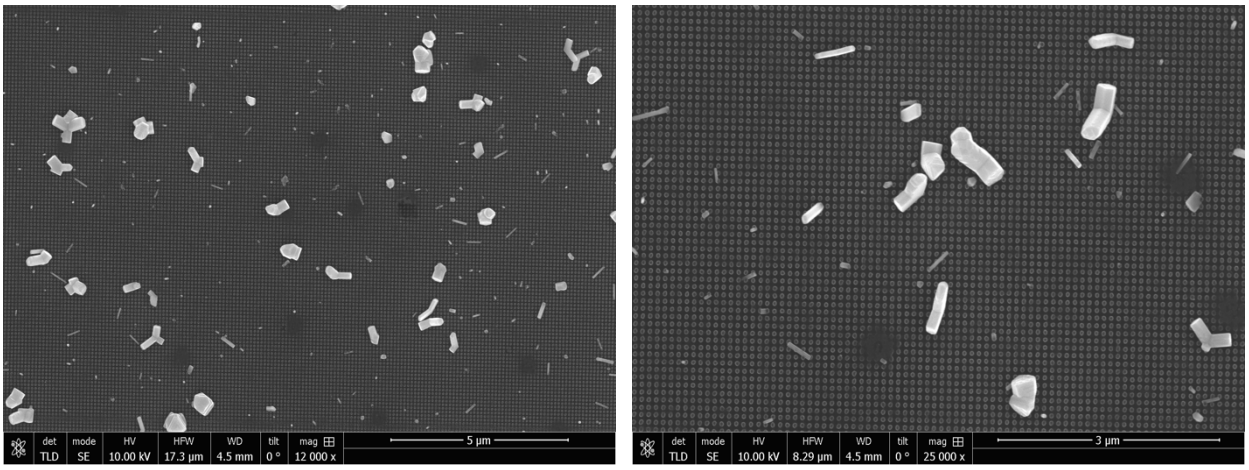


FIGURE 4.51: SAMPLE S4_5, SI (211), 50 NM X 100 NM PATTERN, TIME =3MIN, 10% ZN DOPING, T_{SOURCE}= 580˚C AND $T_{SUBSTRATE}$= 485˚C.

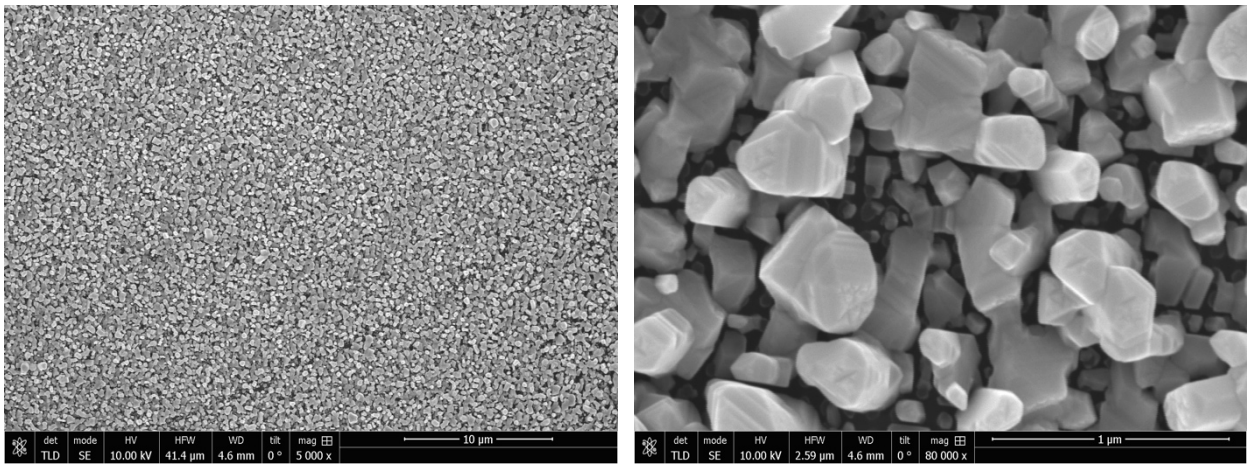


FIGURE 4.52: SAMPLE S4_6, SI (211), 50 NM X 100 NM PATTERN, TIME =3MIN, 10% ZN DOPING, T_{SOURCE}= 580˚C AND $T_{SUBSTRATE}$= 475˚C.

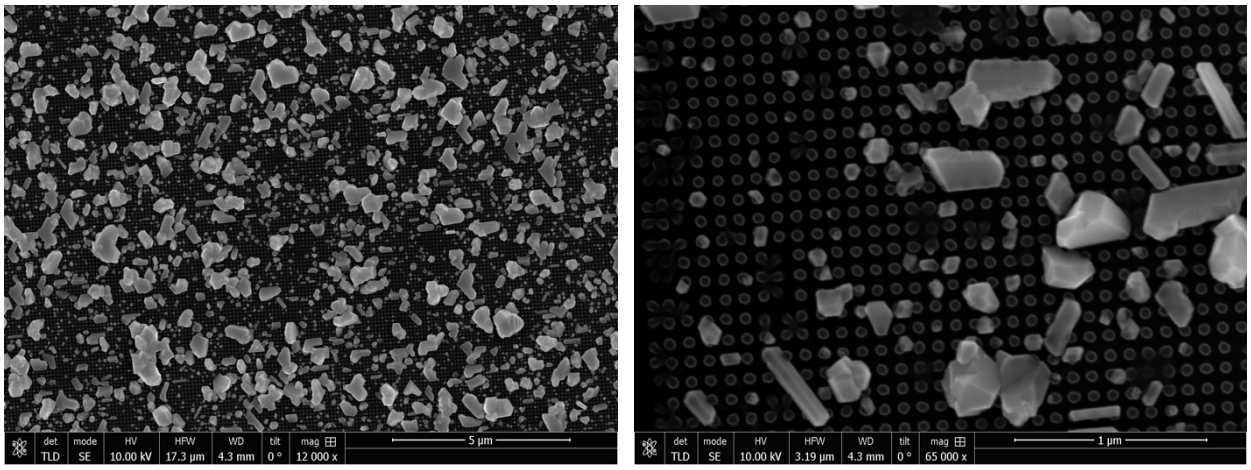


FIGURE 4.53: SAMPLE S4_7, SI (211), 50 NM X 100 NM PATTERN, TIME =7MIN, 10% ZN DOPING, T_{SOURCE}= 575˚C AND $T_{SUBSTRATE}$= 475˚C.

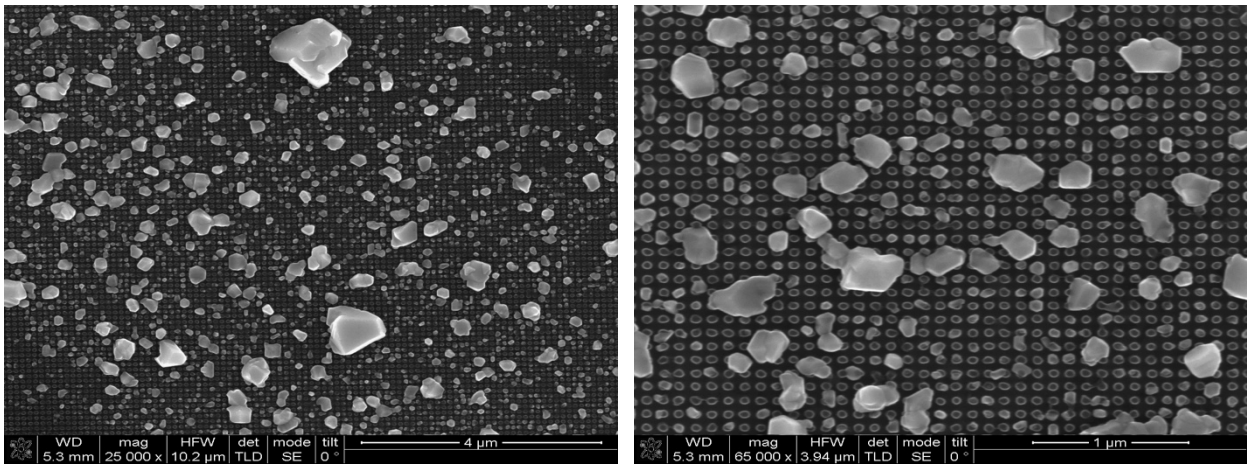


FIGURE 4.54: SAMPLE S4_8, SI (211), 50 NM X 100 NM PATTERN, TIME=5MIN, 10% ZN DOPING, T_{SOURCE}= 575˚C AND $T_{SUBSTRATE}$= 465˚C.

4.2.6 CDTE DOPED WITH 5% AND 10% ZN GROWN ON SI(111) WITH 50 X 100 NM PATTERN (SET V)

The fifth and final set of experiments are preformed to see the effect of changing the substrate orientation to Si(111) with CdTe doped with 5% and 10% Zn. A pitch of 100 nm, a pillar diameter of 50 nm, and a p/d ratio of two is used for Set V. The source is annealed before each experiment to ensure a clean surface of the source for sublimation. For Set V, the pressure is approximately 1.5 Torr, the deposition time is two minutes, a source temperature of 565˚C and substrate temperature of 455˚C are used for a CdTe doped source with 5% Zn. A deposition time of five minutes, a source temperature of 575˚C, and substrate temperature of 465˚C is used for a CdTe doped source with 10% Zn. The RIE etch process is CF_4 and Ar at 4:30 minutes. The growth parameters for Set V are shown in Table 4.8, and SEM micrographs of the samples are included in Figs. 4.55 and 4.56.

TABLE 4.8: SUMMARY OF GROWTH PARAMETERS FOR SET V

Fabrication Parameters	Sample name	Tsor (˚C)	Tsub (˚C)	Reactor Pressure (Torr)	Substrate	Pitch/Diameter (nm)	Zinc Doping (%)	Deposition time (min)	Average Grain Size (µm)
Optimization of Deposition Temperatures	S5_1	565	455	1.5	Si (111)	100/50	5	2	0.477
	S5_2	575	465	1.5	Si (111)	100/50	10	5	0.211

The growth for sample S5_1 is shown in Fig. 4.55. Compared to sample S4_3 (Fig. 4.47), the grains are slightly larger, and are polycrystalline in structure. There are small grains with flat surfaces, but those are more misoriented with respect to the substrate surface. The growth quality appears better in sample S4_3 comapred to S5_1.

The growth for sample S5_2 is shown in Fig. 4.56. Compared to sample S4_7 (Fig. 4.53), the growth appears similar. There are more of the larger grains in S5_2 that appear polycrystalline, than in S4_7. There appears to be more growth on sample S4_7, than in S5_2 with larger average grain size for sample S5_2.

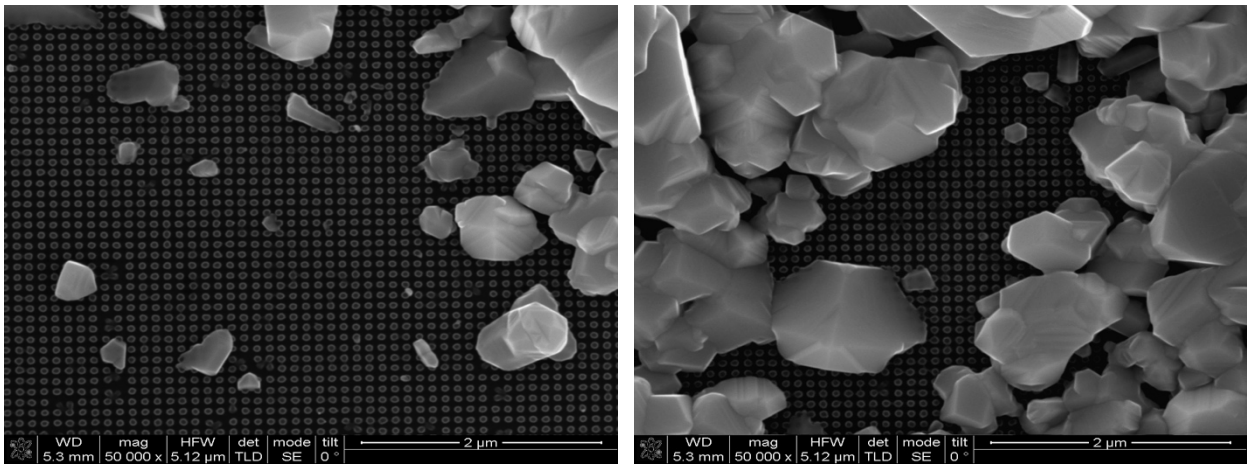


FIGURE 4.55: SAMPLE S5_1, SI (211), 50 NM X 100 NM PATTERN, TIME =2MIN, 5% ZN DOPING, T_{SOURCE}= 565˚C AND $T_{SUBSTRATE}$= 455˚C.

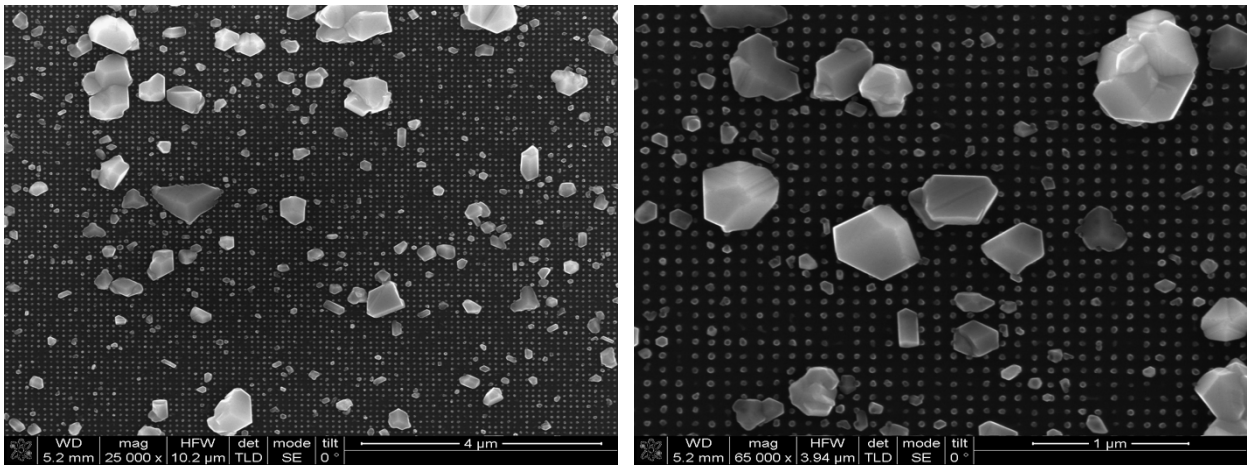


FIGURE 4.56: SAMPLE S5_2, SI (211), 50 NM X 100 NM PATTERN, TIME =2MIN, 10% ZN DOPING, T_{SOURCE}= 575˚C AND $T_{SUBSTRATE}$= 465˚C.

4.3 TEM Characterization of CdTe Doped with Zn

Transmission electron microscopy (TEM) analysis was performed on selective CdTe growth with 5% and 10% Zn doping on Si(211) and Si(111) substrates. TEM analysis was performed to (1) identify the grain structure, (2) determine the orientation of the CdTe growth

with respect to the Si pillar orientation, and (3) identify defects that result from the strain of the interface between CdTe and Si. The TEM analysis uses HRTEM mode and diffraction mode. The type of analysis includes:

- Indexing planes in the diffraction pattern
- Identifying the planes in the HRTEM images
- Comparing the calculated lattice plane spacing to theoretical values
- Measuring the angle of misorientation between specific planes at the CdTe/Si interface.
- Characterizing of structural defects at the CdTe /Si interface

4.3.1 SET I AND SET II TEM ANALYSIS

The TEM is used to analyze the structure of the CdTe growth doped with 5% Zn for Sets I and II. A HRTEM image, at the interface, for Sample S1_6 from Set I (200 nm x 600 nm pattern) and Sample S2_2 from Set II (200 nm x 400 nm pattern) are shown in Figs 4.57 and 4.58. Diffraction patterns are not available for these samples since they were analyzed at UTEP on a Cryo-TEM (JEOL JEM 3200 FS) which does not have the capability to function in diffraction mode.

Sample S1_6 with pattern 200 nm by 600 nm has threading dislocation in the film as identified in Fig. 4.59. Threading dislocation start at the interface and propagate 100 nm to 150 nm in the film. In the literature the threading dislocation travel through the entire film for 0.32 μm [75]. There are two grains visible in Fig. 4.59. The CdTe grain is not only on the Si pillar, but around the entire pillar. Fig. 4.60 shows a close up view of the CdTe/Si interface and as an oxide layer is present on Si surface, highlighted by the red square.

Sample S2_2, patterned with 200 nm pillars and a pitch of 400 nm has threading dislocation extending from the interface (Fig. 4.61). Threading dislocations extend further in sample S1_6 than in sample S2_2. There is only one CdTe grain visible in Fig. 4.61. The CdTe grain has grown around one side of the Si pillar.

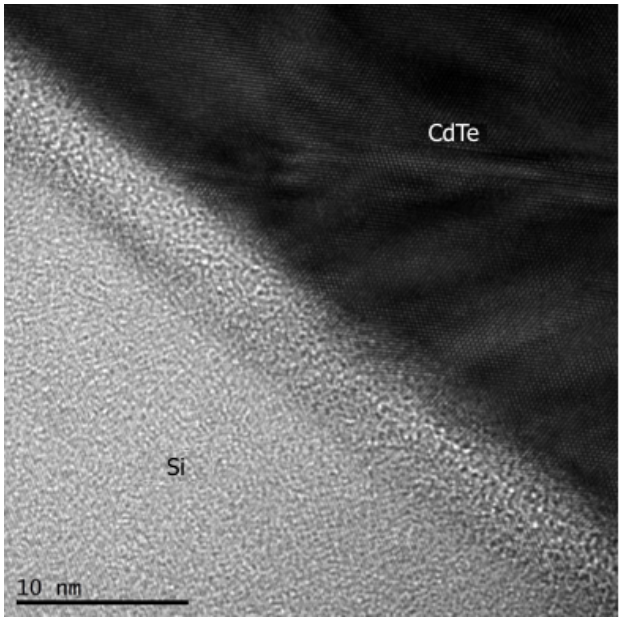


FIGURE 4.57: HRTEM IMAGE OF SAMPLE S1_6, SI(211) SUBSTRATE, 200 NM X 600 NM PATTERN, AND 5% ZN DOPING

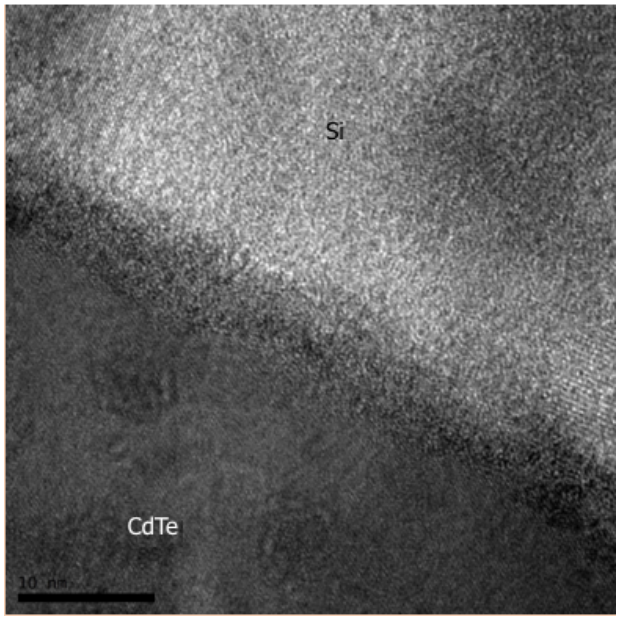


FIGURE 4.58: HRTEM IMAGE OF SAMPLE S2_2, SI(211) SUBSTRATE, 200 NM X 400 NM PATTERN, AND 5% ZN DOPING

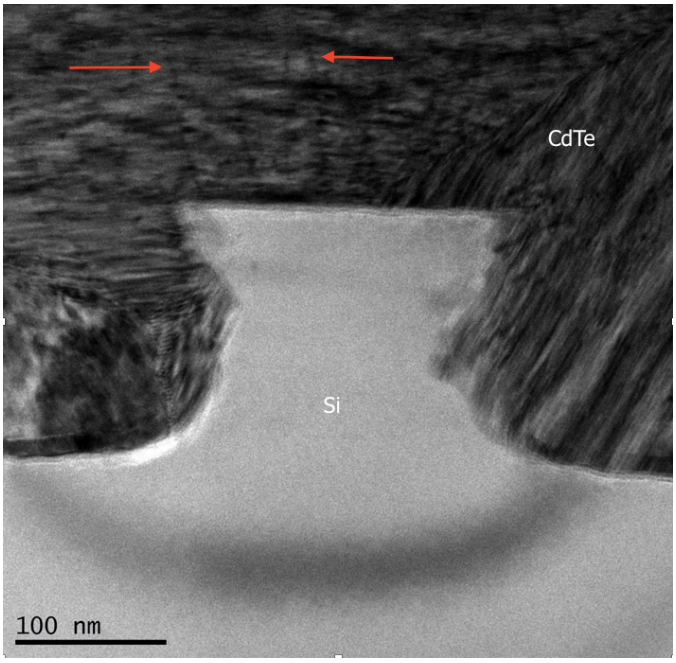


FIGURE 4.59: HRTEM OF SAMPLE S1_6 – CDTE GROWTH ON 200 NM X 600 NM PATTERNED SI(211) WITH THREADING DISLOCATIONS.

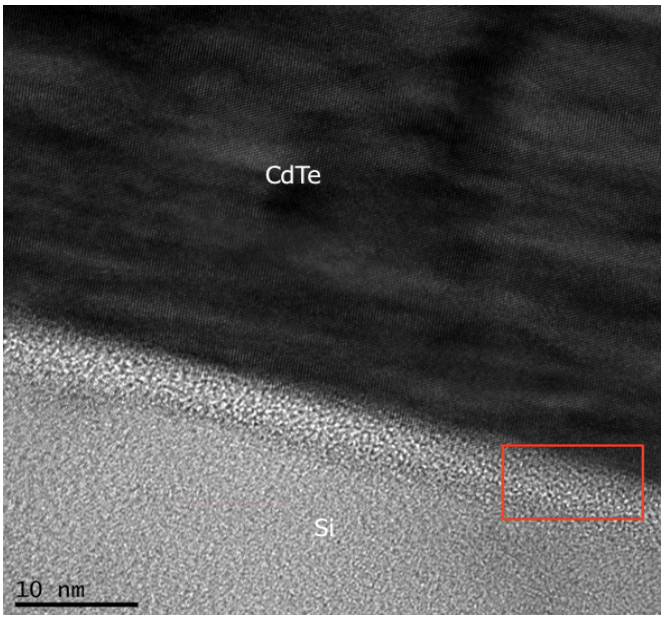


FIGURE 4.60: HRTEM OF SAMPLE S1_6 – CDTE GROWTH ON 200 NM X 600 NM PATTERNED SI(211) INTERFACE

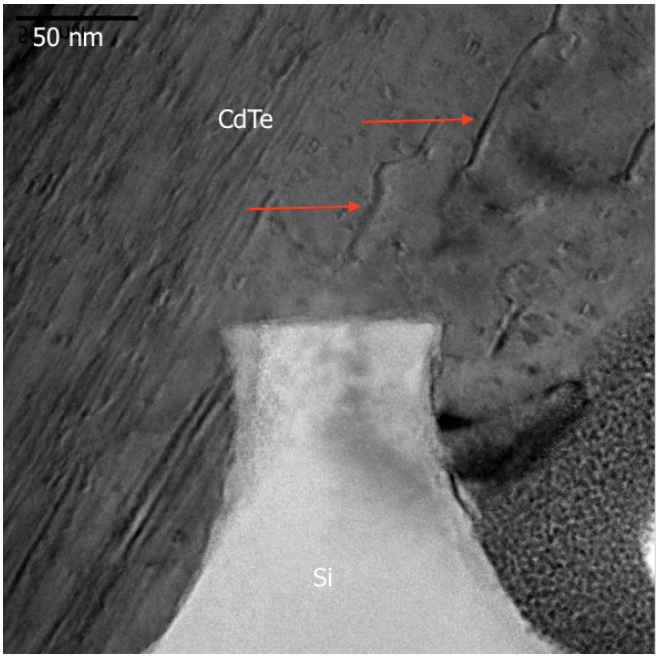


FIGURE 4.61: HRTEM OF SAMPLE S2_2 – CDTE GROWTH ON 200 NM X 400 NM PATTERNED SI(211) WITH THREADING DISLOCATIONS.

4.3.2 SET III TEM ANALYSIS

Figure 4.62 is a HRTEM image of the pillars for sample S3_2 (100 nm x 200 nm pattern with 5% Zn doping), illustrating the CdTe growth around the Si pillars. The corresponding diffraction patterns for this sample are included in Fig. 4.63(a) for Si(211), and Fig. 4.63(b) for a CdTe grain on this substrate.

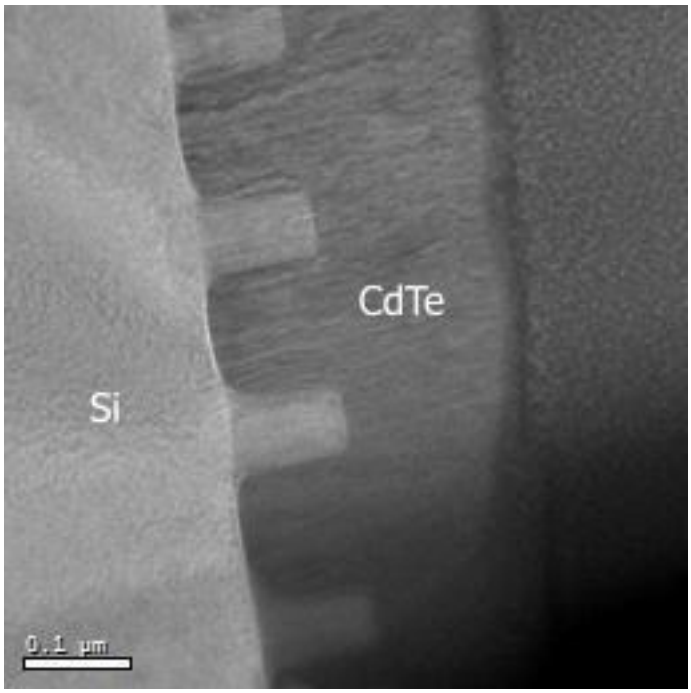
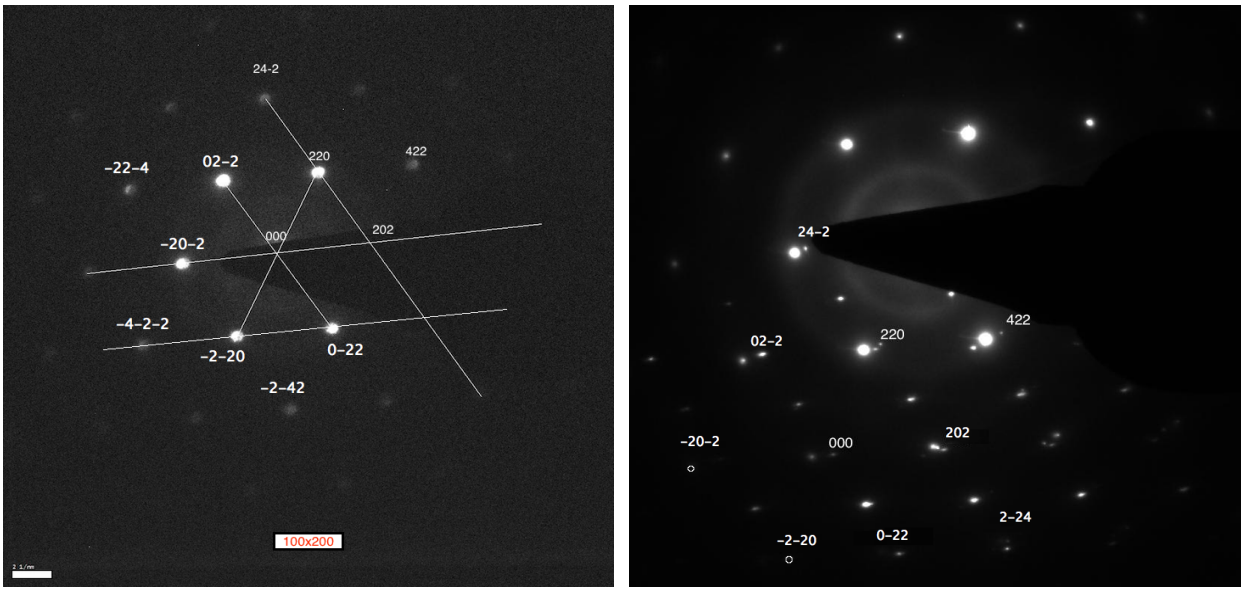


FIGURE 4.62: HRTEM IMAGE OF SAMPLE S3_2, SI(211) SUBSTRATE, 100 NM X 200 NM PATTERN, AND 5% ZN DOPING



(a) (b)

FIGURE 4.63: TEM DIFFRACTION PATTERNS FOR SAMPLE S3_2, SI(211), 100 NM X 200 NM 5% ZN (A) FOR SI(211) AND (B) FOR CDTE

The identification of the atomic planes on the HRTEM image is determined by transposing the identified planes from the diffraction pattern to the HRTEM image. This is accomplished by drawing a vector from the (000) orientation diffraction spot on the diffraction pattern to the diffraction spot of interest. The diffraction spot is associated with a (xyz) plane and corresponds to a [xyz] plane on the HRTEM image. The (xyz) planes on the HRTEM image lie perpendicular or normal to the vector on the diffraction pattern, and this is how the planes are identified on the HRTEM image. The atomic planes are verified using equation (4) in section 3.5.5. This equation calculates the angle between two planes and this value is compared to the angle measured on the HRTEM image between two identified planes.

Fig. 4.64 shows the corresponding HRTEM image of Sample S3_2, where the image on the left shows the orientation of the pillars for the HRTEM image on the right. The Si and CdTe

lattice planes are identified based on the diffraction pattern. The (24-2), (022), and (111) planes are identified for both the Si(211) substrate and the CdTe growth. The Si(111) orientation is not parallel with the surface of the Si pillar. Table 4.9 includes the theoretical and measured values for the angles between the (111) and (24-2) planes for both Si and CdTe. The values coincide, which confirms that the lattice planes identified on the image are correct. The selective growth for the CdTe growth on Si, without a buffer layer, has a misorientation angle of 0.2˚ for sample S3_2 in the (11) orientation (Fig. 4.65). The misorientation for sample S3_2 is less than the misorientation angle of 3.5˚, for growth of CdTe on Si a ZnTe buffer layer a [31].

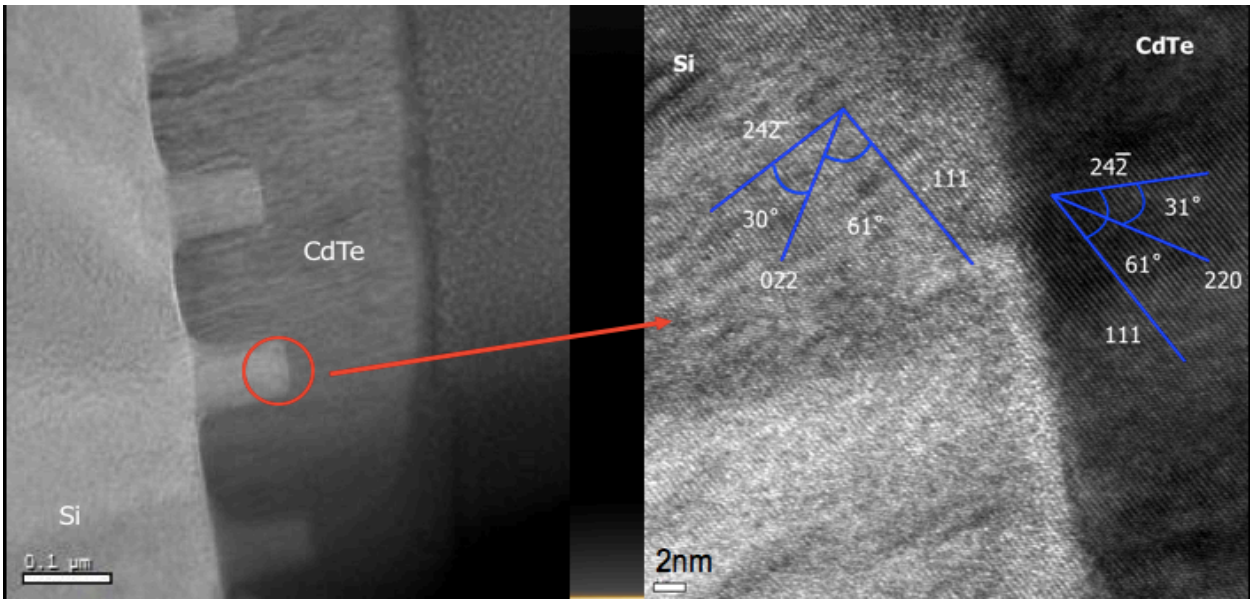


FIGURE 4.64: HRTEM IMAGE OF SAMPLE S3_2 - CDTE GROWTH ON 100 NM X 200 NM PATTERNED SI(211) WITH 5% ZN DOPING.

TABLE 4.9: MEASURED VS THEORETICAL ANGLES FOR HRTEM IMAGE FOR SAMPLE S3_2

	Plane 1	Plane 2	Theoretical (˚)	Measured (˚)
CdTe	111	24-2	90	91
Si	111	24-2	90	92

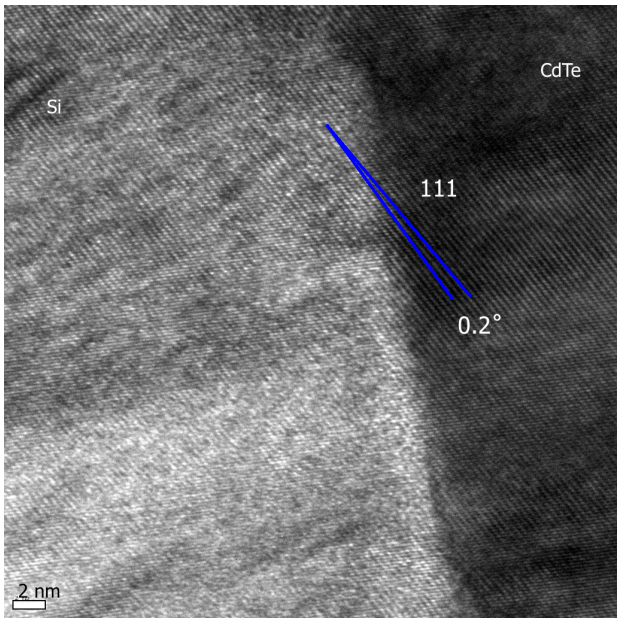


FIGURE 4.65: HRTEM OF SAMPLE S3_2 – CDTE GROWTH ON 100 NM BY 200 NM PATTERNED SI(211) WITH 10% ZN DOPING AND 0.2˚ MISORIENTATION IN THE (111) ORIENTATION.

Fig. 4.66 is a low magnification image of sample S3_17, which corresponds to the CdTe growth with 10% Zn doping on the 100 nm by 200 nm patterned Si(211) substrate. The indexed diffraction patterns for sample S3_17 are shown in Fig. 4.67(a) for Si and Fig. 4.67(b) for CdTe.

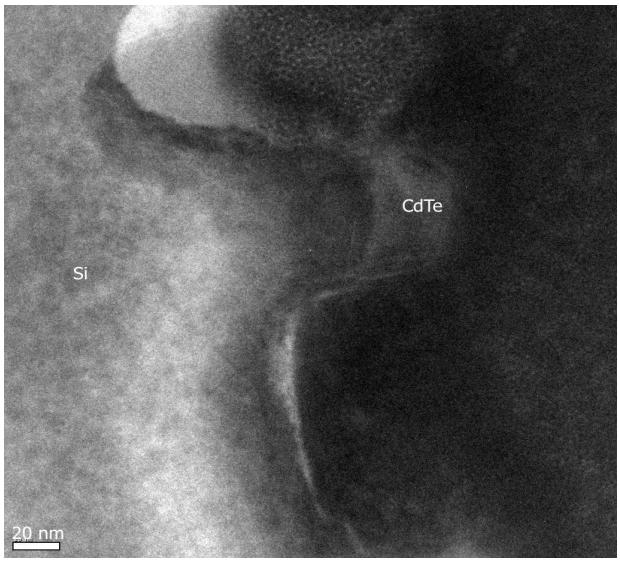
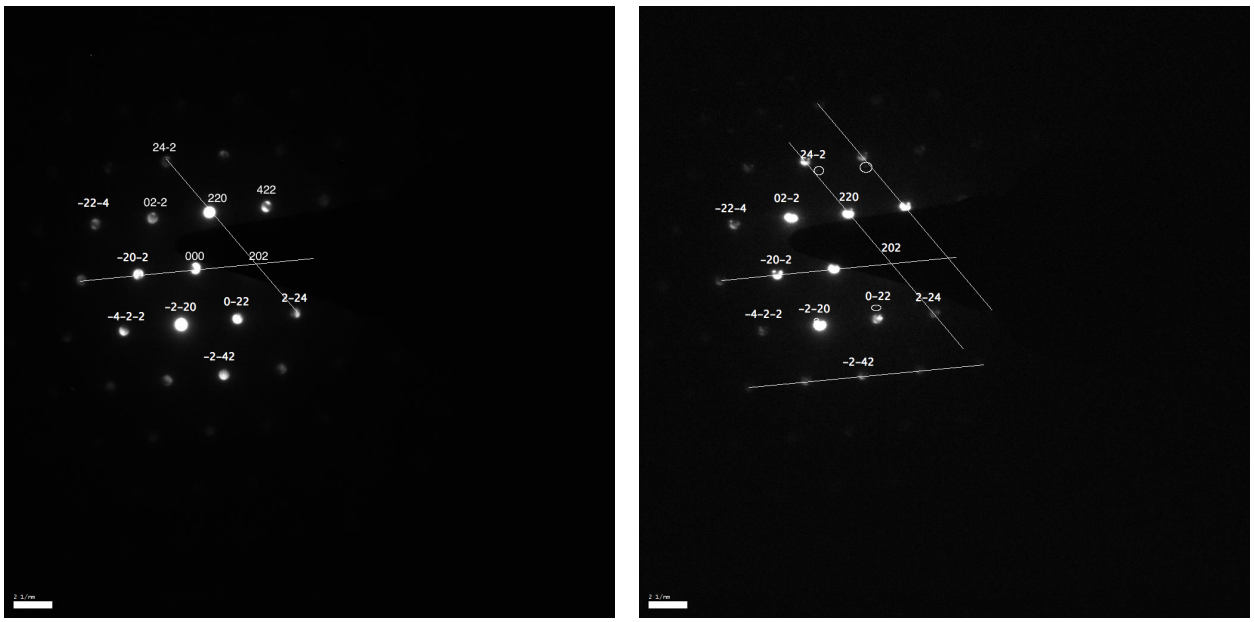


FIGURE 4.66: HRTEM IMAGE OF SAMPLE S3_17, SI(211) SUBSTRATE, 100 NM X 200 NM PATTERN, AND 10% ZN DOPING



(a) (b)

FIGURE 4.67: TEM DIFFRACTION PATTERNS FOR SAMPLE S3_17, SI(211), 100 NM X 200 NM, 10% ZN (A) FOR SI(211) AND (B) FOR CDTE

Figure 4.68 shows corresponding TEM images for Sample S3_17, the image on the left indicating the location of the HRTEM image on the right. The (24-2), (422), and (202) planes are identified for Si(211), and the (202), 02-2), and 24-2) planes are identified for CdTe. Note that the (422) orientation for the Si(211) substrate misoriented slightly from the Si pillar surface.

Table 4.10 shows a comparison of the theoretical and measured values of the angles between the (202) and the (24-2) planes for Si and the angles between the (24-2) and (202) planes for CdTe. The measured values for the CdTe planes are 5˚ off compared to the theoretical values. The selective growth for the CdTe growth on Si, without a buffer layer, has a misorientation angle of 0.2˚ for sample S3_17 in the (24-2) orientation (Fig. 4.69).

Sample S3_17, with pattern 100 nm x 200 nm, has twins in the (24-2) direction (Fig. 4.70). Twins are found to be lamellar twins. The twins switch between the (2-24) and (422) orientations. The grain size is ~53 nm and the twins travel to the surface of the grain.

CdTe growth on Si a with ZnTe buffer layer resulted in a misorientation angle of 3.5˚ [31]. The misorientation angle of 0.2˚ is an improvement over the 3.5˚ value. The misorientation angle of 0.2˚ is the smallest misorientation in this study. Twins are seen on the 100 nm by 200 nm patterned sample with 5% Zn and are along the (2-24) direction, while Zhao et al. 2011 reported twins in the (111) direction for CdTe(211)/ZnTe/Si(211) [31].

Smith et al. (2000) reported growth of CdTe(211) on Si(211) with a ZnTe buffer layer with twin growth in the (111) direction [32]. The misorientation angle ranges from 4˚ to 10˚ with a ZnTe buffer layer in this work by Smith. The angle of misorientation for sample S3_17 was misorentation of 0.2˚. Sample S3_17 has twins at the interface, but it is difficult to see how far the twins travel through the film. The diffraction pattern shown for the CdTe(211)/Si(211) planar

growth appear the closet to the 100 nm by 200 nm pattern where the CdTe diffraction spots are slightly misaligned from the Si diffraction spots reported by Smith [32].

Diaz et al. 2012 uses the CSS to selectively grow CdTe on Si(100) without a mask [29]. The CdTe grains are obereved to grow on each pillar. This is similar to the growth on sample S3_17, with a pattern of 100 nm by 200 nm. The initial growth parameters are based on this study by Diaz.

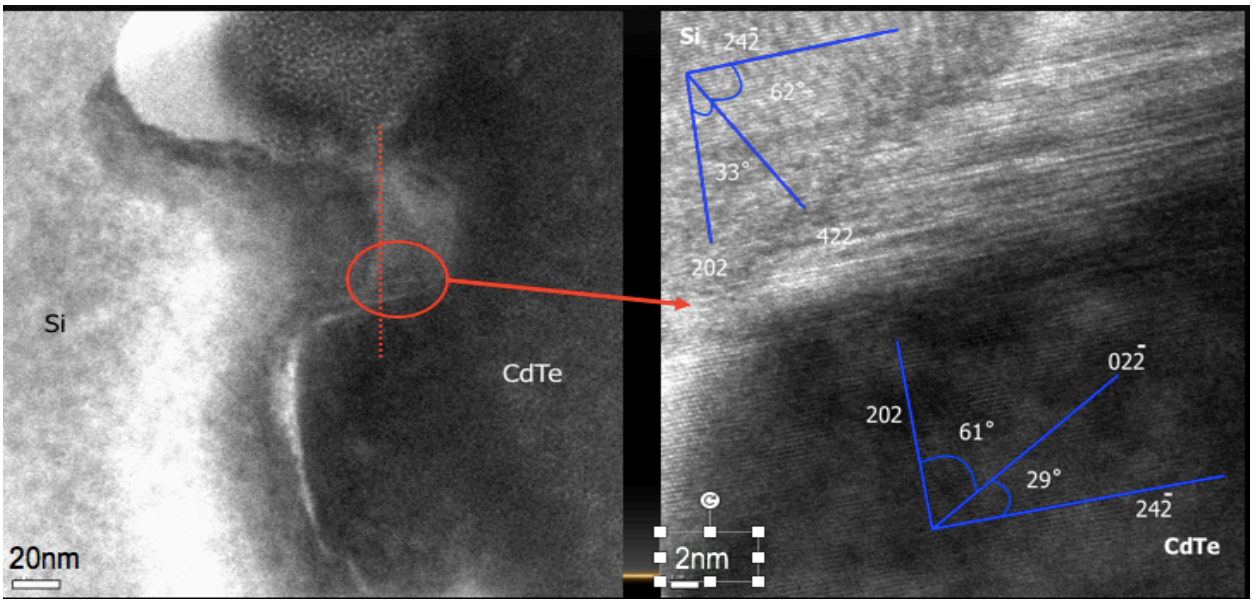


FIGURE: 4.68 HRTEM OF SAMPLE S3_17 - CDTE GROWTH ON 100 NM X 200 NM PATTERNED SI (211) WITH 10% ZN DOPING.

TABLE 4.10: MEASURED VS THEORETICAL ANGLES FOR HRTEM IMAGE FOR SAMPLE S3_17.

	Plane 1	Plane 2	Theoretical (˚)	Measured (˚)
CdTe	202	24-2	90	95
Si	202	24-2	90	90

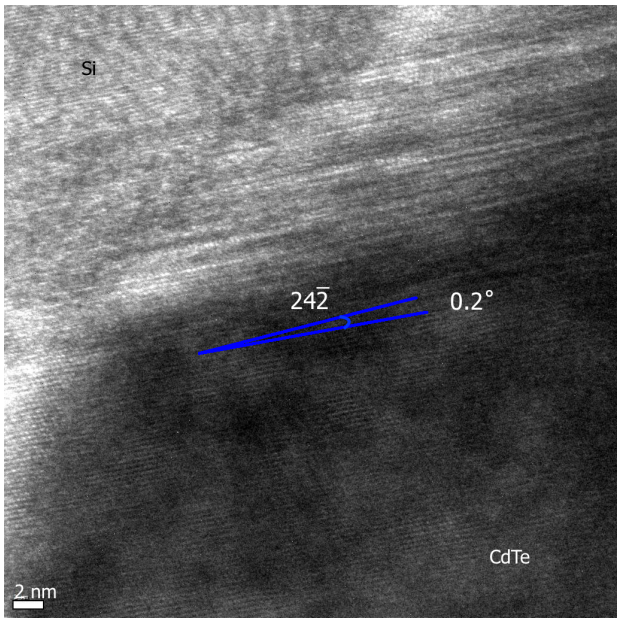


FIGURE 4.69: HRTEM OF SAMPLE S3_17 – CDTE GROWTH ON 100 NM BY 200 NM PATTERNED SI(211) WITH 10% ZN DOPING AND 1.2˚ MISORIENTATION IN THE (24-2) ORIENTATION.

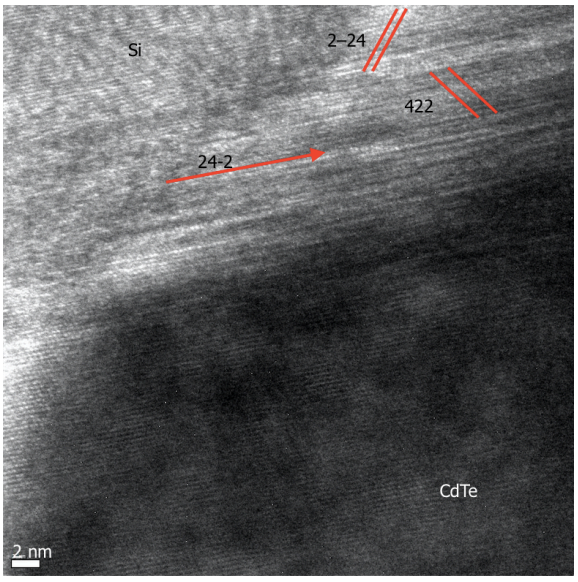


FIGURE 4.70: HRTEM OF SAMPLE S3_17 – CDTE GROWTH ON 100 NM X 200 NM PATTERNED SI(211) INTERFACE WITH TWINS IN THE (24-2) DIRECTION.

4.3.3 SET IV TEM ANALYSIS

Fig. 4.71 is a HRTEM image of sample S4_8 for CdTe growth with 10% Zn doping on a 50 nm by 100 nm patterned Si(211) substrate. The planes visible on the Si pillar represent a thin layer of CdTe in front of the 50 nm Si(211) pillar. The indexed diffraction patterns for this sample are shown in Fig 4.72 (a) for Si(211) and in Fig 4.68(b) for CdTe.

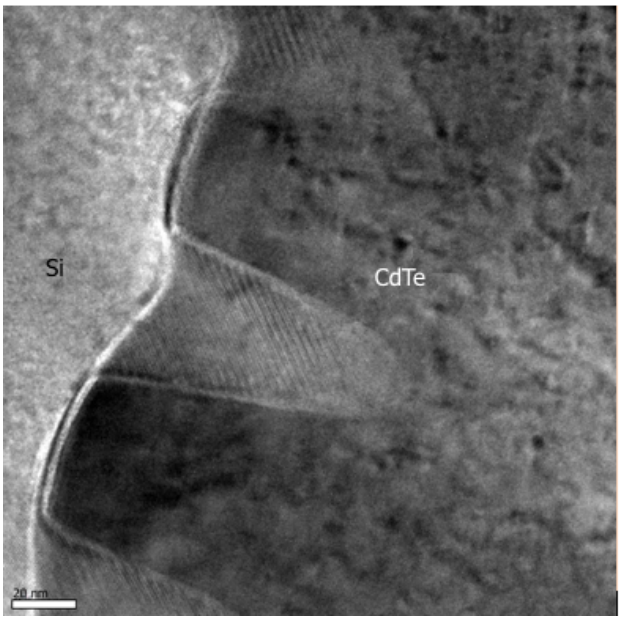
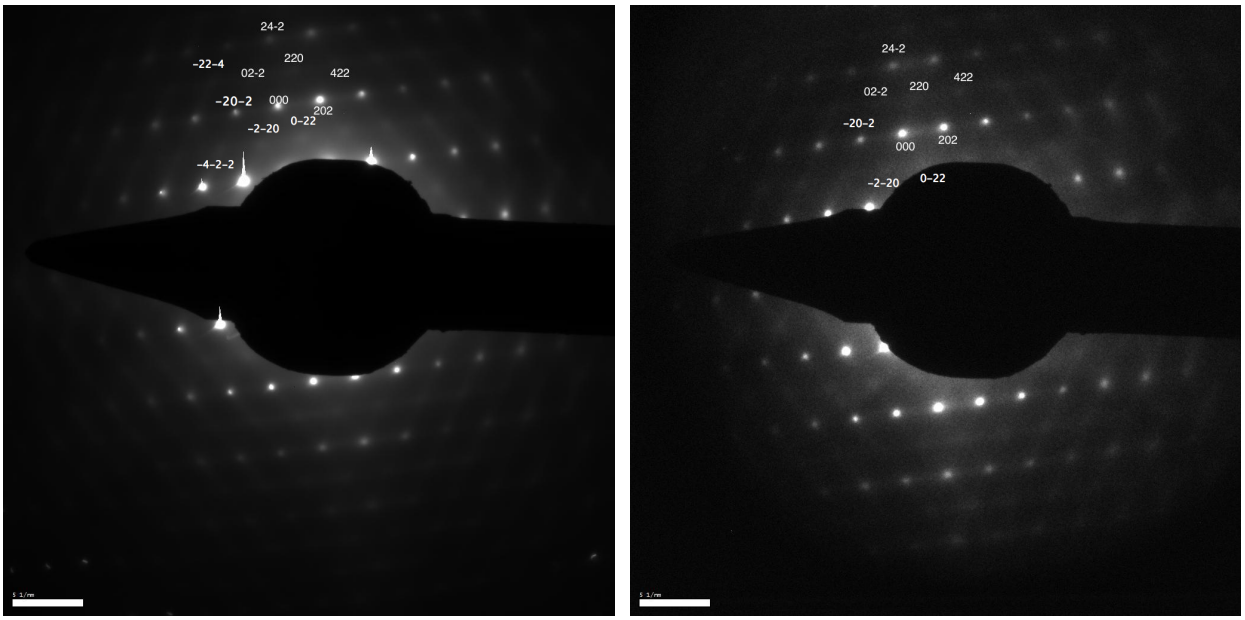


FIGURE 4.71: HRTEM IMAGE OF SAMPLE S4_8, SI(211) SUBSTRATE, 50 NM X 100 NM PATTERN, AND 10% ZN DOPING



(a) (b)

FIGURE 4.72 TEM DIFFRACTION PATTERNS FOR SAMPLE S4_8, SI(211), 50 NM X 100 NM ,10% ZN (A) FOR SI(211), AND (B) FOR CDTE

Fig. 4.73 includes two HRTEM images of Sample S4_8, where the left image indicates the location of the Si(211) pillar (on the bottom left) and on the right, the higher magnification image. The (111), (24-2), and (111) planes are identified for Si(211), and the (220), (24-2), and (202) planes are identified for CdTe, as indicated in Fig. 4.72. Table 4.11 includes the theoretical and measured values for the angles between the (111) orientation and (24-2) planes for Si, and the angles between the (202) and (220) planes for CdTe. There is close correlation between the theoretical and measured values.

A misorientation angle of 1.2˚ for sample this sample is the result of the pillar being more rounded for the 50 nm by 100 nm patterns.

Sample S4_8 with pattern 50 nm x 100 nm has a precipitate in the CdTe film away from the interface (Fig. 4.74). The precipitate is found to be 10 nm away from the CdTe/Si interface.

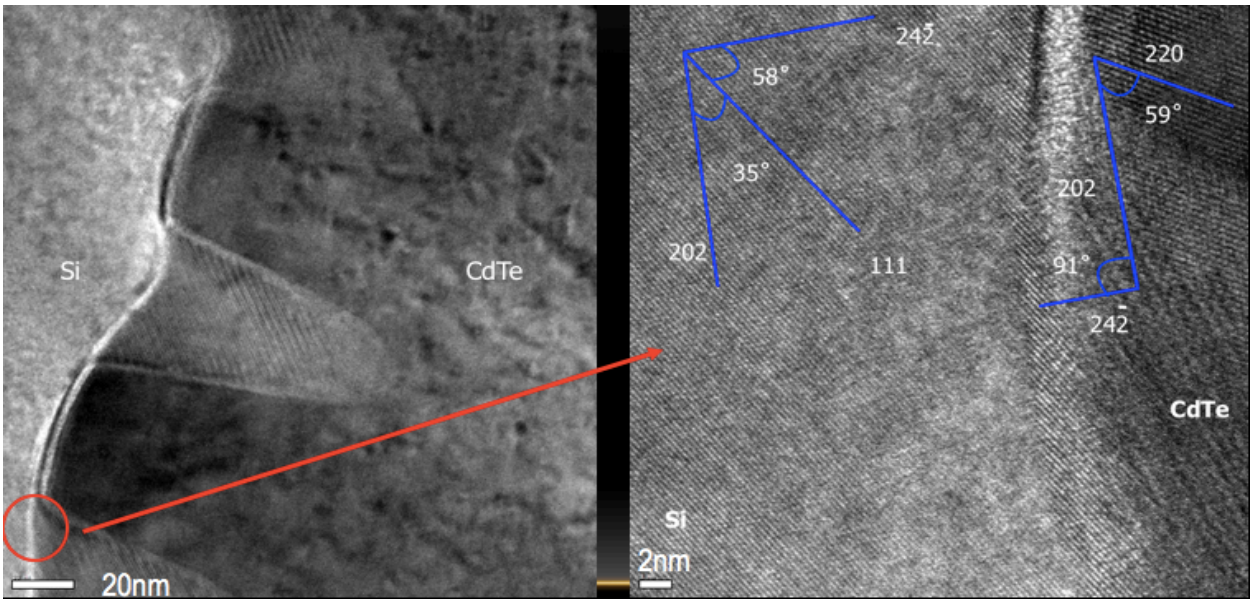


FIGURE: 4.73: HRTEM OF SAMPLE S4_8 – CDTE GROWTH ON 50 NM X 100 NM PATTERNED SI(211) WITH 10% ZN DOPING.

TABLE 4.11: MEASURED VS THEORETICAL ANGLES FOR HRTEM IMAGE FOR SAMPLE S4_8.

	Plane 1	Plane 2	Theoretical (˚)	Measured (˚)
CdTe	220	202	60	59
Si	111	24-2	60	58

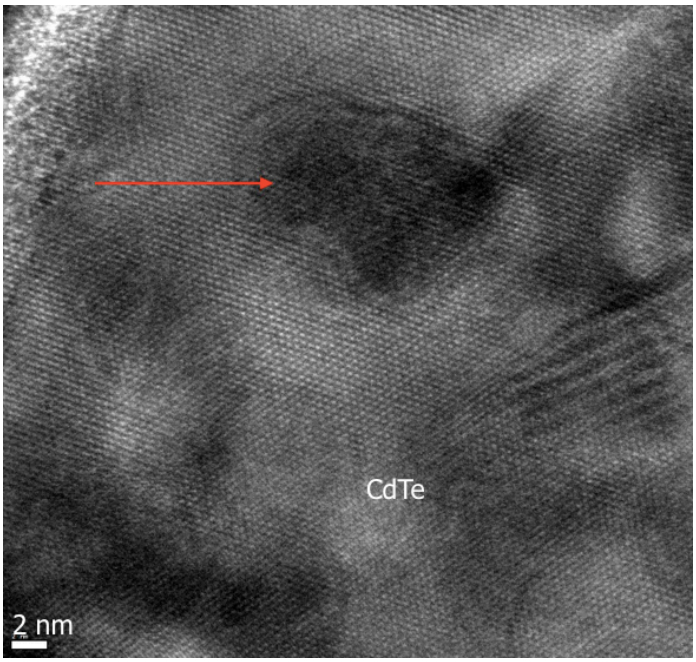


FIGURE 4.74: HRTEM OF SAMPLE S4_8 – CDTE GROWTH ON 50 NM X 100 NM PATTERNED SI(211) WITH PARTICIPATE.

4.3.4 SET V TEM ANALYSIS

The HRTEM image that highlights the selective growth for the CdTe growth with 10% Zn doping on 50 nm x 100 nm patterned Si(111) substrate is included in Fig. 4.75. The indexed diffraction patterns for this sample are included in Fig. 4.76 (a) for Si, and in Fig 4.76(b), or CdTe.

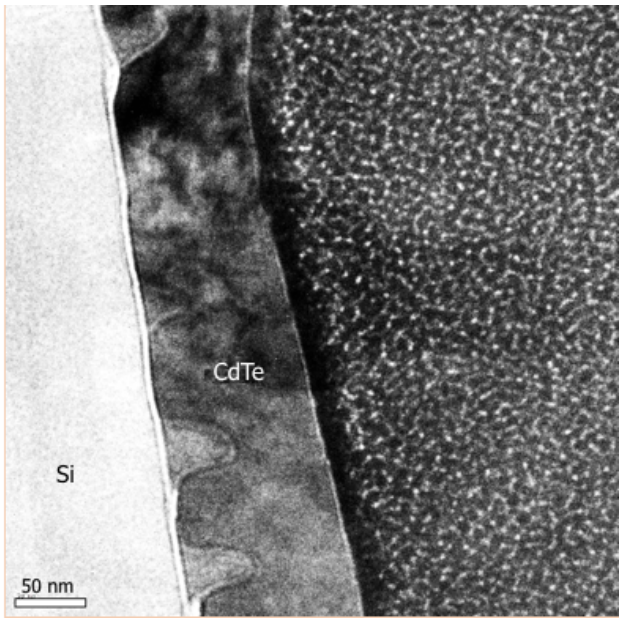
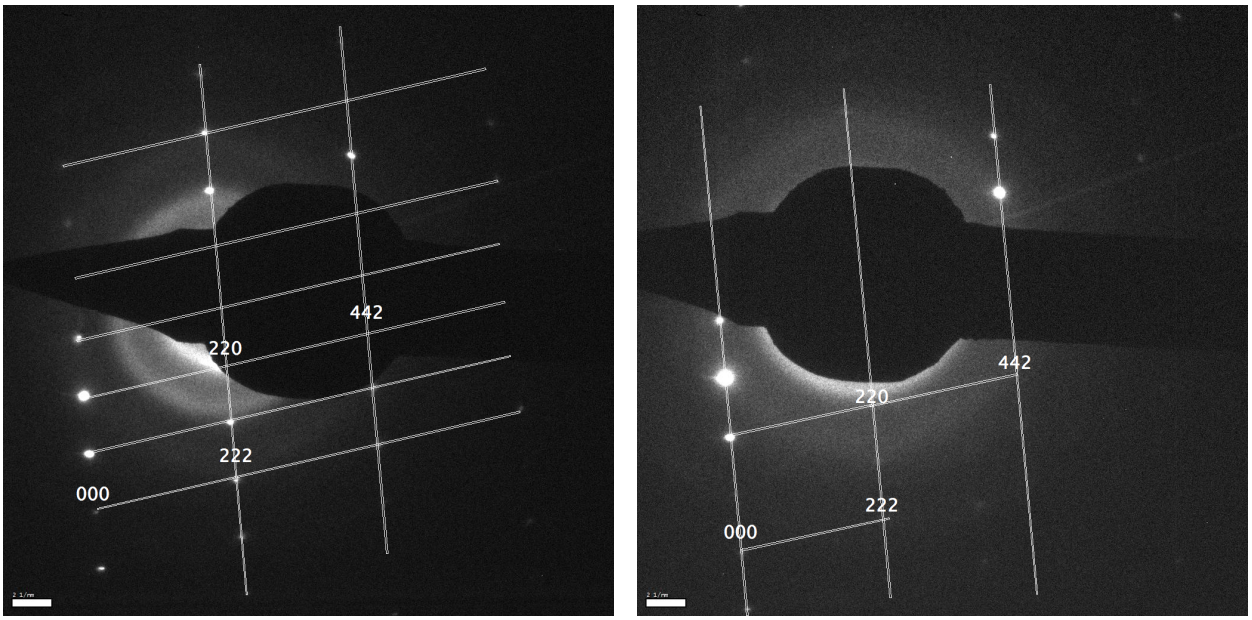


FIGURE 4.75: HRTEM IMAGE OF SAMPLE S5_2, SI(111) SUBSTRATE, 50 NM X 100 NM PATTERN, AND 10% ZN DOPING



(a) (b)

FIGURE 4.76: TEM DIFFRACTION FOR SAMPLE S5_2, SI(111), 50 NM X 100 NM, 10% ZN FOR (A) SI(111), AND (B)FOR CDTE.

The location of the indexed planes in Fig. 4.77 (right) is indicated in the TEM image on the left (bottom right side of the pillar). The indexed planes for Si and CdTe are the (222), (220), and (442) planes, as indicated by the image on the right in Figure 4.76. The (222) orientation is parallel to the Si substrate. Table 4.12 includes the theoretical and measured values for the angles between the (220) an and (222) planes for Si and for CdTe. The values are in close agreement for both materials. The selective growth for the CdTe growth on Si, without a buffer layer, has a misorientation angle of 1.2˚ for sample S5_2 in the (220) orientation (Fig. 4.78).

The selective growth for the CdTe growth on Si, without a buffer layer, has a misorientation 1.2˚. The misorientation angle of 1.2˚ is an improvement over the 3.5˚ value reported by Zhao [31]. The misorientation angle of 1.2˚ in sample S5_2 is the result of the pillar being more rounded for 50 nm by 100 nm pattern.

Zhao et. al (2011) reports that stacking faults are the most common defect for CdTe on Si(111) substrates [31]. In this work, no stacking faults are observed for CdTe grown on 50 nm x 100 nm patterned Si(111) substrate. CdTe grown on Si(111) is reposted to have a higher density of twins at the interface, and to propagate further in the film [44]. No twins are observed in the CdTe film and can be attributed to the 50 nm diameter pillars.

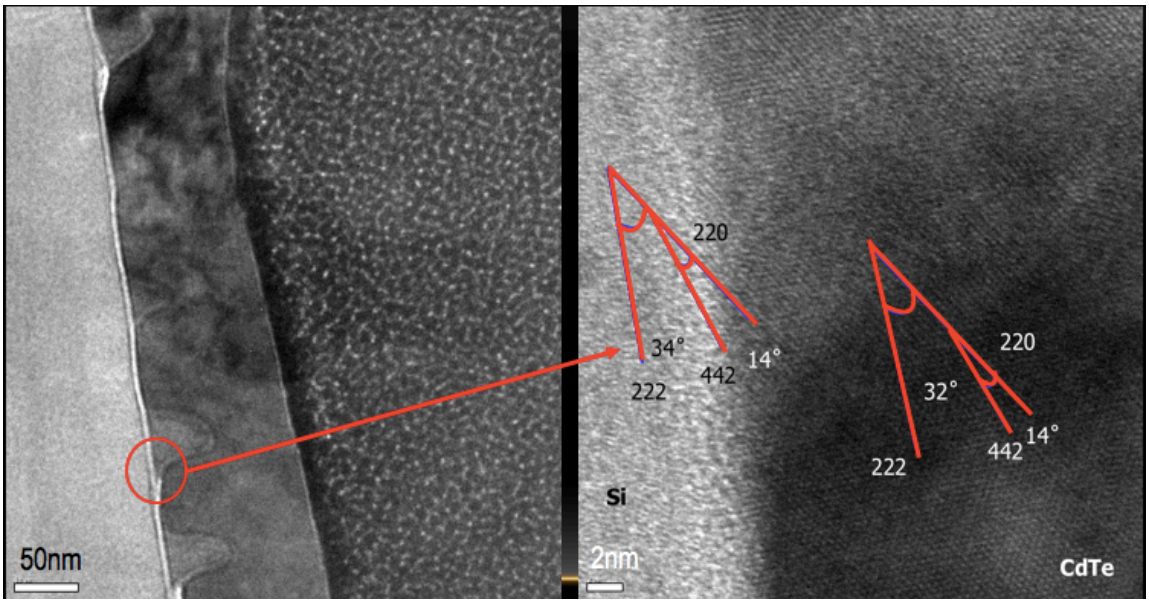


FIGURE: 4.77: HRTEM OF SAMPLE S5_2 – CDTE GROWTH ON 50 NM X 100 NM PATTERNED SI(111) WITH 10% ZN DOPING.

TABLE 4.12: MEASURED VS THEORETICAL ANGLES FOR SAMPLE S5_2.

	Plane 1	Plane 2	Theoretical (˚)	Measured (˚)
CdTe	222	220	35	32
Si	222	220	35	34

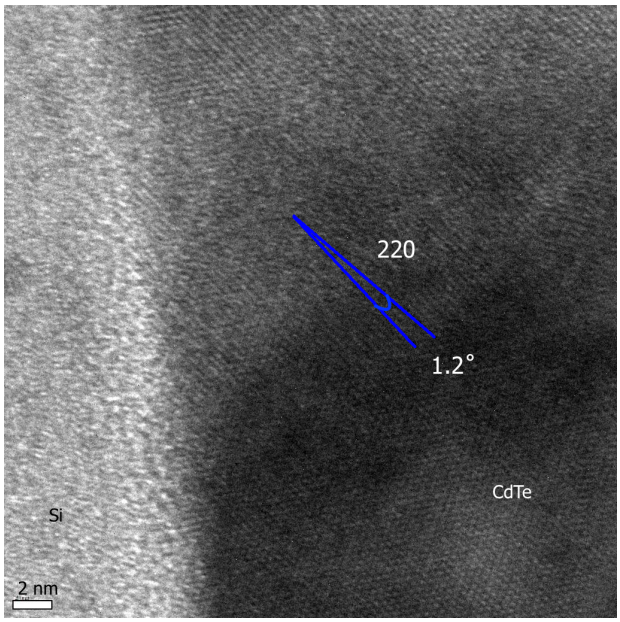


FIGURE 4.78: HRTEM OF SAMPLE S5_2 – CDTE GROWTH ON 50 NM X 100 NM PATTERNED SI(111) WITH 10% ZN DOPING, AND 1.2˚ MISORIENTATION IN THE (220) ORIENTATION.

Chapter 5: Conclusion

The sets of experiments in this work consisted of CdTe doped with 5% and 10% Zn growth on Si(211) and Si(111) substrares, with patterns ranging from 50 nm to 200 nm diameter pillars. Selective growth is achieved, but once the CdTe grain nucleates on the pillar, the grain grows around the pillar. Growth parameters for pressure, spacing of source and substrate, and gas flow are the same for all the experiments. A change in pattern required a variation in source and substrate temperatures for each set, with the exception of Set I and Set II.

5.1 Summary of Growth

Set I to Set V are performed to achieve a selective growth of CdTe on Si(211) and Si(111) using the CSS method, without a mask or buffer layer. The following can be concluded from the results:

- Selective growth is achieved for CdTe with 5% and 10% Zn doping
- The optimal source and substrate temperature is found for each Set
    - Set I and Set II: Source temperature 575˚C, Substrate temperature 485˚C
    - Set III:
        - For 5% Zn doping, Source temperature 585˚C, Substrate temperature 485˚C
        - For 10% Zn doping, Source temperature 580˚C, Substrate temperature 485˚C
    - Set IV and Set V:

    - For 5% Zn doping, Source temperature 565˚C, Substrate temperature 455˚C
    - For 10% Zn doping, Source temperature 575˚C, Substrate temperature 465˚C
- High quality CdTe is grown on Si without a mask or ZnTe buffer layer
- Large grains are grown over multiple pillars.
- Smaller grains resulted in better quality of growth, compared to larger grains.
- As the pillar diameter is decreased the misorientation of the grains is reduced.
- The smaller pitch to diameter ratio resulted in better quality of growth.
- CdTe growth with 10% Zn on 100 nm by 200 nm pattern resulted in CdTe grains on every pillar

5.2 Summary of TEM analysis

TEM analysis is used to analyze the best samples in each Set. The 200 nm by 600 nm and the 200 nm by 400 nm samples diffraction patterns are not available due to the limitations of the Cryo-TEM at UTEP. The TEM at the Microelectronics Research Center at the University of Texas at Austin, is used to analyze the atomic structure of the CdTe film, along with the interface. The diffraction pattern is used to identify the lattice planes for Si and CdTe on HRTEM images. The lattice planes are verified on the HRTEM image by confirming the angle between two planes. The misorientation angle is measured at the CdTe/Si interface. Based on this analysis the following can be concluded:

- Misorientation of the CdTe doped with 5% Zn is less than the misorientation of CdTe doped with 10%.

- The lowest misorientation measured is 0.2˚ for 100 nm by 200 nm with 5% Zn
- The largest misorientation measured is 1.2˚ for 100 nm by 200 nm with 10% Zn.
- Misorientation in this study of 1.2˚ to 0.2˚ is smaller than the misorientation of 3.5˚ with a buffer layer.
- HRTEM images are used to identify structural defects such as lamellar twins and threading dislocation.

The results presented in this dissertation demonstrate the selective growth of CdTe with 5% and 10% Zn on Si(211) and Si(111) substrates. This study shows that CdTe can be grown on Si without the use of a mask or ZnTe buffer layer. The results show that a pitch/diameter of two results in higher quality of growth compared to a pitch/diameter ratio of three. As the pillar diameter is reduced, the quality of CdTe growth is improved. In order to improve the growth on the 50 nm by 100 nm pattern, improvement of the pattern process is required to produce pillars with flat surfaces along with a more uniform pattern.

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Vita

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