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Adaptive Switched Capacitor Voltage Boost for Thermoelectric Generation

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ADAPTIVE SWITCHED CAPACITOR VOLTAGE BOOST FOR THERMOELECTRIC GENERATION

by

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THESIS

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Finally, my utmost gratitude goes to my parents for their continued support throughout my college career.

Abstract

Thermoelectric generators (TEG) and other forms of energy harvesting often provide voltages that are not directly usable by traditional electronics as levels are too low from the TEG. While increasing the number of thermoelectric elements can ultimately increase the power output, there is a tradeoff between size and power. By implementing charge pumps, a proposed circuit technique is described that can boost the TEG output to levels that can be used for energy harvesting applications. Current voltage boost circuits for TEGs simply boost a voltage by a set amount. The proposed circuit consists of an analog chip, to provide several charge pump stages as well as a dynamic latched comparator for analog to digital conversion (ADC), and a digital circuit, to control the stages of the charge pump and adaptively boost the voltage to within a specific range rather than an unchangeable, fixed multiplication. Due to the possibility that the polarity of the TEG's output voltage can reverse, dependent on environmental changes, the first charge pump stage is designed to allow for polarity switching to ensure the output is always at a positive voltage. Additionally, to improve energy efficiency, the digital controller's state machine uses constant voltage Maximum Power Point Tracking (MPPT). Finally, the digital controller can adjust the number of charge pump stages to maintain a desired output voltage range. The manner in which these features are implemented are discussed. Future work will still be necessary for ensuring maximum circuit efficiency, adjust behavior, and to ensure durability of the system.

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Chapter 1: Introduction

Interest has grown over the last few years into renewable energy. While wind and solar energy are both capable of generating large amounts of energy, research is also growing into harvesting energy from alternate sources that generate lower amounts of energy. One such form of energy harvesting is from thermoelectric generators (TEGs). Handheld TEGs generate voltages in the millivolt range with power generated in milliwatts [10]. Graphs for the voltage and power generated by a sample TEG provided by a current thermoelectric research group, TXL-Group, Inc (TXL), is shown in figures 1.1 and 1.2. These levels are below the usable threshold for most general electronics, which require several volts and such low power would be consumed quickly. With such low voltages generated, there is a need for the ability to boost the voltage. This can be achieved through the use of many different DC-to-DC which use storage elements, such as capacitors and inductors, to either increase or decrease a voltage from a power source.

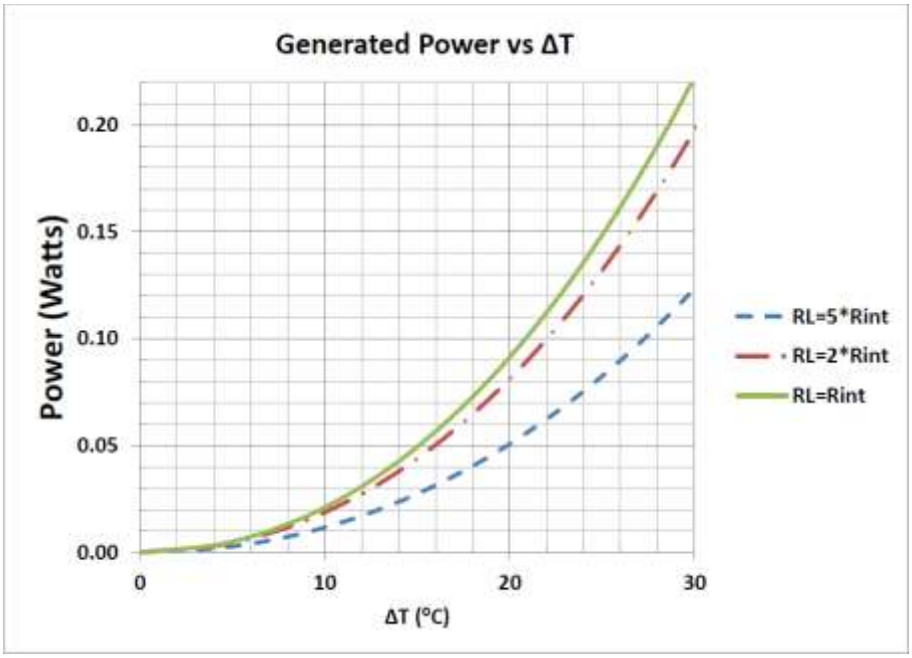

Figure 1.1 Load Power as a Function of ΔT for Three Different Load Resistances [10]

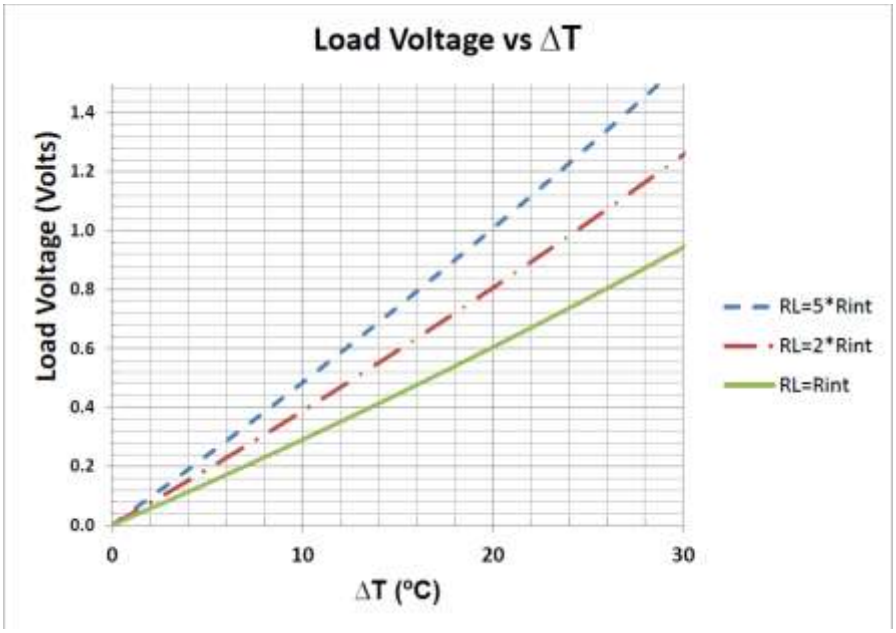

Figure 1.2 Load Voltage as a Function of ΔT for Three Different Load Resistances [10]

In this project, the focus will be on using switched capacitor charge pumps due to their high efficiency (P_{Out}/P_{In}) compared to other methods [8]. With general charge pumps, there are several problems to overcome. First, the voltage output of a TEG is dependent on the difference in temperature between the two sides of the module. This temperature difference, with one side cooled, actively or passively, and the other side exposed to the environment or a heat source, is necessary for voltage generation [9]. Over time, depending upon how the temperatures on the two sides are maintained, the temperatures will fluctuate, resulting in varying voltages. Traditional voltage boosts for TEGs proved a static multiplication factor for the TEG output. This could lead to voltages either too high or low to run a load. For our purposes, we assume the load will be a battery being charged by our system. Too little voltage and we won't properly charge. Too much voltage results in excess heat that could damage the circuit or battery. Therefore, we need a system that can adaptively adjust the charge pump's multiplication factor based upon the input voltage.

Additionally, a TEG can change polarity over time. Voltage is generated by the transfer of heat between the two sides of the module through individual elements of p and n-type materials,

usually doped bismuth telluride (Bi2Te3) for room temperature range applications [5]. These elements are arranged in thermal parallel and electrical series [2]. When heat is transferred in one direction, a positive voltage is generated. If the transfer of heat reverses, the polarity of the output voltage reverses as well. This leads to a problem with any system used to increase the output of a TEG. If the polarity switches, the system will act as a drain rather than a charging source. This means that the system must be capable of identifying a shift in polarity and adjusting the output to maintain a positive voltage at the output.

A final problem that needs to be addressed with any TEG charge pump is output power efficiency. Treating the TEG as a non-ideal power source, the obvious assumption would be that the load impedance of the charge pump circuit would have to be equal to the internal resistance of the TEG in order to achieve maximum power transfer to the load. However, research has shown that maximum power can be achieved by maintaining the operating voltage at half the open circuit voltage (V¬OC) [11]. With this approach, VOC must be measured and the output voltage is maintained at approximately half VOC to obtain maximum power at the output. This approach would also allow the charge pump to be usable by different TEGs since different TEG designs can have internal resistances ranging between 1-10 Ω that varies with temperature [9]. Since the maximum output power isn't dependent on impedance matching, the design wouldn't be limited to a single TEG model.

Taking these conditions in mind, an ideal charge pump would have to achieve three goals. First, the charge pump would need to contain several multiplication stages in order to maintain the output voltage within a range to avoid situations where the charge pump over or undercharges the load. Such a setup would require the ability to mix and match the number of multiplication stages in order to meet the specified range. Second, the charge pump must be capable of detecting a polarity switch within the TEG. For example, one current energy harvesting application being tested by TXL is the use of TEGs to power LEDs for speed humps. The LEDs used only light up

for a short time and require low amounts of energy, so the power generated by the TEG is sufficient when allowed to charge a storage device throughout the day. The TEG module is placed with the top side of the module exposed to the surface of road, while the bottom side is connected to a subsurface heatsink. While the subsurface temperatures tend to stay constant, the surface temperatures will vary throughout the day. During the day time, a voltage with one polarity can be generated as the heat from the hotter surface travels from the top of the module to the heatsink cooled bottom. As night time falls and time passes, it is possible that surface temperatures fall below the temperature of the subsurface, causing the output voltage to switch polarity as the bottom side of the module is now hotter than the side exposed to the surface. For such an application, the circuit would need to be capable of being reconfigured to maintain a positive output at the load. Third, to maintain maximum output power, the charge pump would require a system for maximum power point tracking. The output needs to be adjustable to half VOC in order to meet this requirement.

For a handheld TEG, the size of the charge pump system would have to be similarly sized (demonstration model provided by TXL measured 30mm x 30 mm) to avoid creating a bulky system. In addition to requiring a hot side, the modules will often require some system in place to remove heat from the cool side of the TEG to ensure there is a proper temperature gradient between the two sides of the TEG. Adding a bulky charge pump circuit would limit the places in which the TEG system could be deployed. The current design implements the use of separate chips for the analog and digital circuits, but future designs will integrate both circuits into a single chip.

Chapter 2: Background

This goal of this project was to create an adaptive charge pump system to meet the needs of a TEG. The system will be designed to meet a specification set determined by TXL. These specifications indicate that the charge pump must be able to deal with an input V_{OC} ranging from 50 mV to 250 mV from the TEG as well as a range of 1 Ω to 10 Ω for the TEG module's internal resistance. The system will output a voltage between 3 and 5 volts to a resistive load or a rechargeable cell, with 3.3 volts used as a target. Power out vs power in (P_{out}/P_{in}) will be targeted at 70%.

2.1 THERMOELECTRICS

TEs are commonly used for two main purposes. When provided with a power source as shown in Figure 2.1 (A), the current flow causes the electrons in the n-type material and holes in the p-type material to conduct towards the base of the structure [2]. The flow of the carriers, in an effect known as Peltier effect, conducts heat in the direction of flow based upon the material type. This cools the top of the module. The amount of heat dissipation is a factor of the current flowing through the elements and the Peltier coefficients of the materials.

When used as a power source, as in Figure 2.1 (B), the heat transfer between the hotter top junction and cooler base causes electrons and holes from the n-type and p-type materials, respectively, to flow towards the bases, causing a voltage difference [2]. As a counterpart to the Peltier Effect, the Seebeck effect describes this phenomenon. Similar to the Peltier Effect, the amount of electricity generated is a factor of the temperature gradient and Seebeck coefficient.

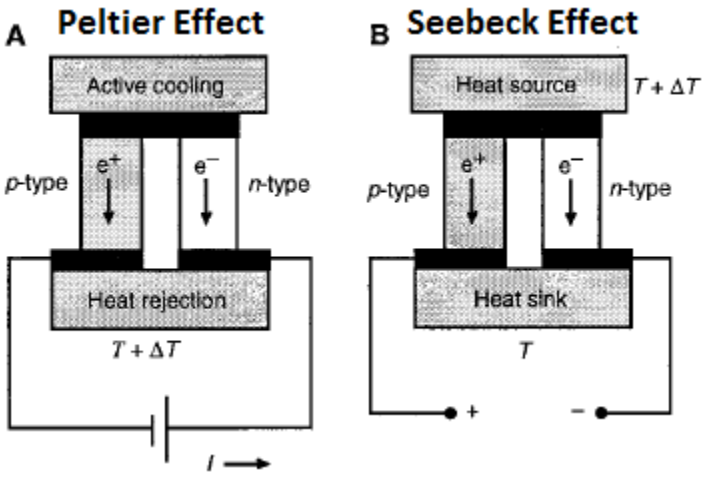

Figure 2.1 (A) Peltier Heat Pump (B) Thermoelectric Generator [2]

This interaction is the basis for TEGs. Figure 2.1 shows a single thermocouple system. Typical TEGs are designed with multiple thermocouples to increase the generated output voltage. One common arrangement is a vertical/vertical-type configuration in which the thermocouples are arranged vertically and connected in thermal parallel and electrical series as shown in Figure 2.2 [4].

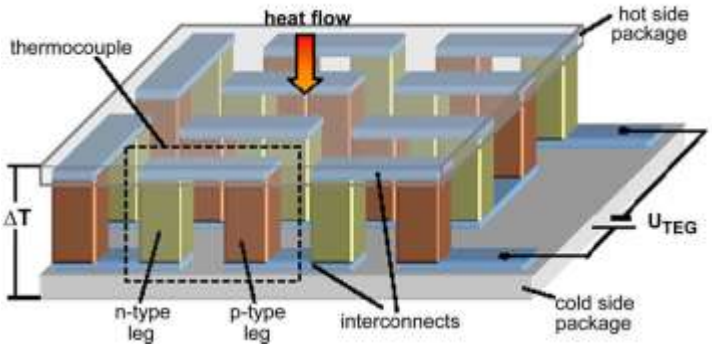

Figure 2.2 Vertical/vertical-type Thermoelectric Generator [4]

The TEG used for this project consisted of 127 thermocouples (254 thermoelements), each providing approximately 200 μV/°C [10]. The formula for determining V_{OC} is given by [10]:

$$V_{OC} = N * (0.0002 * 1.004^{\Delta T}) * \Delta T \quad (2.1)$$

Where N is 254 (127 thermocouples * 2) and ΔT is the temperature difference between the hot and cold side of the TEG. Accordingly, the higher the temperature difference between the hot and cold side, the larger the output voltage.

However, high temperature differences require a system to maintain a cold side. For TEGs used in energy harvesting, any type of active cooling would cost more in energy consumed than would be generated by a TEG. Therefore, smaller temperature differences would be expected. As such, the voltage output can be expected to be in the mV range and would need a system to boost this output in order to generate a usable output.

Currently, bismuth telluride is the material of choice for TEGs for applications near room temperature and with doping allowing for better performance at higher temperatures [5]. The creation of p-type and n-type material for various temperature ranges can be achieved through doping with antimony being a common dopant. Additionally, the control of the ratio of bismuth, telluride, and antimony in the alloy can have effects on the material's properties.

2.2 Switched Capacitance Charge Pump

In order to increase the output from the TEG, a voltage boost will be needed. The type of DC-DC converter to be used depends on the application. For this project, switched capacitor charge pumps were chosen for their high efficiency ratios [8]. Additionally, for simplicity, a switched capacitor design was chosen in order to minimize the number of transistors used in the charge pump section to reduce the circuit's $R_{DS(on)}$ and maximize efficiency.

The basic concept of a switched capacitor charge pump lies in switching a set of capacitors between parallel and series in charge and discharge stages. An example of a voltage doubler is shown in Figure 2.3 (A). When both switches are in position 0, both capacitors, C1 and C2, are in parallel and charge to V_{OC} as shown in Figure 2.3 (B). At this point, the load is not connected to

the circuit. When the switches are placed in position 1, then the capacitors are placed in series and the load is placed in parallel with both series capacitors as shown in Figure 2.3 (C). When in this configuration, the output is boosted to $2*V_{OC}$. In the case of a capacitive load, the two series capacitors (C1 and C2) are drained to charge the output capacitor until the output capacitor is at the same voltage as the two series capacitors. To get a full $2*V_{OC}$, successive parallel/series cycles are necessary.

Switched capacitance charge pumps can achieve various voltage multiplications by adding additional capacitors, but the circuit designs become increasingly more complex. Chaining various multiplication stages will allow for larger output voltages for low voltage TEG applications. Similar parallel/series switching can also create voltage dividers by charging a number of capacitors in series to one voltage, then switching all the capacitors to parallel with the load in parallel as well.

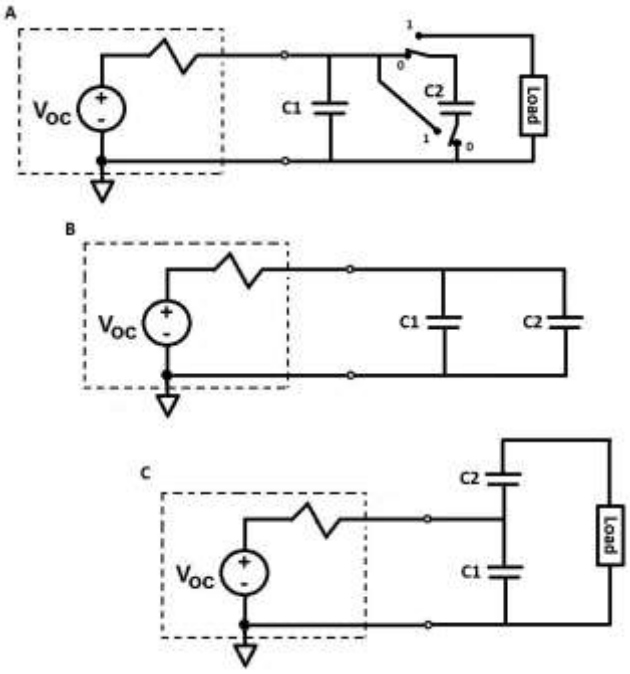

Figure 2.3 (A) Switched Capacitance Voltage Doubler (B) Switches in position 0 (C) Switches in position 1

2.3 Analog to Digital Converter Design

In order to determine the number of multiplication stages necessary to maintain the output voltage within the desired range, as well as for optimization purposes, the digital controller needs a way to measure the TEG's output voltage. For this, a simple ADC is used to provide a usable, low resolution digital signal for the digital controller. The needs of this system do not require a highly accurate or high speed ADC, so a simple design will be implemented as shown in Figure 2.4.

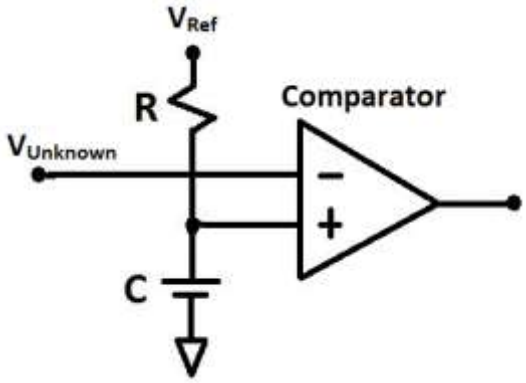

Figure 2.4 Analog to Digital Converter

The RC circuit connected to the reference voltage (V_{Ref}), with known resistor and capacitor values, charge the capacitor connected to the positive terminal of the comparator at a known rate given by [1]:

$$V_C(t) = V_{Ref}(1 - e^{-t/RC}) \qquad (2.2)$$

The output of the comparator is connected to a counter in the digital controller. The digital controller provides V_{Ref}. The ADC counter starts counting when V_{Ref} is set high and finishes counting when the output from the comparator is a logical 1. Using equation 2.2, the counter value now represents the approximate value of the unknown voltage ($V_{Unknown}$). The accuracy of the

approximate value is determined by the frequency and size of the counter as well as comparator design.

The behavior of the ADC for the project will be that of a zero-order hold sampling [6]. In this type of ADC, the value of the analog signal is captured at the instant of sampling and held until the signal is to be sampled again. Instead of a constant rate sampling though, the ADC will only be sampled at specific times at which the value of $V_{Unknown}$ is needed.

2.3.1 Comparator Design

Several designs for the comparator were considered. A simple CMOS dynamic latched comparator was used because it exhibited the necessary zero-order hold behavior as well as being transistor based without the need for capacitors or resistors. This will minimize layout size and inputs/outputs necessary for discrete elements. Additionally, latched comparators provide positive feedback for regenerative amplification [3]. This leads to a faster output and better power efficiency when compared to a design with multi-stage linear amplification. The design for a basic dynamic latched comparator is shown in Figure 2.5.

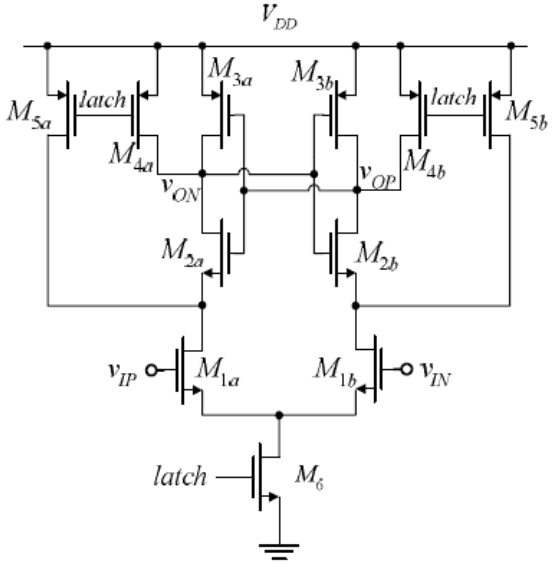

Figure 2.5 Dynamic Latched Comparator [3]

In this case, the latch signal is the controlling signal for the comparator. When low, reset transistor pairs M_{4a}/M_{4b} and M_{5a}/M_{5b} are in the closed state and set the output nodes V_{ON} and V_{OP} to V_{DD}. The differential pair transistors, M_{1a} and M_{1b}, have V_{DD} at their drains, but are disconnected from ground by M_6 which is open, so no current flows. When latch is high, the reset transistor pairs are open and the inverters formed by M_{2a}/M_{3a} and M_{2b}/M_{3b} enter a regeneration phase where the differential pair transistor with a higher input voltage receives more current that sets the appropriate output, V_{ON} or V_{OP}, to full V_{DD} and the other is set to ground. This condition is held for as long as the latch signal remains high [3].

2.4 Maximum Power Point Transfer

Due to the low power output of the TEG, maximum power output from the voltage pump circuit is desired. Figure 2.6 shows the equivalent model of the TEG when connected to a load resistance [9].

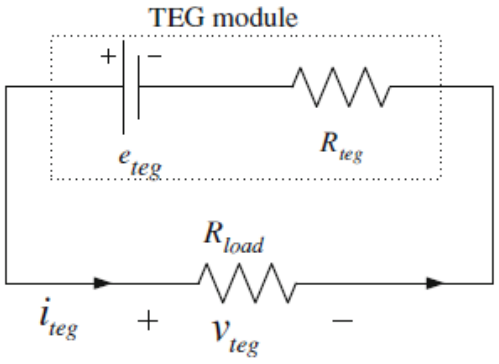

Figure 2.6 TEG Equivalent Model [9]

Traditional thinking would imply maximum power output is obtained when the load resistance is equal to the internal resistance of the TEG (R_{teg}). However, the internal resistance of the TEG is highly temperature dependent as shown in equation (2.3) [9]:

$$R_{teg} = \int_0^l \frac{\rho_p(T_p(x))}{S_p} dx + \int_0^l \frac{\rho_n(T_n(x))}{S_n} dx \qquad (2.3)$$

Additionally, previous studies have shown that impedance-matching does not yield maximum power output [11]. However, using constant voltage MPPT, maximum power output can still be obtained by maintaining the operating voltage at half of V_{OC}.

Chapter 3: Methodology

This chapter discusses the design challenges and choices taken with consideration to the project goal being an adaptive charge pump capable of increasing the output from a TEG to within a selected range while maintaining maximum output power.

3.1 Analog Circuit Design

3.1.1 Multistage Voltage Boost

As discussed previously, in order to obtain the desired voltage range of 3-5 volts, a number of voltage multiplying charge pumps will be used. For our purposes, four cascaded multiplication stages will be used with the ability to bypass two of the stages. Figure 3.1 shows a black box representation of the suggested system. For all stages, switches are implemented in CMOS with transmission gates. Single pole, double throw switches use two transmission gates with reversed enable signals while single pole, single throw switches use a single transmission gate with the enable configured depending on whether or not the switch is to be normally open or normally closed.

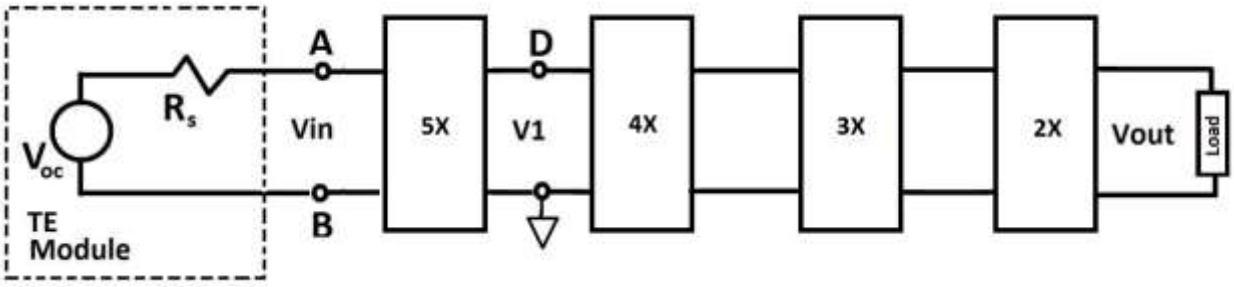

Figure 3.1 Multistage Voltage Boost

With this setup, the maximum output multiplication is 120X. This will allow the charge pump system to charge a minimum voltage of 25 mV to the desired 3 V. As shown in Figure 3.1,

every input voltage will be multiplied by 120. However, this isn't always necessary. With higher input voltages, it will be necessary to bypass one or more stages in order to hit the target voltage range. However, the 5X stage will be maintained in every situation since, as will be discussed later, it will provide the input to the ADC through node D (as shown in Figure 3.1) and will be designed in order to allow for polarity switching. This would mean, in order to maintain the 3-5 V range, the maximum input voltage would be 1 V.

Additionally, the 2X stage is no longer bypassed due to issues with high side switching when the output voltage approached V_{DD}. To avoid this problem, when using transmission gates for high side switching, the gate voltage would need to be increased beyond the applied V_{DD} [6]. This would require a bootstrap circuit using an additional capacitor and transistor. Instead of this approach, a low side switch design was implemented for the 2X stage with low threshold voltage Schottky diodes replacing the switches on the high side. Due to this, in order to achieve output voltages greater than $V_{DD} - V_{TH}$, the 2X stage is not bypassed. Unfortunately, this means the output voltage range has expanded to 3-10 V.

3.1.2 Multiplication Stage Designs

The requirements for the different charge pumps led to separate designs for the various multiplication stages to be discussed.

The 5X stage is not only responsible for the initial multiplication from the TEG, it also has to have a reconfigurable output to allow for polarity switching should the output from the TEG turn negative. Such a situation was discussed in the introduction when using a TEG with one side exposed to the surface of a road and the bottom side thermally connected to a heatsink buried below the surface. The design for an output reconfigurable switch capacitance 5X charge pump is shown in Figure 3.2.

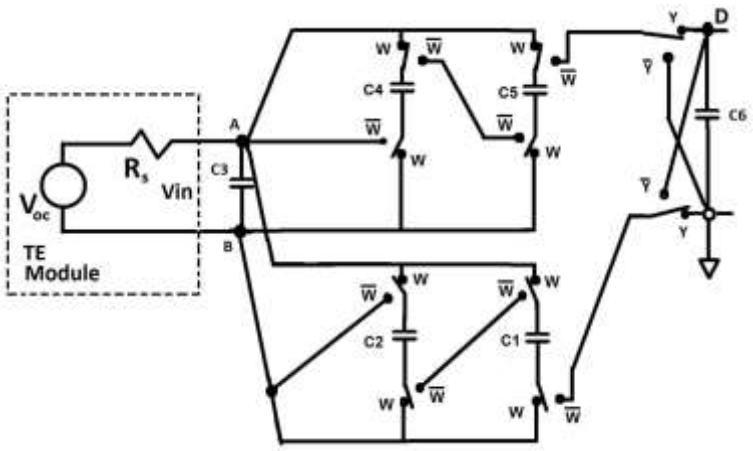

Figure 3.2 5X Multiplication Stage

Signal W is the series/parallel signal generated by the digital controller. In the state shown in Figure 3.2, W is high and output capacitor C6 is disconnected from the circuit. Capacitors C1-C5 are in parallel and are all charged to V_{in}. When W is set low, capacitors C1-C5 are placed in series, with the series combination placed in parallel with output capacitor C6. Furthermore, control signal Y (also from the digital controller) is capable of switching the configuration of the output capacitor to maintain a positive output.

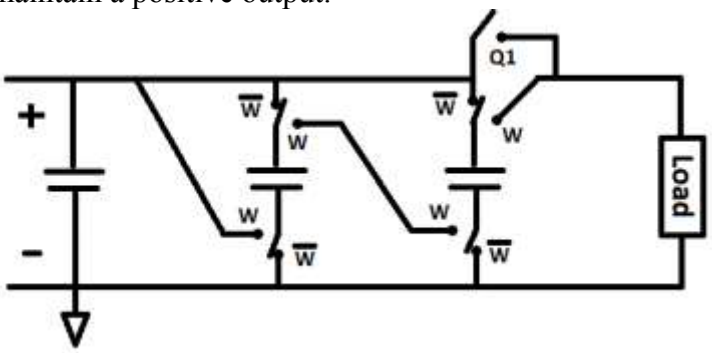

Figure 3.3 3X Multiplication Stage

Figure 3.3 shows the schematic for the 3X stage. The 4X stage is similarly designed with an extra capacitor. Thanks to the 5X stage, the input voltage polarity to the stage is always positive, so there is no need for the output to be reconfigurable. However, the 3X and 4X stages have an

additional controlling signal, Q1 for the 3X stage and Q for the 4X stage. Each signal bypasses the respective stage as well as sets W to zero (not shown) to prevent the series/parallel switching of the stage and maintain a parallel configuration while the stage is bypassed. The input is still connected to the output, but with the bypassed stage simply appearing as a large capacitor to the stages before and after.

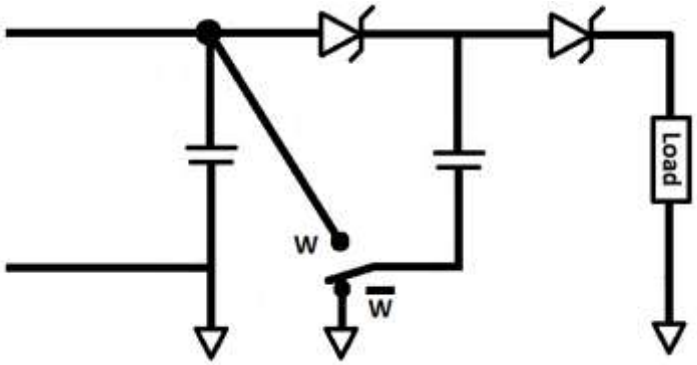

Figure 3.4 2X Multiplication Stage with Low Side switching

The initial design of the analog system used a 2X multiplication design similar to Figure 2.3 (A) with the same bypass switch employed in the 4X and 3X stages. However, after fabrication and testing, it was shown that the design was limited in output voltage due to issues with the switches turning off when the V_{DS} through the transistors grew too large. This limited the output to approximately 2.6 V with a 3.3 V V_{DD}. To avoid this situation, the low side schematic shown in Figure 3.4 was implemented. Since the switch is now on the ground side, excess voltage is no longer an issue. After the change, the 2X stage was no longer bypassable in order to allow for output voltages above 2.6 V, even when the 2X stage would normally have been bypassed.

3.1.3 Comparator Design

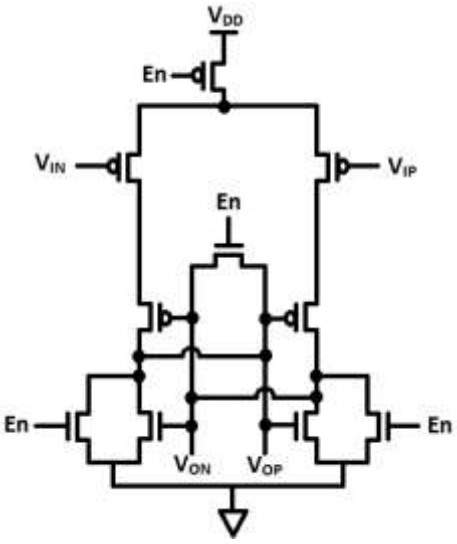

Figure 3.5 Inverted Dynamic Latched Comparator

Figure 3.5 shows the schematic for the dynamic latched comparator used. The operation of the comparator is similar to the design shown in Figure 2.5 with a few key differences. The design is inverted and negatively enabled. This ensures that, when the enable signal is set high, both inverters are coupled together and connected to ground. This gives an output of zero out of both V_{ON} and V_{OP} when the comparator isn't sampling. The output is sampled on the falling edge of the enable signal and the input voltage with the highest voltage sets the appropriate output high. Both outputs remain latched while the enable signal remains low. The inputs will be connected similar to Figure 2.4 where V_{IP} will come from the RC circuit (V_{Ref} from the digital controller) and V_{IN} will come from the output of the 5X stage (Node D in Figures 3.1 and 3.2).

3.1.4 Capacitor and Transistor Sizes

The stage capacitors were chosen to mirror a step down approximate to the multiplication of the stage. Capacitor values were also chosen based on standard values. The 5X stage capacitors were set at 10 μF. Capacitors for the 4X stage were chosen to be approximately $1/5^{th}$ the size of

the 5X stage capacitors. Thus, 2.2 µF capacitors were used. The 3X capacitors were chosen to be approximately 1/4th the size of the 4X capacitors at .47 µF. Furthermore, the 2X capacitors are 168 nF.

Similarly, the transistor sizes are reduced by equivalent divisions. The 5X stage has 400 µm PMOS transistors and 200 µm NMOS transistors, the 4X stage has 100 µm/50 µm PMOS/NMOS transistors, the 3X stage has 32 µm/16 µm PMOS/NMOS transistors, and the 2X stage has 16 µm/8 µm PMOS/NMOS transistors. The comparator transistors were all sized to 8 µm.

These sizes were chosen on a trial basis. Proper sizing analysis will be part of continued design research in this project.

3.2 DIGITAL CIRCUIT DESIGN

The block diagram for the digital circuit is shown in Figure 3.6.

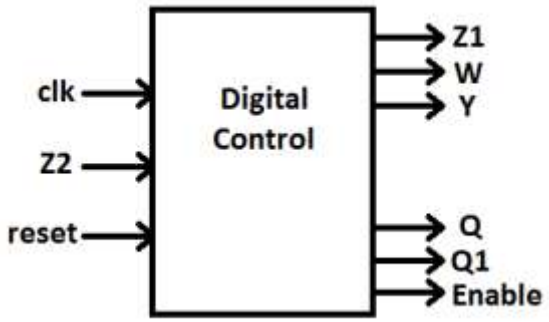

Figure 3.6 Digital Controller Block Diagram

Inputs:

clk and reset – externally generated

Z2 – Input from positive comparator output (V_{ON})

Outputs:

Z1 – Reference voltage to RC circuit of the ADC

W – Parallel/Series switch signal (0 – Series, 1 – Parallel)

Y – 5X stage polarity switch signal

Q, Q1 – Bypass signal for the 4X and 3X stages, respectively

Enable – Comparator enable signal

3.2.1 Timing

A key component of the digital logic is based around timing and counters. The input clock is set at 100 KHz. With a 100 KHz clock, the timing for the ADC is determined by the necessary resolution/accuracy. Taking into consideration the fact that the voltages out of the 5X stage will generally range between 250 mV and 1 V (5 * the estimated TEG output range of 50 mV to 250 mV) the resolution for the ADC can be relatively small. Also, knowing the maximum expected output is 1 V, and building a bit of extra room for possibly higher output values, the charging of the RC circuit input to the comparator can be cut short, since V_{Ref} will be set at 3.3V. With this in mind, the maximum count for the ADC was set to 50 clock cycles. The enable signal will be an inverted version of the clock during enable phases. If the RC circuit time constant is set at 1 ms, 50 clock cycles (500 μs) will ensure a voltage at the capacitor of 1.298 V according to equation 2.2. Thus, the ADC's RC circuit will require a .1 μF capacitor and a 10 kΩ resistor (both standard values).

As for the signal W, the comparator requires the capacitors to be maintained in one state or the other while sampling to get an accurate voltage and fifty clock cycles are required for a maximum ADC count. Since a full period consists of one full series cycle and one full parallel cycle, then the smallest time period for series/parallel switching is 1 ms. Using the 100 KHz master clock, a 1 KHz clock will be derived as the timer for W switching.

Finally, since the TEG output will remain relatively stable over moderate lengths of time, adjustments to the system can be done over longer stretches of time. Due to this, the state machine

for the digital controller is spread over a 10 s time period with major phases occurring once every second.

3.2.2 State Machine

The state machine is split into phases based upon even and odd seconds (0 s - 9 s), and added behavior in seconds zero and five. For second zero, the first 50 ms are spent charging the 5X stage output capacitor to a full $5*V_{OC}$. The switching frequency for W is set to 10 KHz during this phase to aid charging to $5*V_{OC}$. After 50 ms, the voltage is sampled and saved. This saved voltage is used to determine whether or not the 4X and 3X stages are to be bypassed, as shown in Table 1, and for later duty cycle adjustments. Then the ADC capacitor is allowed to discharge until, approximately, the half second mark. After fully discharging, the comparator is once again enabled for polarity sensing and Z1 kept low. This allows for the ADC to be used for polarity sensing. With the ADC capacitor fully discharged, the positive input (V_{IP}) to the comparator is zero, and a high output from the comparator indicates a negative voltage at the negative input to the comparator (V_{IN}). Signal Y is then set either high or low based upon the result of the polarity sensing phase (low if the output is positive, high if the output is negative). After the polarity is set, the state machine switches to the even second phase for the last half second. Second five follows the same pattern as second zero, but the state machine switches to the odd second phase after polarity sensing.

For the last half of the zero second and every even second, the state machine adjusts the number of clock cycles for which W is set low (series). The default duty cycle for W is 50% with 32 clock cycles high (parallel) and 32 clock cycles low (series) based off the 1 KHz clock. During the even second phase, the state machine waits until the first instance of the W signal reaching the final clock cycle in which it is low. This means 500 µs before the signal switches from low to high. For instance, if the low cycle count is set to 32, then the state machine waits until the first instance of the low cycle count reaching 31. During the final clock cycle, the ADC is enabled for sampling

to measure the voltage during this discharge phase. If the minimum voltage is greater than approximately 45% of $5V_{OC}$, then the duty cycle is adjusted by increasing the number of 1 KHz clock cycles W spends in series by one. If the voltage is less, then the number of series clock cycles is decreased by one. If it is the same, then the number of cycles stays the same. This test and adjustment only occurs once during the even second phase.

Similarly, for the odd second phase, the state machine waits until W is 500 μs away from switching from high to low. When the state reaches this point, the ADC is enabled for sampling and the voltage is saved for this charging phase. If the voltage is greater than approximately 55% of $5V_{OC}$, then the duty cycle is adjusted by reducing the number of clock cycles spent in parallel. If the voltage is less, then the number of clock cycles is increased by one. Otherwise, the duty cycle remains unadjusted. Both even and odd phases are designed to maintain an approximately 50% operating voltage for MPPT.

The logic for shorting the 4X and 3X stages, Table 3.1 shows the voltages multiplications necessary at the estimated voltage ranges.

Table 3.1 Voltage Multiplication Ranges

Voltage at Node D	Multiplication	Shorted Stage(s)	Output Voltage
$V_D > 1.65$	2	4X, 3X	$V_{Out} > 3.3$
$0.55 < V_D < 1.65$	6	4X	$3.3 < V_{Out} < 9.9$
$0.4125 < V_D < 0.55$	8	3X	$3.3 < V_{Out} < 4.4$
$0.1375 < V_D < 0.4125$	24	None	$3.3 < V_{Out} < 9.9$

3.3 FULL CIRCUIT

Figure 3.7 shows the full circuit block diagram. The block diagram shows the setup for the ADC as well as the fact that the switching signals for each subsequent multiplication stage is

opposite the previous stage. This is accomplished with basic inverters within the analog circuit. Additionally, to avoid metastability, both unclocked inputs to the digital controller, Z2 and reset, are run through two flip flops. For the case of Z2, this means that two extra clock cycles are needed before the output from the comparator is seen by the digital controller. This delay is accounted for in the digital logic.

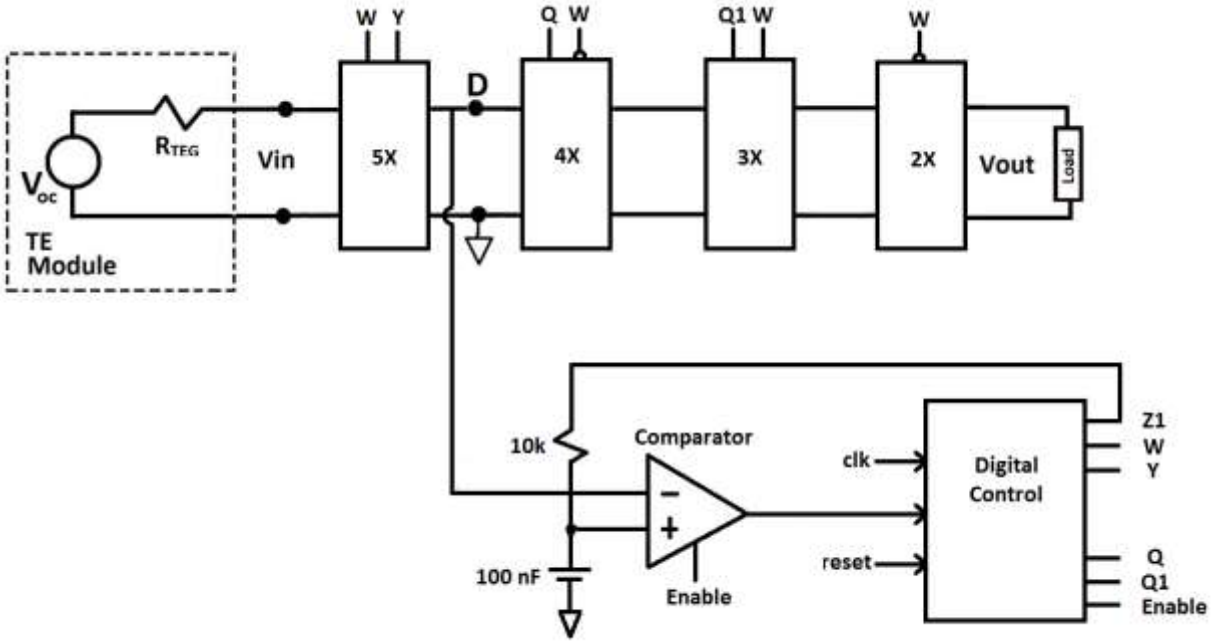

Figure 3.7 Block Diagram

Chapter 4: Results

An initial fabrication run was submitted in January of 2013. The fabricated chips were received in April of the same year. Figure 4.1 shows both fabricated chips.

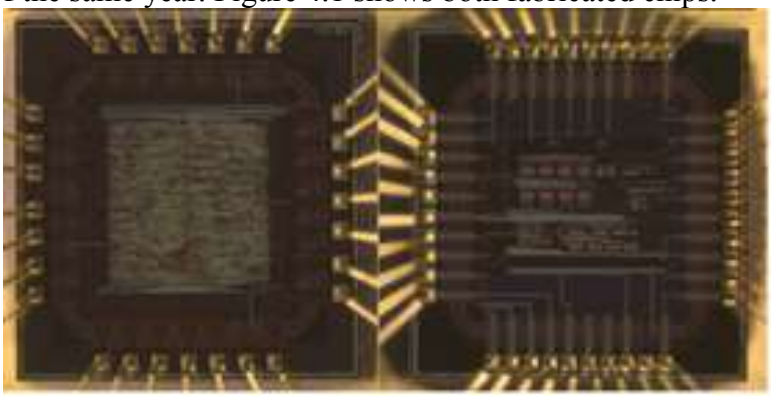

Figure 4.1 (Left) Digital Chip (Right) Analog Chip

The initial chips were tested and did not function properly. The output from the analog chip were generally small voltages that appeared to be generated by noise. After testing, it was determined that the digital chip functioned properly, but the analog chip did not. Looking into the original schematics for the analog design, it became apparent that the 5X stage had improperly connected switches. In the series phase, a misconnection to C3 meant the capacitor was bypassed. There was also no connection to ground for the series connection when configured with signal Y low. This left the capacitors floating. While reviewing the rest of the stages, no connection errors were found, but the high side switching problem in the 2X stage was discovered. Both problems have been fixed for the current iteration of the analog chip.

4.1 Digital Circuit Simulations

The following simulations show the various phases of the digital controller. The digital code is simulated using Xilinx and ISim.

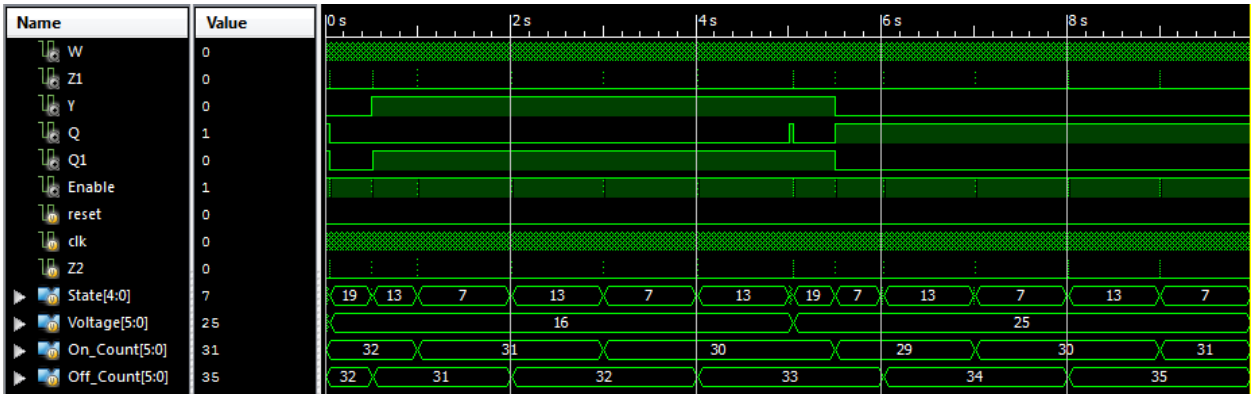

Figure 4.2 Ten second Simulation

Figure 4.2 shows the entirety of the ten second cycle for the digital controller. Of note, this overview shows the functionality of the polarity switch signal, Y, and the two cutoff signals, Q and Q1. Additionally, the changing of On_Count and Off_Count show the duty cycle changes being made to the switching of W.

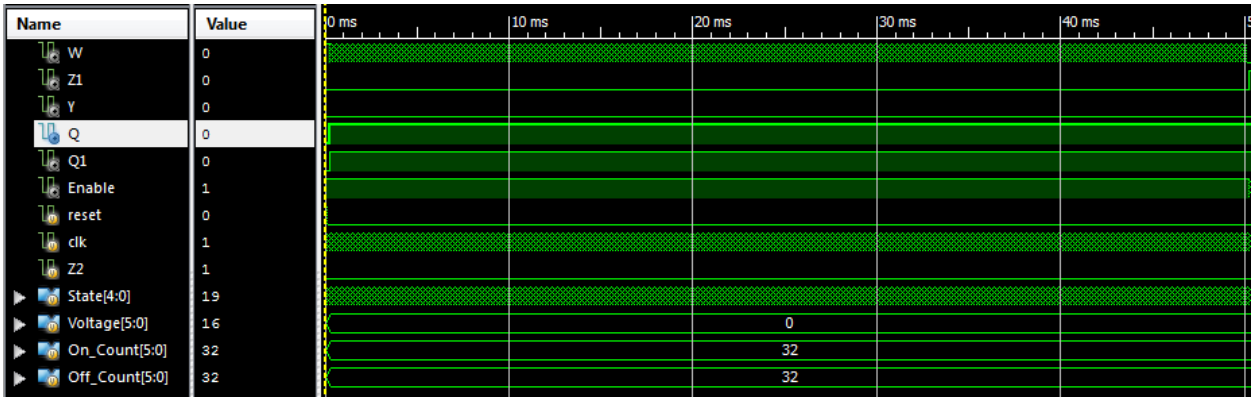

Figure 4.3 Charging stage

The first 50 ms of the simulation are shown in Figure 4.3 in which the W is set to a 10 KHz frequency and both cutoff signals are set high. This phase is to ensure that the 5X stage charges its output capacitor to a full 5*V_{OC} before ADC sampling is started.

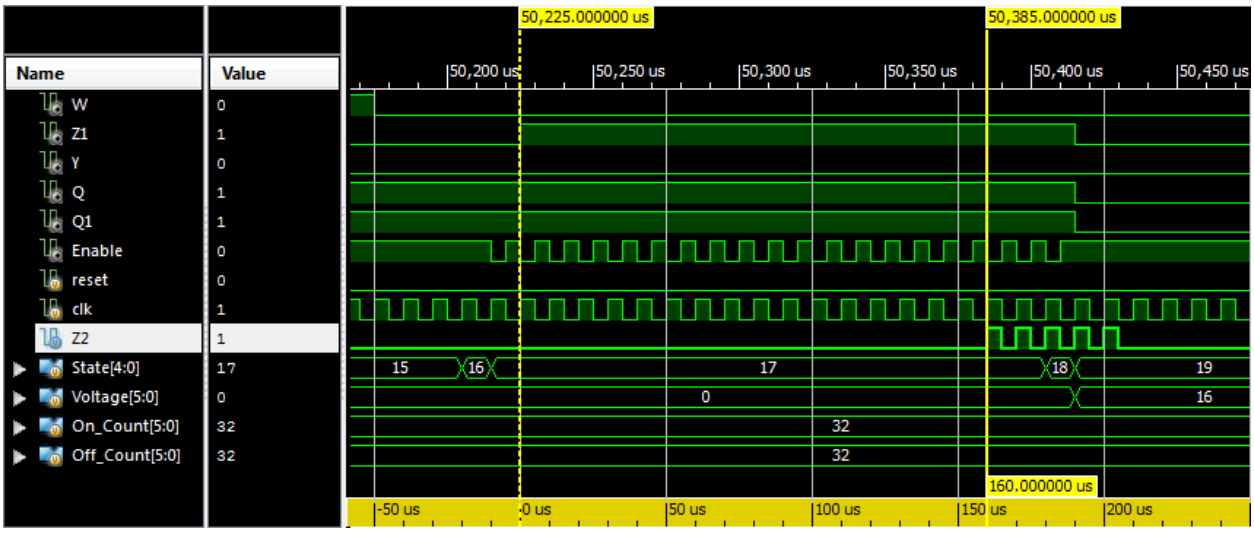

Figure 4.4 5*V_{OC} Sampling

Figure 4.4 shows the 5*V_{OC} sampling phase. Z2 is timed by the test bench. As the yellow measurement bars show, Z2 goes high after 160 µs. As stated before, Z2 is delayed by two clock cycles to sync the signal with the clock and avoid metastability. This can be shown by the two clock cycle delay between when Z2 goes high and state 18 is entered. After state 18, the 160 µs delay is saved in the 6 bit register labelled Voltage. This indicates the voltage was approximately 487 mV based on equation 2.2. Accordingly, the appropriate cutoff signal will be set when the proper stage is entered. Looking at Table 3.1, the 3X stage should be cutoff and this can be seen in Figures 4.2 and 4.6 when signal Q1 goes high at about the 0.5 s point.

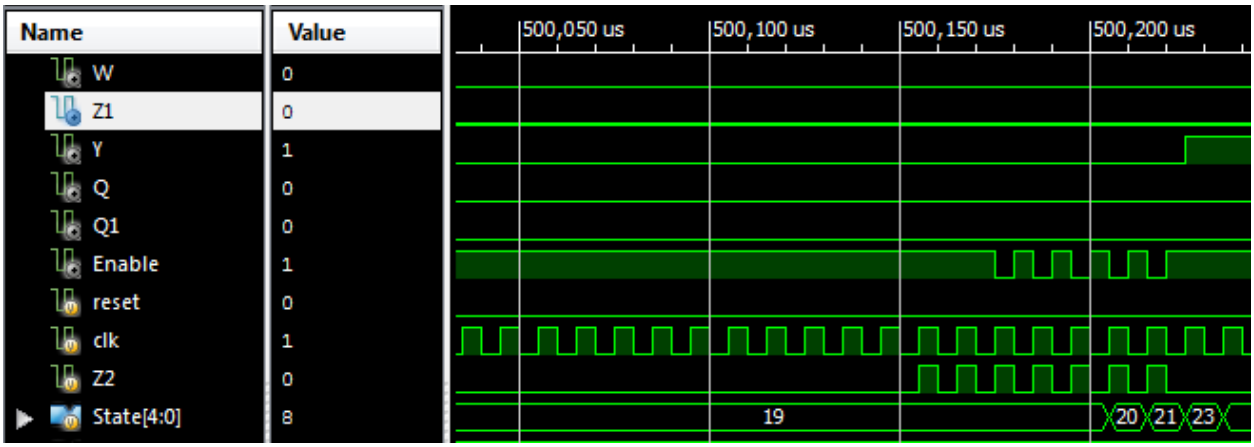

Figure 4.5 Polarity Sensing

Figure 4.5 shows the polarity sensing phase. After waiting until the approximate 500 ms mark to allow the RC capacitor attached to the input of the comparator to fully discharge, the comparator is enabled to test for polarity. In this case, the test bench was designed to simulate a negative voltage. This leads to the Y signal going high at the start of state 23.

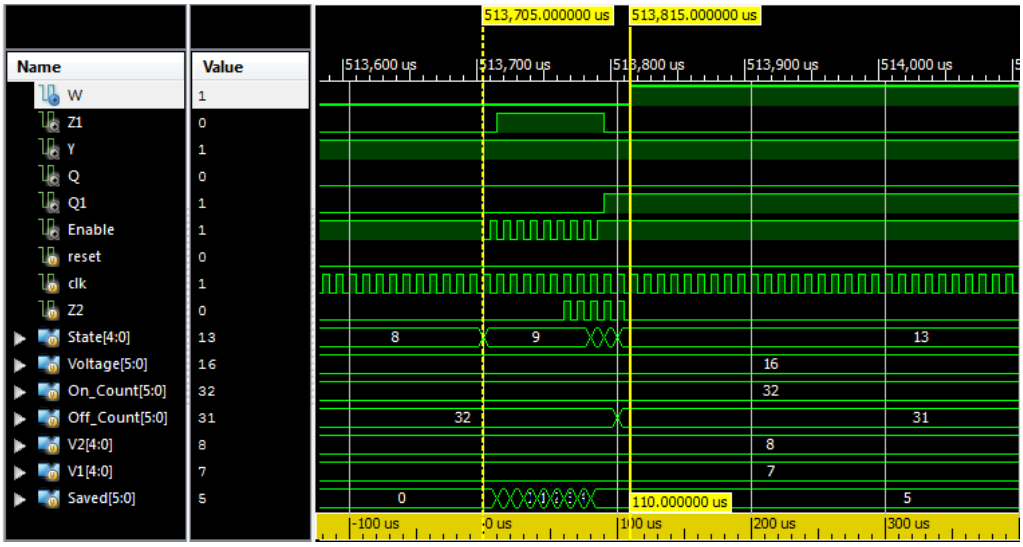

Figure 4.6 Even Second Phase

Figure 4.6 shows the even second phase. As described in the chapter 3, the even second phase is designed to begin 50 clock cycles (500 µs) before W switches from low to high. Z2 was timed to simulate too long of a discharge phase, resulting in a lowering of the off count. For this phase, the 6 bit register named Saved is compared to V1 (45% of 5*V_{OC}). This lowers the number of 1 KHz clock cycles at which W will be held low. The change can be seen taking effect in state 13 where W is set high early.

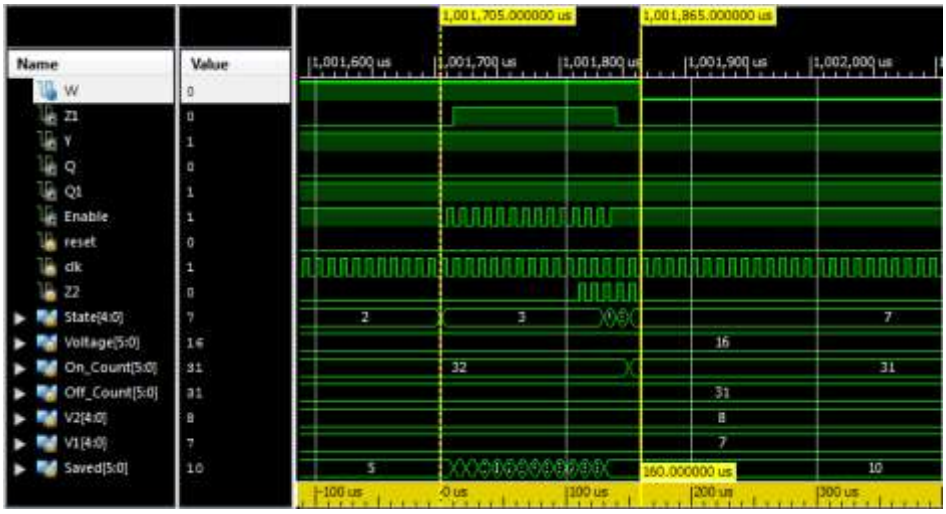

Figure 4.7 Odd Second Phase

Figure 4.7 shows the simulation for the odd second phase. Similar to the even second phase, the odd second phase begins when W is 500 µs away from transitioning from high to low. Z2 was timed to simulate too long of a charge phase, resulting in a lowering of the on count. The Saved register is being compared to V2 (55% of 5*V_{OC}). Similar to the even second phase, the change goes into effect by changing W low early in state 7.

4.2 Analog Circuit Simulations

The analog designs are implemented and simulated using Cadence Virtuoso.

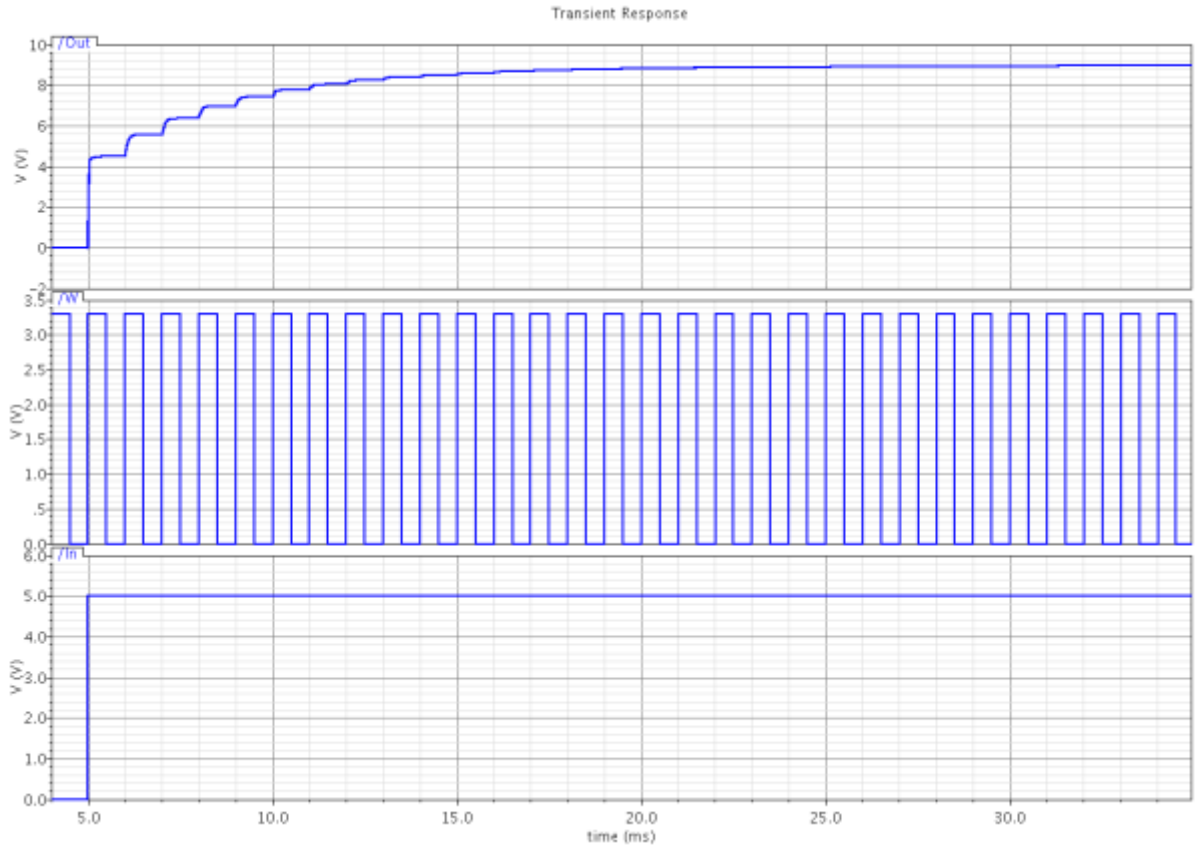

Figure 4.8 2X Stage Simulation

In Figure 4.8, due to the use of, Schottky diodes, a full 2X multiplication is not obtained. With an input of 5V, the output tends towards approximately 9.2 volts with enough time. This is to be expected since the Schottky diodes used have a voltage drop of 390.5 mV. The typical charge pump behavior can be seen with successive charge/discharge phases necessary to reach full charge. W is simulated by a 1 KHz clock signal.

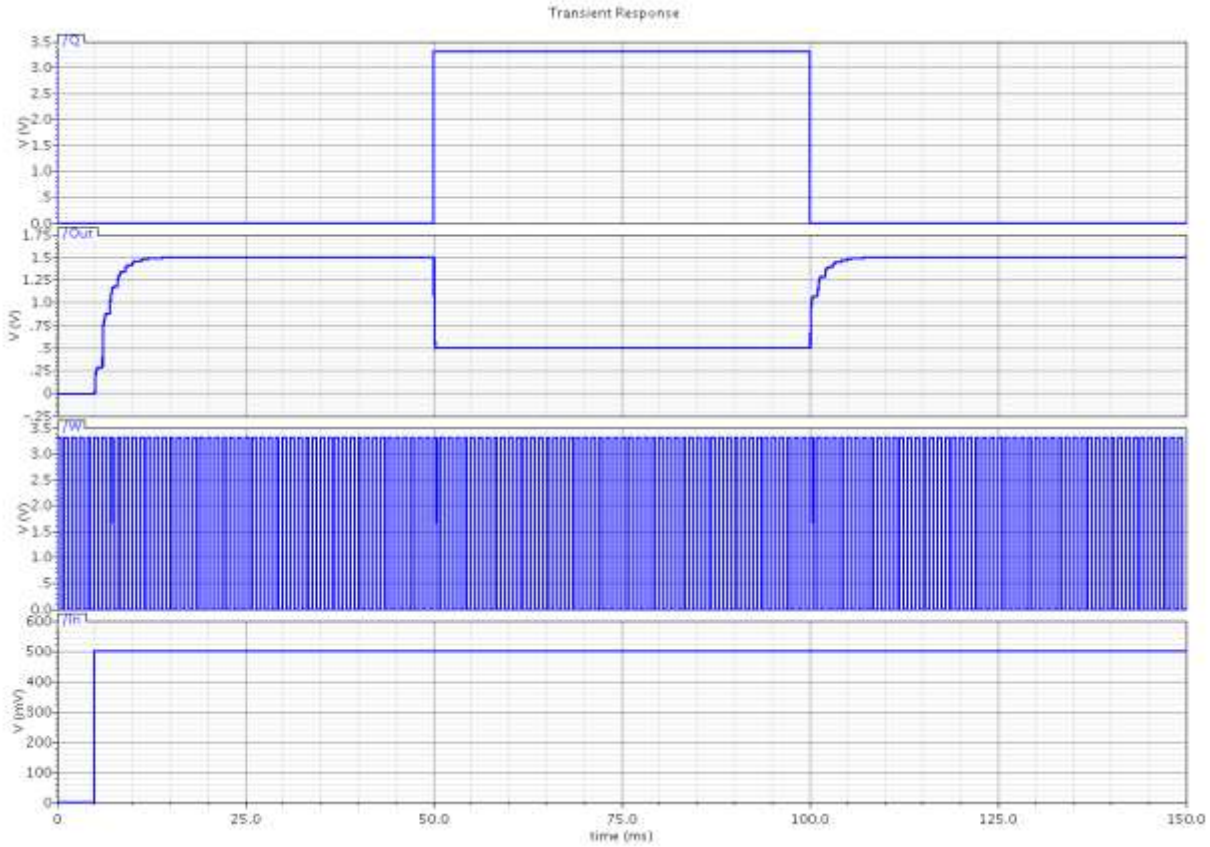

Figure 4.9 3X Stage Simulation

Figure 4.9 shows the behavior of the 3X stage to include the bypass signal Q1. The input voltage is properly multiplied to 1.5 V at the output when Q1 is low. When Q1 is high, the multiplier is bypassed and the input is shorted to the output.

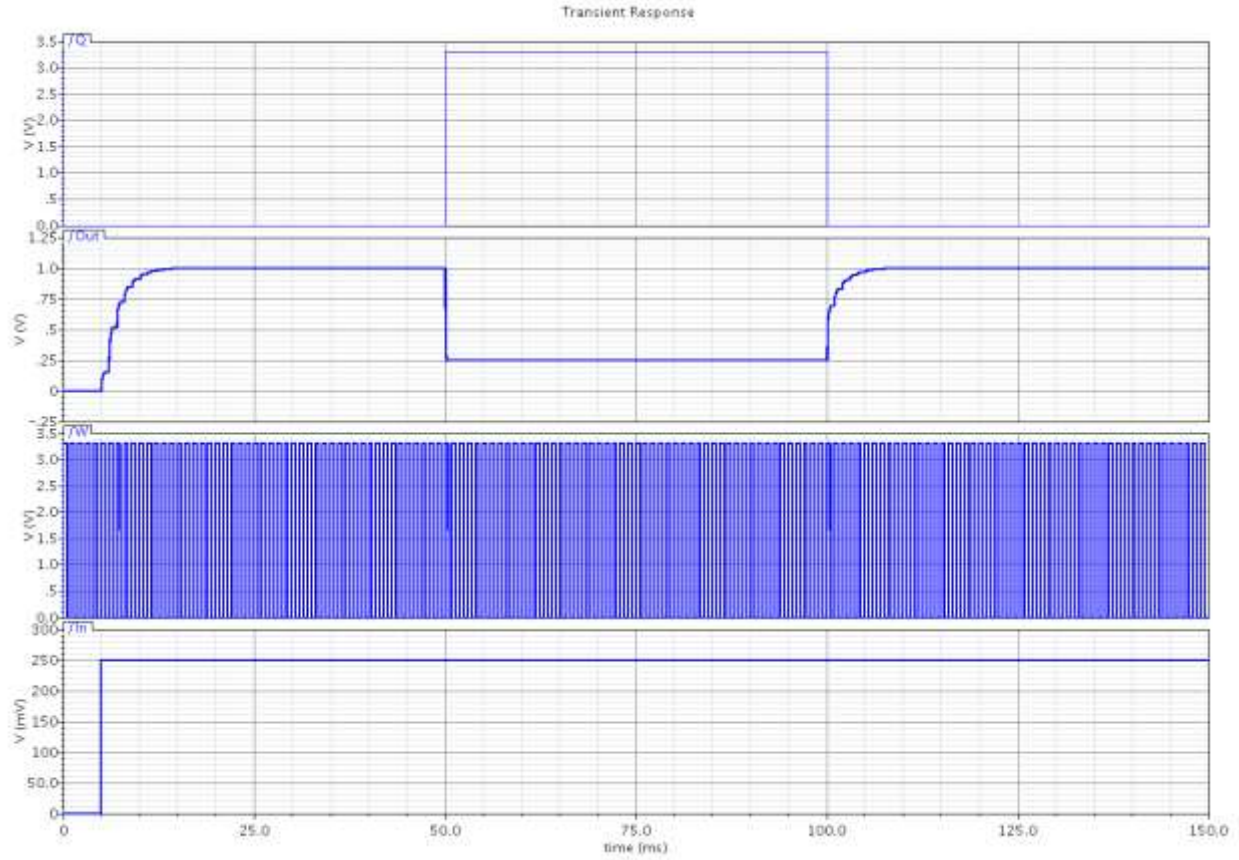

Figure 4.10 4X Stage Simulation

The same test for the 3X stage was used for the 4X stage simulation in Figure 4.10. The 250 mV input is properly multiplied to 1 V when Q is low. When Q is high, the input is shorted to the output.

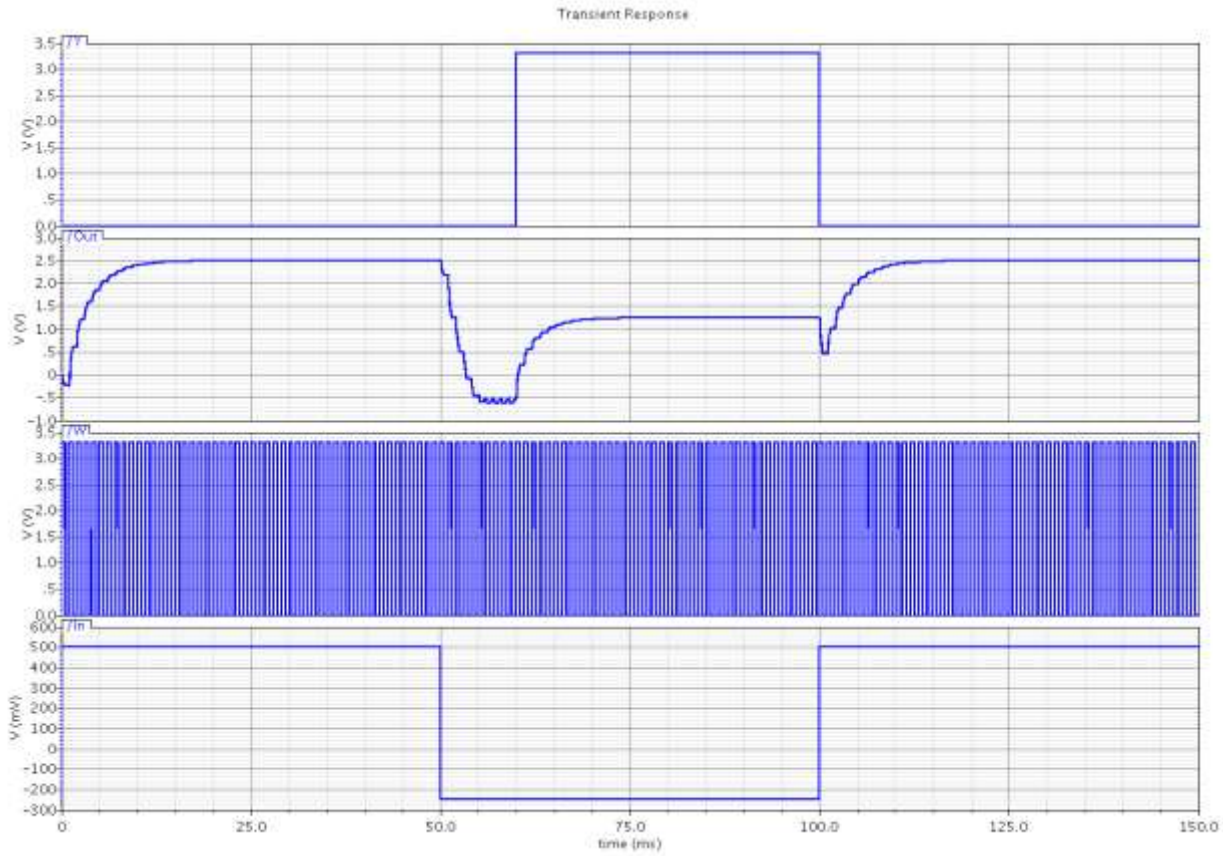

Figure 4.11 5X Stage Simulation.

Figure 4.11 shows the proper functioning of the 5X multiplication as well as the function of the polarity switching. When the input voltage is positive and Y is low, the 500 mV input is properly boosted to 2.5 V. When the voltage goes negative and Y is low, the output is negative, but is charged positive and multiplied appropriately when Y goes high.

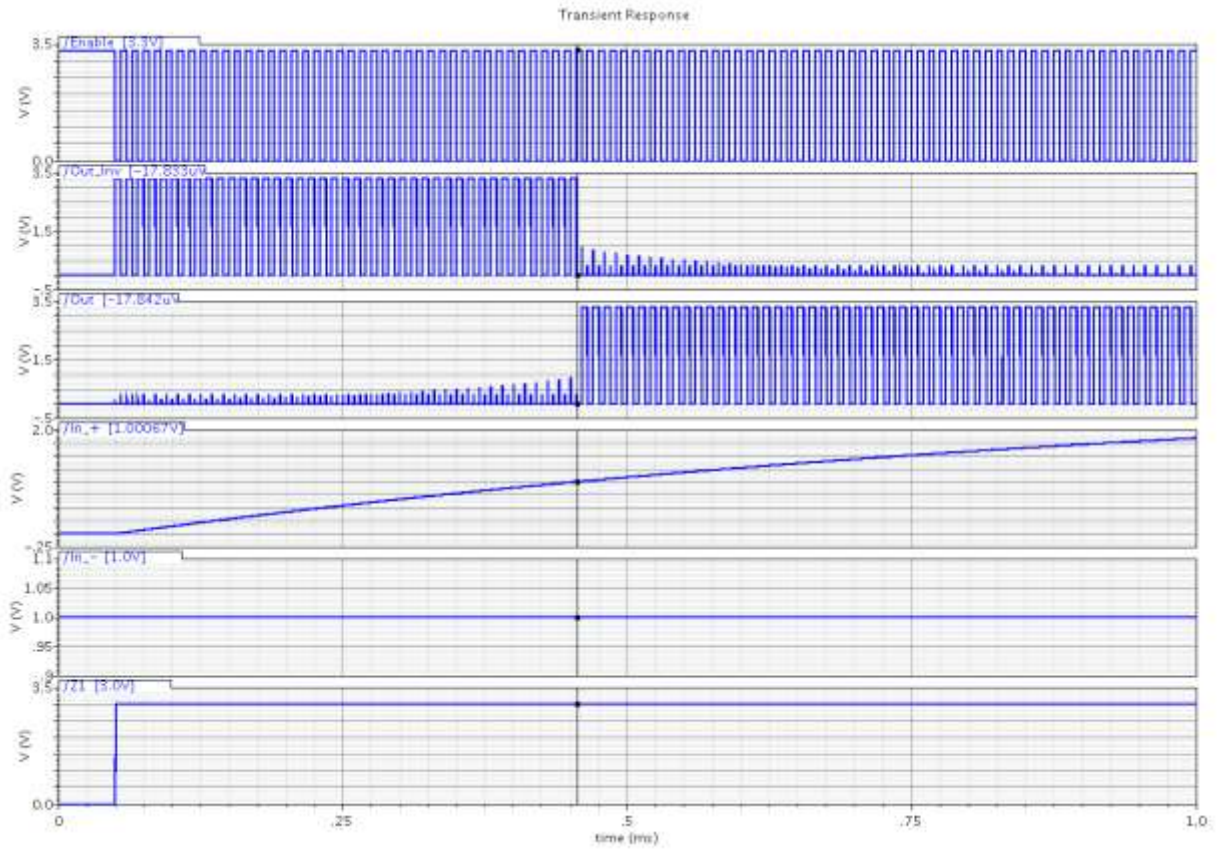

Figure 4.12 Comparator Simulation

In figure 4.12 the full view of the comparator test is shown. Z1 goes high and charges an RC circuit attached to the positive input to the comparator, same as the ADC setup. A vertical line a little past the .45 ms mark shows the point at which the positive input voltage surpasses the negative input voltage. The following falling edge from the enable signal leads to the output going high during low periods of enable. Also, as shown in the first 50 μs, when enable is high, both outputs are set to zero.

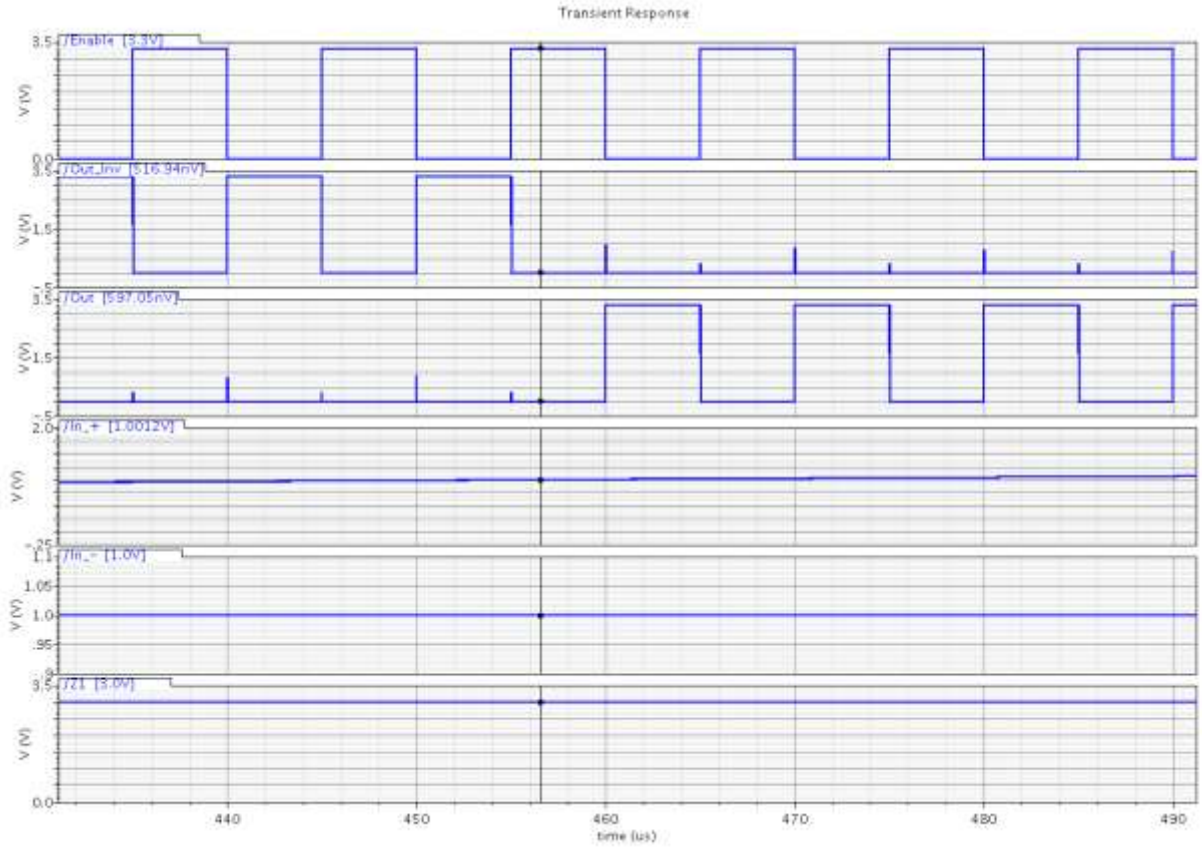

Figure 4.13 Zoomed in Comparator Simulation

In Figure 4.13, the simulation in Figure 4.12 is zoomed into the section where the output is set high. At the 460 µs mark, enable has a falling edge and the output signal is high during the times when enable is low.

4.3 Full Circuit Simulations

For full circuit simulations with both circuits connected, Cadence Virtuoso is used. As such, there were certain limitations. Due to the large number of transistors associated with the synthesized digital controller, simulations take a considerable amount of time. Additionally, the computer hardware used had limited memory. These RAM limitations meant simulations were limited to less than 270 ms. This limited the amount of functionality that can be observed.

Two versions of the digital controller are used. One version of the digital code is for simulation purposes. It eliminates the charging times built into the various phases. This allows observation of functions, such as the duty cycle adjustments and polarity sensing, but, without proper charging times, means that output voltages are wildly inaccurate. The second version of the digital controller is the initial design sent for fabrication. Changes have been made since that time, but software glitches prevent synthesizing the new digital design. However, the changes are minor and the basic functionality is still the same.

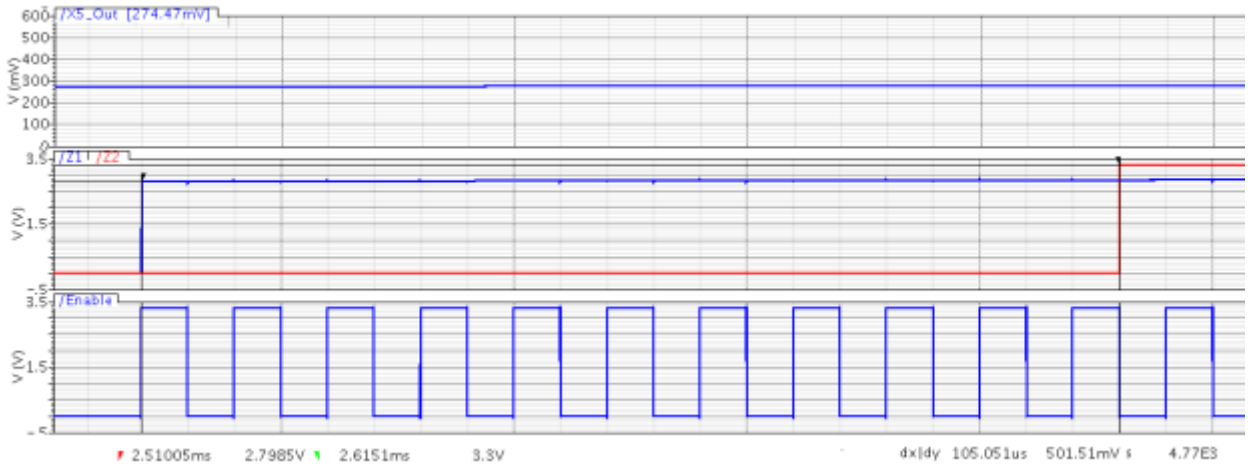

Figure 4.14 ADC Simulation

In Figure 4.14, the simulation has an input voltage of 75 mV. The simulation occurs with the reduced charge time digital controllers and the circuit is in an odd second ADC phase. In the figure, the timing between when Z1 goes high and Z2 goes high is shown as 105 µs. This includes a 15 µs delay due to a negatively enabled flip flop. The flip flop was placed to ensure Z2 stays high and isn't clocked by the enable signal. Due to propagation delay, Z2 was going high a few microseconds after a clock rising edge. This meant that the digital clock never registered Z2 going high. With the flip flop added, Z2 latches high as long as the output from the comparator generates a high clocked signal. However, it introduces a 15 µs delay. This simulation shows, taking into consideration the delay, that 90 µs have passed between Z1 and Z2 going high. According to equation (2.2) this indicates a voltage of 284 mV, which is close to the actual 274 mV output from the 5X stage.

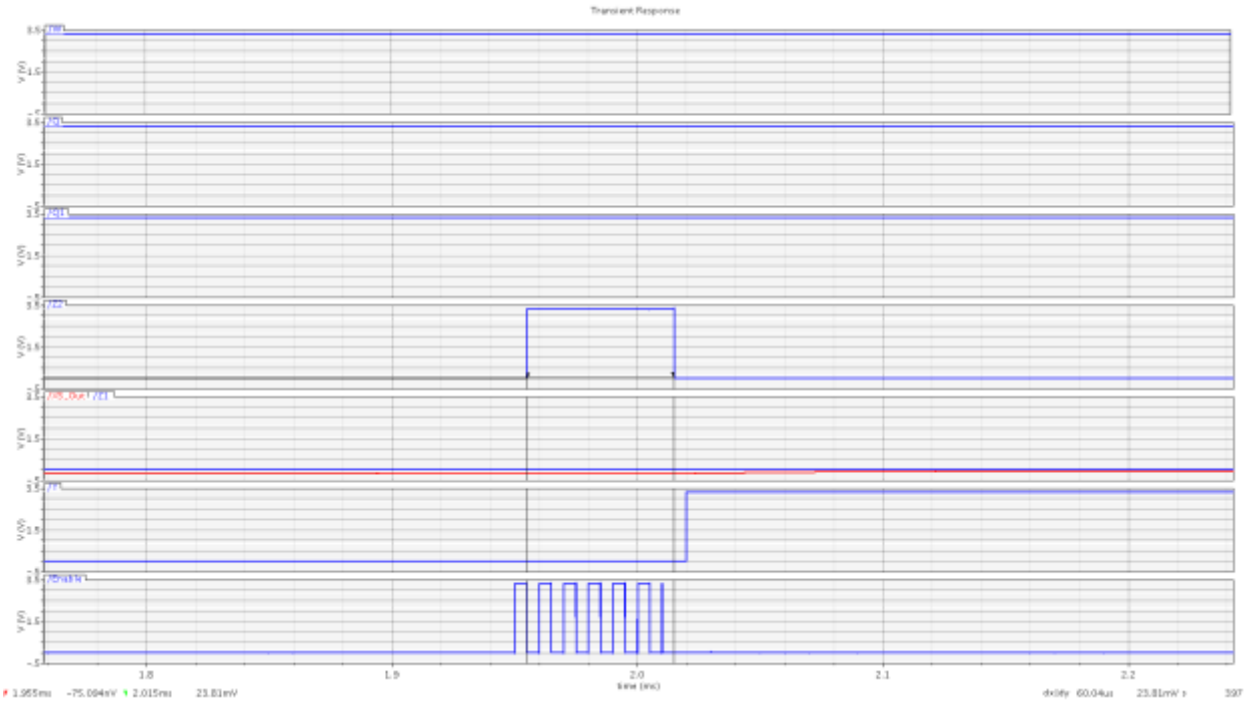

Figure 4.15 Polarity Sensing

In figure 4.15, the polarity sensing behavior is showing. The input voltage is set to -200 mV. In this phase, W, Q, and Q1 are set high. Z1 is set to zero. The red line indicates that the 5X output is lower than Z1. After a falling edge on the enable signal, Z2 latches high. Shortly after, signal Y goes high.

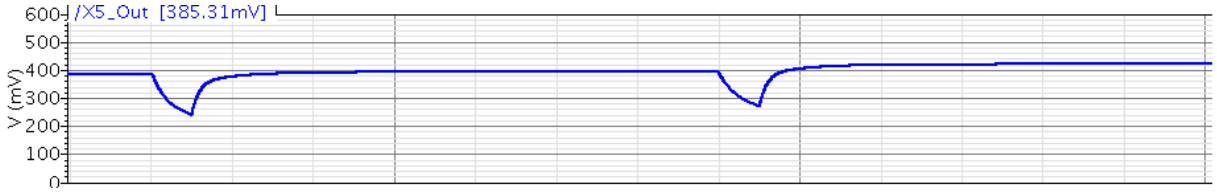

Figure 4.16 Optimization Effects

Figure 4.16 shows the effects of several optimization phases. This is shown in the short discharge and increased charging.

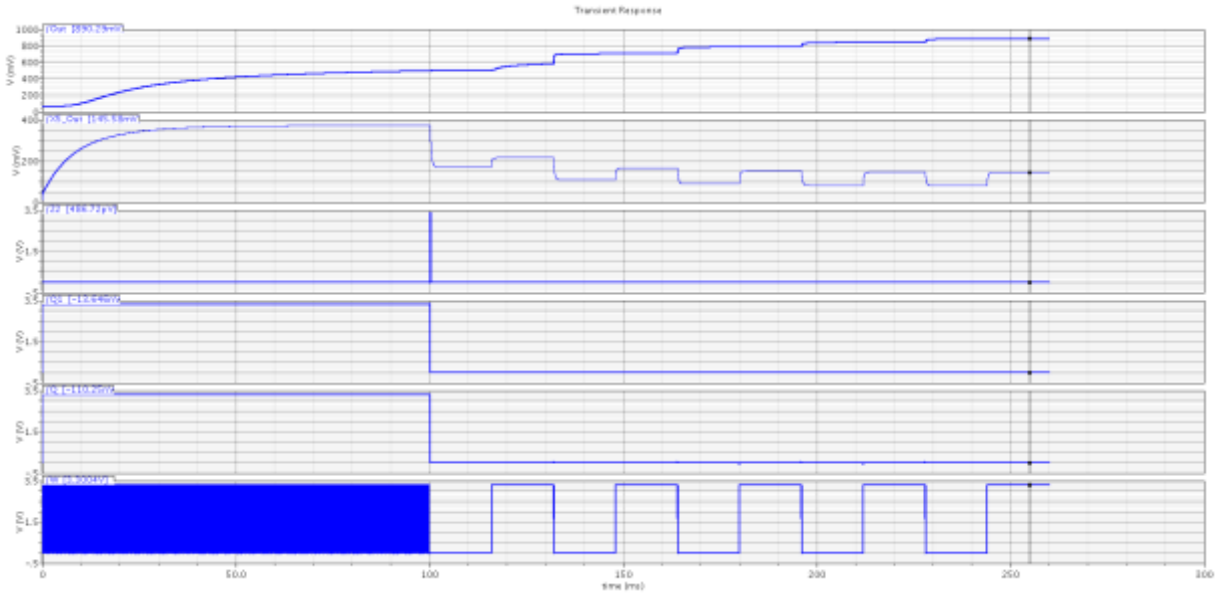

Figure 4.17 Full Simulation (75 mV)

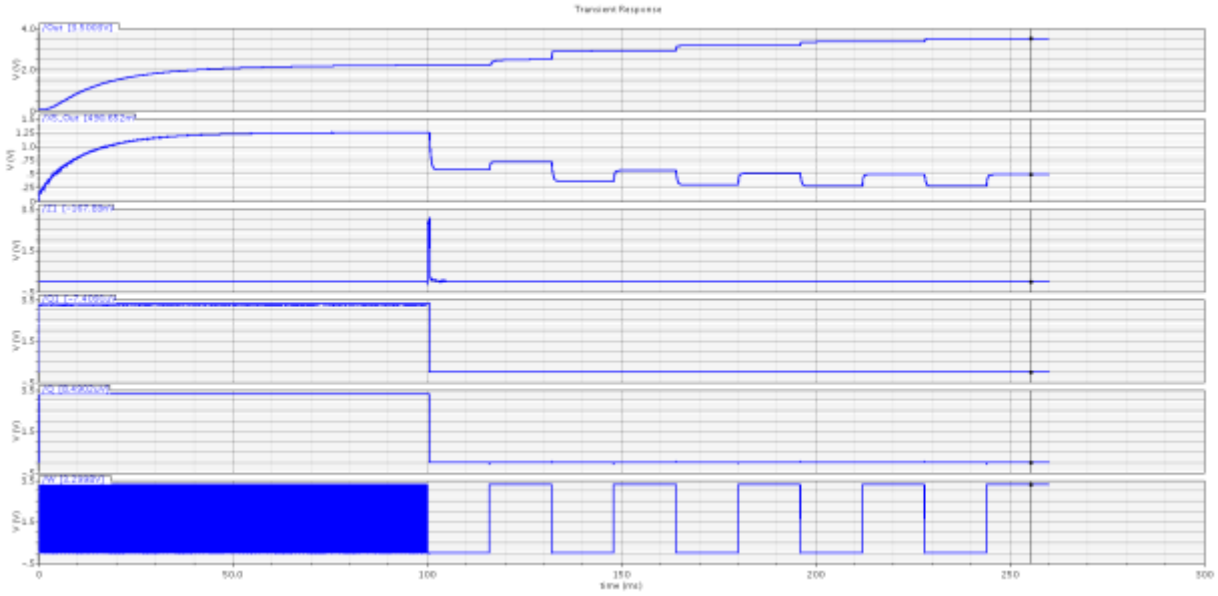

Figure 4.18 Full Simulation (250 mV)

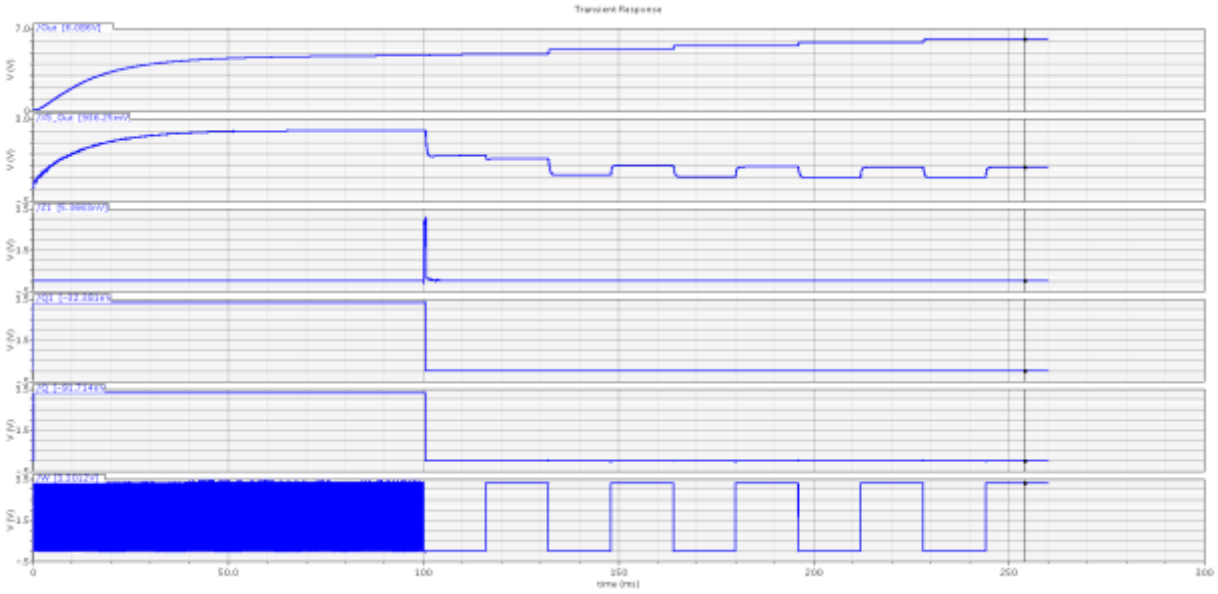

Figure 4.19 Full Simulation (500 mV)

In figures 4.17, 4.18, and 4.19, show the maximum length simulation possible without causing computer crashes. The 5X out shows the effects of the attempted optimization. However, the voltage appears to be going below 50% for all three simulations. No optimization adjustment phases have occurred and the long W period increases the length of time it takes to charge the circuit, so the output never reaches maximum voltage. A longer test could have yielded more meaningful results.

Chapter 5: Conclusion

After receiving, testing, and learning from the mistakes of the first fabricated version of the digital and analog chips, considerable testing and review of the designs leads to confidence in the second version providing a substantial proof of concept. The full schematic simulations are short, but provide enough of a glimpse to have confidence that the next fabrication will provide a working product that will give considerable feedback. Undoubtedly, more changes will have to be made to perfect the system.

The individual circuits show that they function ideally by themselves, but the full interaction between the two is unknown. Initial review of the full system simulations indicate that adjustments to the optimization algorithm may be necessary. The period for parallel/series switching may need to be shortened or initialized to a smaller value since a starting period of 64 ms with 50% duty cycle drops the voltage well below 50% of $5*V_{OC}$. Additionally, the multiplication ranges shown in Table 3.1 may need to be reconsidered to take into account that the analog chip will be, predominantly, operated at $2.5*V_{OC}$ for optimization purposes.

5.1 Future Work

As discussed previously, optimization of transistor sizes will still need to be done to maximize circuit efficiency. Initial plans are to use SPICE simulations to determine the appropriate transistor sizes for each stage.

Testing of fabricated chips will also, inevitably, lead to adjustments to the logic of the digital controller. One aspect of digital logic that will need to be explored is ensuring that the non-bypassed stages are properly switched. Currently, the 5X and 3X stages follow the same series/parallel switch timing while the 4X and 2X stages are inverted. This means that, should the 4X stage be bypassed, subsequent stages will have synchronized series/parallel switching. A similar situation arises if the 3X stage is bypassed. This is not desirable behavior. Figure 5.1 shows

a proposed design that was to be added to the analog circuit, but was discarded to avoid additional $R_{DS(on)}$ losses. This logic cannot be easily implemented through the digital controller, because the switch inputs to each stage are not accessible from outside of the analog system. The inversion currently occurs within the analog system.

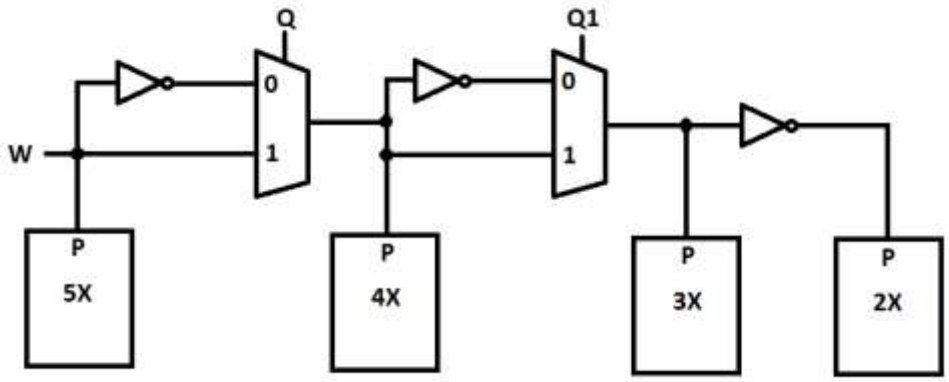

Figure 5.1 Stage Switch Logic

Analog design changes may also be implemented in the form of 3X and 4X stages capable of unlimited output voltages. This will allow the possibility of bypassing the 2X stage to give better customization of the output voltage ranges to reduce resistive power losses at the load.

Finally, when the designs are closer to finalization, both analog and digital systems will be integrated into a single chip. This will open up the possibility of the digital logic being able to individually address the switch inputs to each stage to fix the problem of back to back stages having synchronized parallel/series switching. A single package will also reduce overall system size.

References

[1] Daugherty, Kevin M. *Analog-to-digital conversion: a practical approach*. McGraw-Hill, Inc., 1995. Print.

[2] DiSalvo, Francis J. "Thermoelectric cooling and power generation." *Science* 285.5428 (1999): 703-706.

[3] Figueiredo, Pedro M., and Joao C. Vital. "Kickback noise reduction techniques for CMOS latched comparators." *IEEE Transactions on Circuits and Systems II: Express Briefs* 53.7 (2006): 541-545.

[4] Glatz, Wulf, et al. "Bi_2Te_3-Based Flexible Micro Thermoelectric Generator With Optimized Design." *Journal of Microelectromechanical Systems* 18.3 (2009): 763-772.

[5] Goldsmid, H. Julian. "Bismuth telluride and its alloys as materials for thermoelectric generation." *Materials* 7.4 (2014): 2577-2592.

[6] Palumbo, Gaetano, and Domenico Pappalardo. "Charge pump circuits: An overview on design strategies and topologies." *IEEE Circuits and Systems Magazine* 10.1 (2010): 31-45.

[7] Razavi, Behzad. *Principles of data conversion system design.* Piscataway: IEEE Press, 1995. Print.

[8]Seeman, Michael D., and Seth R. Sanders. "Analysis and optimization of switched-capacitor DC–DC converters." *IEEE transactions on power electronics* 23.2 (2008): 841-851.

[9] Sun, Kai, et al. "Evaluation of high step-up power electronics stages in thermoelectric generator systems." *Journal of electronic materials* 42.7 (2013): 2157-2164.

[10] TXL Group, Inc., “Thermoelectric Generator Module with lower internal resistance and 127 Thermoelectric Couples,” TXL-127-03L datasheet, 2014.

[11] Youn, Nari, et al. "Achieving maximum power in thermoelectric generation with simple power electronics." *Journal of Electronic Materials* 43.6 (2014): 1597-1602.

Vita

Rene Brito was born in El Paso, Texas in 1984. His parents are Pedro and Evangelina Brito. He graduated from the Montwood High School, El Paso, Texas, in 2002. Shortly after graduating high school, he went to basic training for the United States Air Force. After attending basic training and technical school, he was stationed in Minot AFB, North Dakota. His first three years were spent as a cruise missile maintainer before accepting a special duty assignment as a squadron instructor for the 5th Munitions Squadron.

After leaving the Air Force in 2008, Rene took time off before enrolling at the University of Texas at El Paso (UTEP) in the spring of 2010. While enrolled as an undergrad, he worked as a systems administrator for the school's engineering department. He completed his bachelor's degree in Electrical Engineering in the spring 2014. He continued his education at UTEP as a graduate student, pursuing a master's degree in computer engineering. While attending, Rene worked at TXL-Group, Inc. from 2014 to 2015.

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